Novel Quantum Nanodevice-based Logic Circuits Utilizing Semiconductor Nanowire Networks and Hexagonal BDD Architecture

Seiya Kasai

Graduate School of Information Science and Technology and Research Center for Integrated Quantum Electronics, Hokkaido University
N14, W9, Sapporo 060-0814, Japan E-mail: kasai@rciqe.hokudai.ac.jp

Abstract – Novel quantum nanodevice-based logic circuits utilizing III-V semiconductor nanowire network structures together with a hexagonal binary-decision-diagram (BDD) logic architecture are presented. An ultra-small-size and ultra-low-power digital logic processor, "nanoprocessor (NPU)", based on the hexagonal BDD quantum circuit for an ultra-small knowledge vehicle is also described.

I. INTRODUCTION

Development of information technology (IT) has been achieved by the progress of Si CMOS LSI technology. A demand of recent ubiquitous IT is to extend spectrum of computer technology as shown in **Fig. 1(a)**, namely, the one direction is higher speed and higher volume information processing and another is tiny and ultra-law power signal processor embedded in every objects and operating almost buttery free, such as smart dusts [1] or ultra-small knowledge vehicles [2] as shown in **Fig. 1(b)**. For their realization, further progress of the LSI technology is really necessary. However, the Si CMOS LSI technology following Moore's low is now facing various limitations, such as tremendously high power consumption, due to the break down of Dennard's scaling law.[3,4] Therefore, paradigm shifts of the LSI technology, corresponding to inventions of transistor and integrated circuit, are strongly required.

Quantum nanodevices and their integrated circuits has been expected to overcome the limitation of the Si CMOS technology because of their rich functionality, small size and high speed operation with low power. Although they have always suffered from various problems such as low operation temperature and low gain, recent rapid progress of nanotechnologies have begin to solve the problems. Exploration of new logic architectures and circuit approaches has given new opportunities of realistic applications to quantum nanodevices. Quantum computer is one of the most interesting applications of quantum nanodevices because of its fantastic performance from the super parallelism of the quantum mechanics, and many extensive researches have made on its realization. On the other hand, in case of tiny ultra-law power processors, there has been no solution to implement by quantum nanodevices yet even with their improtance. For the latter purpose, our research group proposed and has been investigated a hexagonal BDD logic quantum circuit approach [5,6], which utilizes a binary-decision-diagram (BDD) logic architecture instead of the CMOS logic gates, together with the sophisticated III-V semiconductor quantum nanostructure fabrication technology.

In this paper, recent research and development of the hexagonal BDD logic quantum circuit technology by author's group and its application to a novel ultra-small and low-power processor, "nanoprocessor" [7,8] are described.

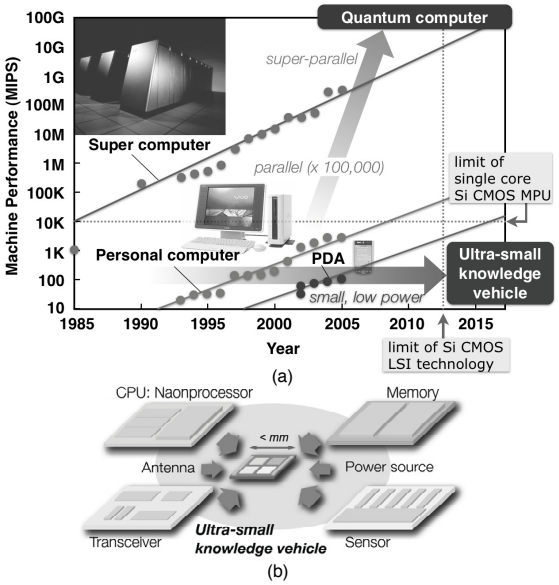


Figure 1. (a) Evolution of computer performance and technology trend and (b) concept of an ultra-small knowledge vehicle.

Ⅱ. Concept of Hexagonal BDD Quantum Circuit and Its Implementation

Basic concept of the hexagonal BDD quantum circuit is schematically shown in **Fig. 2**. This circuit utilizes the binary-decision diagram, BDD, for its logic architecture [9,10], instead of the conventional logic gate architecture. The BDD is a representation scheme of a logic function by a directed graph and its circuit processes the binary logic. The BDD consists of roots, terminals and node devices as shown in **Fig. 2(a)**. Each node device has one entry branch and two exit branches. Its function is to select one of the exit branches for the information messenger coming from the entry branch according to the binary logic input, x_i = 0 or 1, as shown in **Fig. 2(b)**. The logic function, f, is evaluated by transferring the messenger from the root to terminals through the path selected by each node device. When the messenger reaches the terminal-1, then the logic is true, or when it reaches the terminal-0, then the logic is false.

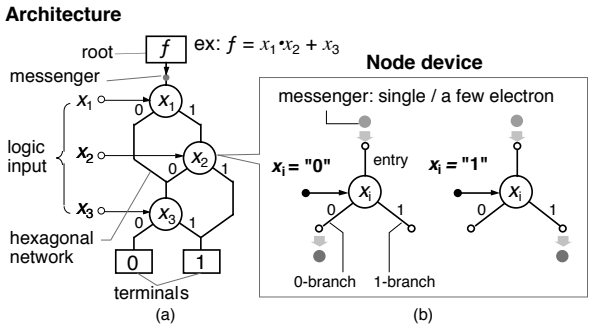


Figure 2. Basic concept of hexagonal BDD quantum circuits.

Key features of the hexagonal BDD quantum circuit are; (1) ultra-low power consumption by ultra-low-current-drive with single or a-few electrons, and (2) compact circuit layout for a logic graph representation utilizing hexagonal networks.

The feature (1) results from complete separation of input and output in the BDD. This is quite different from the CMOS logic architecture in which many logic gates connect in cascade. This allows us to use any medium as the messenger as well as to use devices with small transfer gain and less uniformity.[10] Then, we can use single or a-few electrons and quantum nanodevices for messengers and their control, respectively. As seen in **Fig. 3**, reduction of electrons per bit leads to the reduction of power-delay product, PDP. Here, it should be noted that classical devices such as MOSFETs can only control many electrons statistically and can never control each electron. If the number of electrons is less than 100, they suffer from noise due to statistical fluctuation of 10 % as shown in **Fig. 3**. Only quantum nanodevices utilizing the

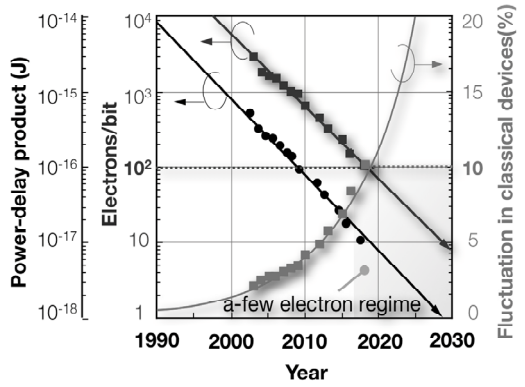


Figure 3. Estimated PDP and electrons per bit as a function of yea from ITRS data [4]. Statistical fluctuation in classical devices fron the number of electrons is also plotted.

quantum mechanics can control small number for electrons accurately within the Heisenberg uncertainty in which the minimum PDP is defined by the Plank constant. In order to realize ultimately low power dissipation of circuits, we utilize the quantum mechanics positively in the hexagonal BDD.

The feature (2) comes from the three-fold symmetry configuration of a node device. Arranging node devices naturally results in a hexagonal layout as shown in **Fig. 2(a)**. Thus, we represent a logic graph directly on hardware utilizing a hexagonal network structure for high-density integration of the node devices.

For hardware implementation of the hexagonal BDD quantum circuits, we have investigated a GaAs-based hexagonal nanowire network structures controlled by nanometer-scale Schottky wrap gates (WPGs) [11], as shown in **Fig. 4(a)**. The WPG is a structure in which a nanometer scale Schottky gate is wrapped around a nanowire. It has a simple lateral planar structure suitable for planar integration and can produce tight gate control and strong electron confinement. The nanowires are formed usually by wet chemical etching of AlGaAs/GaAs modulation-doped heterostructure

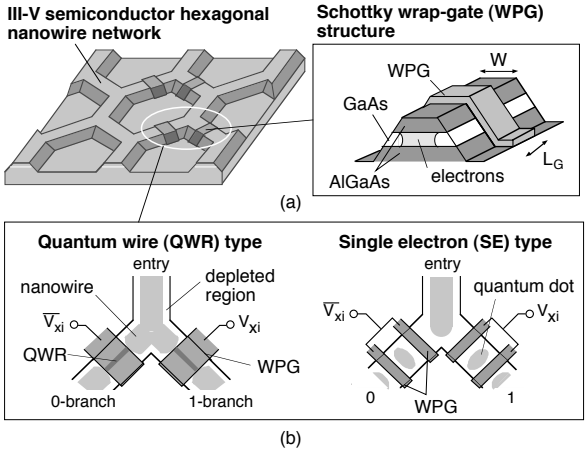


Figure 4. (a) Implementation of the hexagonal BDD quantum circui and Schottky wrapgate (WPG) structure and (b) designs of WPG-based BDD quantum node devices.

wafers using electron beam (EB) lithography. We can utilize combination of superb quantum transport along high-quality heterointerface with high electron mobility and well-behaved GaAs Schottky interfaces with high barrier height.

Various types of node devices can be designed by arranging WPGs on nanowire networks, as shown in **Fig. 4(b)**. A nanowire with a single WPG operates as a quantum wire transistor (QWRTr). A nanowire controlled by a couple of narrow WPGs with a short spacing produces double tunneling barriers with a quantum dot in between with suitable WPG voltages. This operates as a single electron transistor (SET). The SE node devices can precisely control single electrons, and can realize small values of PDPs. The QWR node devices have simple structure to fabricate, and useful for feasibility study of integration.

III. Device Characteristics

Figure 5(a) shows an SEM image of a fabricated QWR-type node device. *I-V* characteristics of an exit-branch nanowire with a WPG at room temperature (RT) is shown in **Fig. 5(b)**. WPG devices can operate as a conventional FET as shown in **Fig. 5(b)**. At low temperature, WPG-controlled nanowires in QWR and SE node devices showed clear conductance quantization and conductance oscillation characteristics, respectively, as shown in **Fig. 5(c)**. These characteristics in the quantum regime were maintained up to a few ten K. Fabricated devices exhibited clear path switching characteristics based on quantum transports as shown in **Fig. 5(d)** for a QWR node device as an example. The path switching operation was also obtained even at RT as also shown in **Fig. 5(d)**, even when quantum transport vanished. This is because WPG-controlled nanowires can also operate as a conventional FET at RT as seen in **Fig. 5(b)**. The difference between the operations in low and high temperatures is the number of electrons in a messenger or in a bit operation. The number of electrons, N, should be increased to overcome fluctuations increasing bit error rate in higher temperatures. This corresponds to increase of the PDP since it is given by $C_G\Delta V_G^2 = Q\Delta V_G = Ne\Delta V_G$, where C_G is gate capacitance, Q is the total charge and e is an electron charge. As described previously, in case of the classical regime, N should be larger than 100 to suppress the statistical fluctuation less than 10 %. Thus, $N << 100$ is possible only in quantum nanodevices.

We estimated PDP values of fabricated WPG-based QWR and SE devices and they are summarized in **Table I**. The values were estimated using PDP = $C_G\Delta V_G^2$.[6] Gate capacitances were evaluated experimentally from V_G-dependent magnetoresistance measurement for QWR devices [12,13] and from Coulomb blockade characteristics for SE devices [6]. Small PDP value of 10^{-22} J was obtained in SE devices at 1.6 K. This value is four orders of magnitude smaller than 10^{-17} J of a 20 nm-gate Si MOSFET at 300 K [14]. PDPs for QWR devices were 10^{-20} J for the WPG length, L_G = 630 nm, and 10^{-21} J for L_G = 65 nm. However, there is a trade off between the PDP value and temperature. Taking account of $\Delta V_G \propto kT/e$ in QWRTrs and SETs and PDP $\propto T^2$, PDPs of the SE

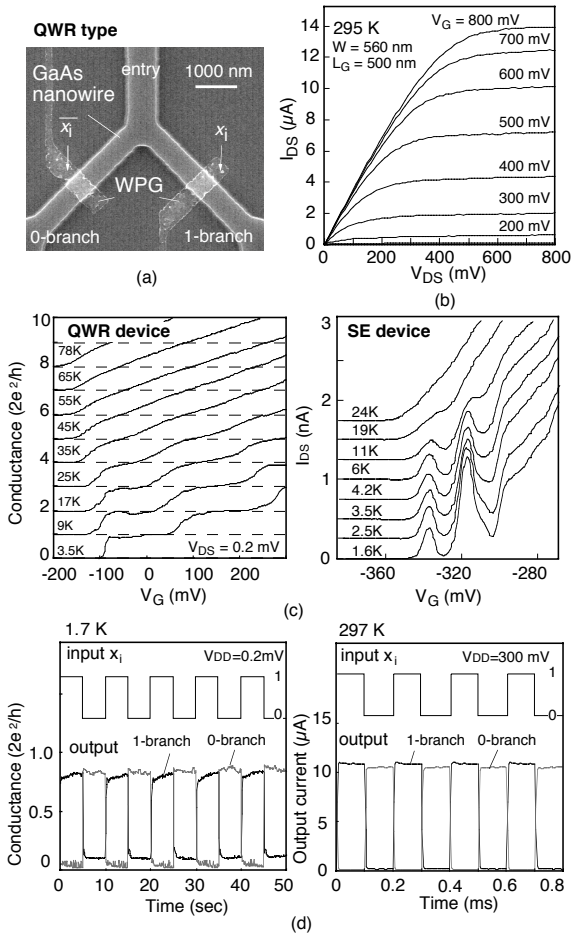


Figure 5 (a) SEM image of fabricated WPG-based QWR-type BDD quantum nodedevice, (b) its I_{DS}-V_{DS} characteristics, (c) conductance characteristics of QWR- and SE-type devices, and (d) path switching characteristics of the QWR-type node devices.

Table I Evaluated power-delay products.
The gray values at 300 K are estimated from PDPs at 1.6 K.

Device	L_G	PDP	
		1.6 K	300 K
WPG QWR Tr	630 nm	10^{-20} J	10^{-16} J
WPG QWR Tr	65 nm	10^{-21} J	10^{-17} J
WPG SET	30 nm	10^{-22} J	10^{-18} J
Si MOSFET (Lab.)	20 nm		10^{-17} J

and QWR devices at 300K are deduced 10^{-18} J and 10^{-17} J, respectively. It is found that there is still an advantage of quantum nanodevices in power consumption at RT. These results clarify the capability of ultra-low power consumption of the hexagonal BDD quantum circuits. The obtained PDPs of QWR devices were found to depend on the WPG size. This indicates that further small PDP values can be realized by scale down of the WPG size. In **Fig. 6**, PDPs for various electron switching device are plotted as a function of year. The exponential decrease of PDP values through the change of fundamental devices for circuit constructions can be seen, but recent and future trend by CMOSs is predicted to be stalled. The obtained results for the QWRTr and the SET are also plotted in **Fig. 6**, which shows that the scalability of PDP in electron switching devices can be maintained in future by quantum nanodevices.

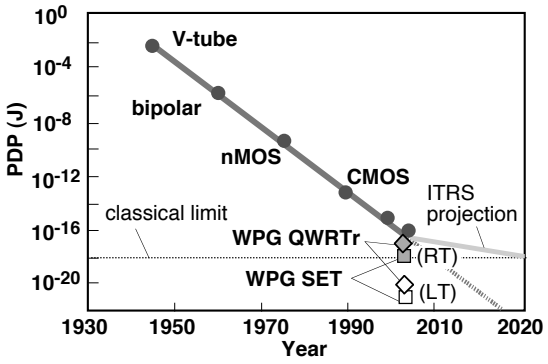


Figure 6. Evolution of PDPs for electron devices.

IV. Logic Elements and Subsystems

Hexagonal BDD-based elemental logic circuits integrating several node devices were successfully fabricated and their correct operations were realized. **Figure 7(a)** shows an SEM image of a fabricated QWR-type AND logic and its input-output waveforms. It showed correct logic operation utilizing the conductance switching between 0-th and 1st steps of the quantized conductance, $2e^2/h$. It could also operate as an AND logic in the classical regime at room temperature, adjusting gate and terminal voltage. SE-type OR logic was also fabricated and their correct operations were confirmed both in quantum regime with SE transport and in the classical regime with many-electron transport, as shown in **Fig. 7(b)**.

It should be mentioned that any combinational circuits can be designed utilizing the hexagonal BDD quantum circuit approach by an universal circuit design guideline; (1) omitting of terminal-0 (because the logic

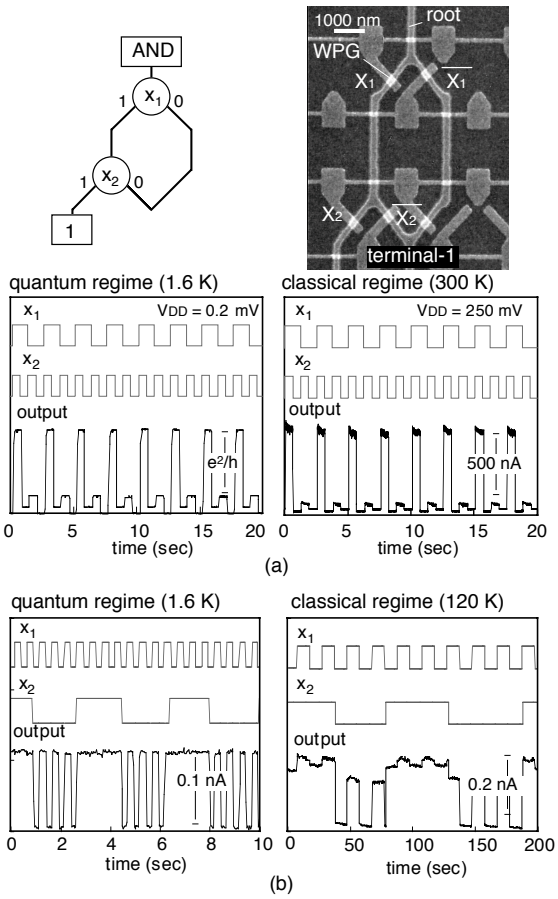


Figure 7. Basic BDD logic elements and their operations. (a) QWR-type AND logic and (b) SE-type OR logic.

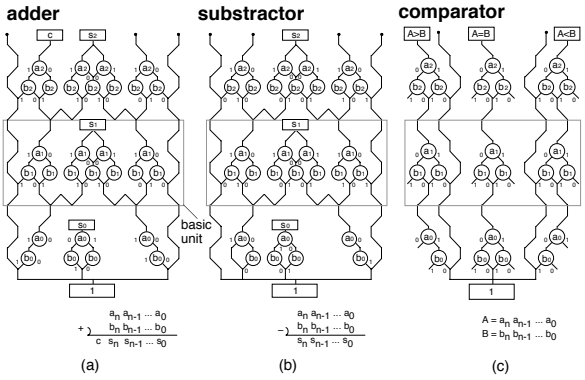
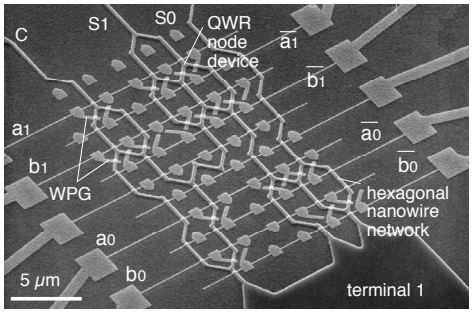


Figure 8. Circuit diagrams of hexagonal BDD subsystems: (a) adder, (b) substractor and (c) comparator.

can be determined by checking whether the messenger arrives at the terminal-1 or not), (2) representing a logic function by a principal disjunctive canonical form, and (3) removing redundant/equivalent nodes and branches without causing nanowire crossing. Various sub-systems for arbitrary bit size were successfully designed using this design guideline as shown in **Fig. 8**, including n-bit adder, substractor and comparator. In these examples, subsystems for any bit size can be realized by stacking basic units as indicated by boxes

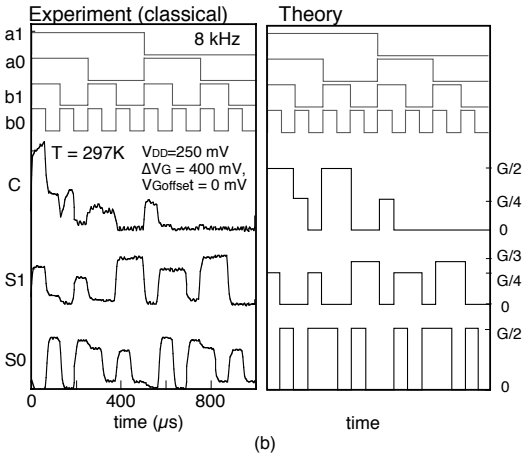
with dashed lines in **Fig. 8**. Other combinational circuits including decoder, encoder, parity generator and checker were also designed using the hexagonal BDD. It was found that BDD circuits require smaller number of devices than those in the CMOS logic gate architecture in most cases. [15] For example, an adder unit in the hexagonal BDD for requires 11 devices, whereas that of a CMOS logic gate-based full adder requires 24 transistors. This also helps for compact implementation.

Typical hexagonal BDD-based subsystems have been successfully fabricated on GaAs-based hexagonal nanowire networks. **Figure 9(a)** shows a fabricated QWR-type 2-bit adder. This circuit integrates 14 node devices using 9 M nodes/cm^2 fabrication process. Its correct operation of this adder circuit was confirmed at RT as shown in **Fig. 9(b)**. In this operation, same input logic swing and offset voltages were given to all node devices. This indicates that device characteristics are fairly uniform. It may be also the case that the hexagonal BDD circuits can operate allow rather wide variations of device parameters for correct operation. **Figure 10** shows a fabricated QWR-type 8-bit adder, where 84 devices are integrated on 74 µm x 19 µm area using a network of 25 M nodes/cm^2 fabrication process.



$c_1 = a_1 \cdot b_1 + a_0 \cdot b_0 \cdot (a_1 + b_1)$
$s_0 = a_0 \oplus b_0$
$s_1 = \overline{a_0} \cdot \overline{b_0} \cdot (a_1 \oplus b_1) + a_0 \cdot b_0 \cdot \overline{(a_1 \oplus b_1)}$

(a)



(b)

Figure 9. (a) SEM image of fabricated hexagonal BDD QWR-type 2-bit adder and (b) input-output waveforms by experimental at RT and theory.

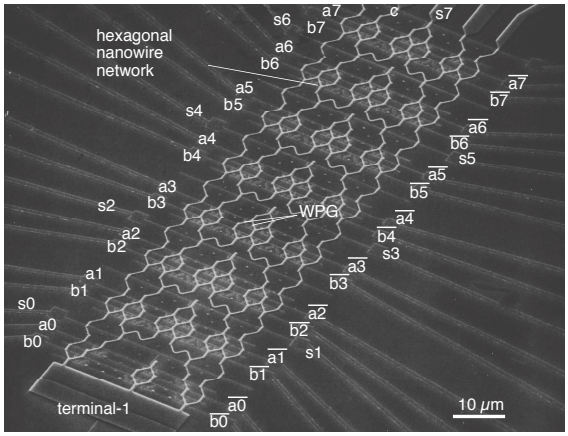


Figure 10. Fabricated hexagonal BDD QWR-type 8-bit adder.

This is the highest scale of device integration so far reported on the quantum nanodevice logic circuits. Large number of BDD devices can be integrated without nanowire crossover. At present, 45 M nodes/cm^2 circuit fabrication process has already been developed.

V. NANOPROCESSOR

A nanoprocessor (NPU) [7,8] that we aim to realize is an ultra-small and ultra-low power processor, featured by 1/1,000x size and power consumption of microprocessors (MPUs). In order to realize the nanoprocessor, we have utilized the hexagonal BDD quantum circuit and III-V semiconductor-based nanowire networks. **Figure 11** shows an NPU system architecture. It has a conventional von Neumann type architecture. Core of the NPU includes arithmetic logic unit (ALU) and controller, indicated by gray areas in **Fig. 11**, are designed with combinational circuits, therefore these components can be designed using the hexagonal BDD quantum circuits. This is expected to result in remarkable reduction of the NPU power consumption. As a first step to the implementation of the NPU, 8-insturction 2-bit ALU has been designed utilizing the hexagonal BDD circuits. A circuit

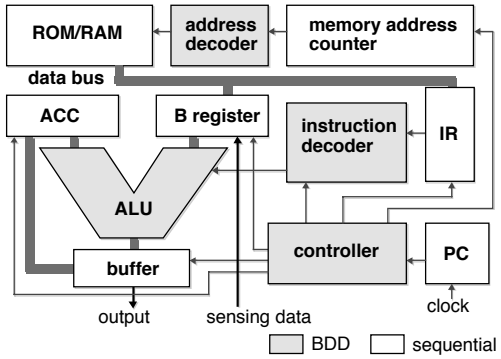


Figure 11. Nanoprocessor system architecture.

diagram of the ALU is shown in **Fig. 12(a)**. It can be successfully designed with hexagonal layout and no nanowire crossover. The ALU consists of eight subsystems for each instruction and combines them with a selector for each bit. This is a simple design and makes it easy to check the logic even in the case when the number of bits and instructions increase. The device count of the hexagonal BDD ALU is 56 whereas the transistor count of a 7-instruction 2-bit CMOS ALU is 144. Smaller device count is effective for reducing both the circuit area and the power consumption. An SEM image of the fabricated QWR-type test ALU structure using 45 M nodes/cm^2 fabrication process is shown in **Fig. 12(b)**. Correct operation of the ALU component was confirmed by circuit simulation as shown in **Fig. 12(c)**.

On the other hand, white components in **Fig. 11** which are registers and counters based on flip-flop (FF) are sequential circuits. It is difficult to implement them using the BDD. Sense amplifiers and level adjusters are also necessary for signal level matching between BDD components or between them and other components. They are also required to operate from low temperature to room temperature as well as to be implemented on hexagonal nanowire networks. To satisfy these requirements, the circuits using WPG-controlled nanowire FETs formed on hexagonal networks have been investigated. As already shown in **Fig. 5(b)**, WPG-controlled nanowires can operate as conventional FETs by overdriving with higher drain voltage. We confirmed that WPG-controlled nanowire FETs have enough transfer gain to compose FFs and amplifiers from fabrication of inverter circuits on a hexagonal nanowire network and their characterization even at room temperature. It is obvious that they can operate also at low temperature. Actually, as shown in **Fig. 13(a)**, a RS-FF circuit was fabricated and correct operation was confirmed experimentally at room temperature. This also confirms that SRAM can be implemented on the hexagonal nanowire networks. Registers by D-FF and counters by T-FF were also successfully designed on hexagonal networks and correct operations were confirmed by simulation as shown in **Fig. 13(b)** for the D-FF as an example, allowing small input voltage swings. Thus, whole NPU system with the hexagonal layout and operating from low temperature to room temperature is possible.

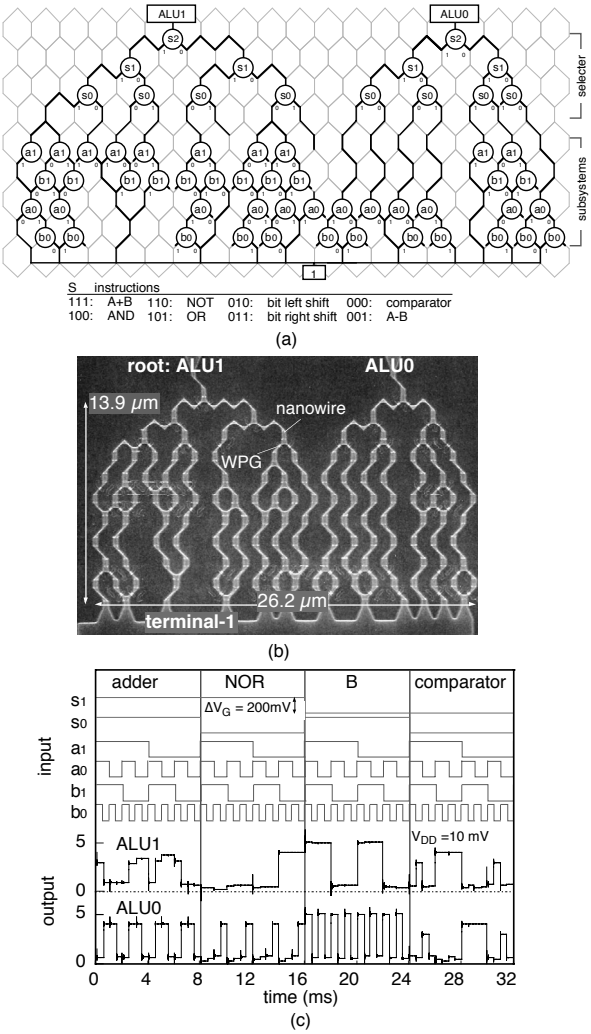


Figure 12 (a) Circuit diagram of hexagonal BDD 8-instruction 2-bit ALU, (b) SEM image for fabricated circuit and (c) input-output waveforms by simulation.

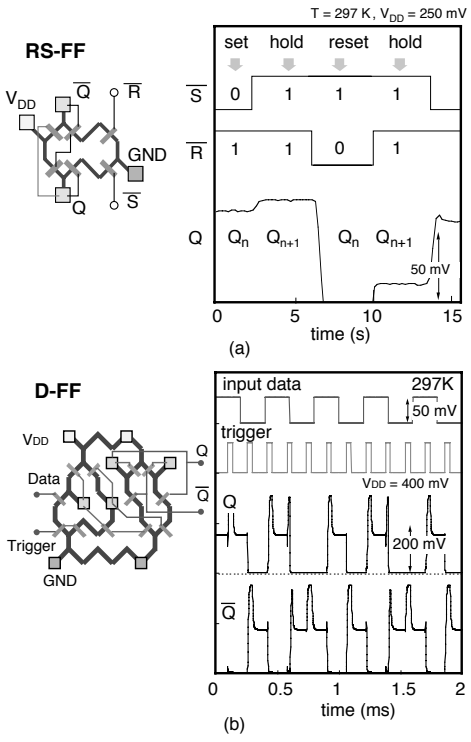


Figure 13 (a) RS-FF design and measured input-output waveforms and (b) D-FF design and input-output ewaveformes by simulation.

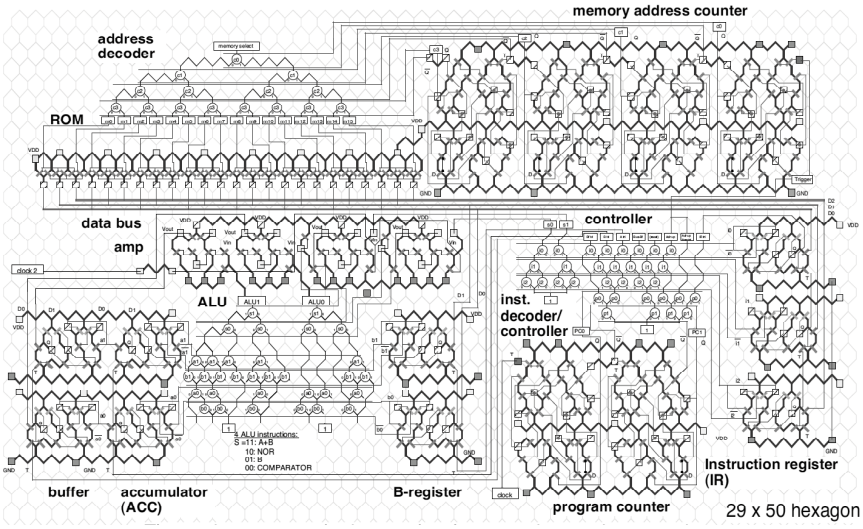


Figure 14. Hexagonal BDD-based 2-bit nanoprocessor layout.

A 2-bit nanoprocessor integrating the components described above was successfully designed as shown in **Fig. 14**. The system area is 29 x 50 hexagons. Whole system was designed with hexagonal layout and no nanowire crossover. Important components of this system including an ALU, decoders and a controller, were designed utilizing the hexagonal BDD circutis. Other components were also arranged on the same hexagonal nanowire network as shown in **Fig. 14**. In this system, eight instructions are implemented. Device count in the NPU is 381, which is much smaller number than that of about 700 transistors in a CMOS-based processor with the same system architecture in **Fig. 11**. The input-output waveforms by the circuit simulation at 1 MHz clock of the 2-bit NPU are shown in **Fig. 15**. The designed NPU system is found to process signals correctly.

Finally, power consumption and system size of the NPUs are estimated and compared with the CMOS-based MPUs. The power consumption, P, was estimated from the simple equation, $P = a \bullet n_d \bullet \mathrm{PDP} \bullet f_{clock}$, where a is activity factor, n_d is device count and f_{clock} is clock frequency. The activity factor was evaluated for each component by counting the number of switching events in the component for typical system instructions and data processing. The average value of a was found to be 0.21. Total power consumption was obtained by summation of power consumptions of each component. In this evaluation, 10 times large supply voltage and logic swing were assumed for the sequential circuits and amplifiers. Then, the power consumption of the hexagonal BDD-based 2-bit NPU utilizing SE-type devices in **Table I** came to only 0.01 nW at 10 MHz clock. The obtained power consumption is 0.01 times smaller than that of the CMOS-based system. In case with smaller design rules, the difference of power consumptions between NPUs and CMOS MPUs will be larger, since the CMOS suffers from static power loss by gate and body leakage currents in devices by the technology node of hp65 or later, which do not appear in our Schottky WPG structure. The analysis of the system also showed that most of the power was consumed in sequential circuits in the present NPU. Further sophisticated design of the system architecture and exploring alternative approaches to implement sequential circuits are thus desirable. On the other hand, when the bit size increases, the NPU system power consumption was found to be dominated in combinational circuits rather than by sequential circuits [8]. The device counts in BDD-based combinational circuits are known to be smaller than those of CMOS logic gate-based ones in general cases [15]. Rough estimate indicates that BDD components dominate the system area and power when the bit size ≥ 4.

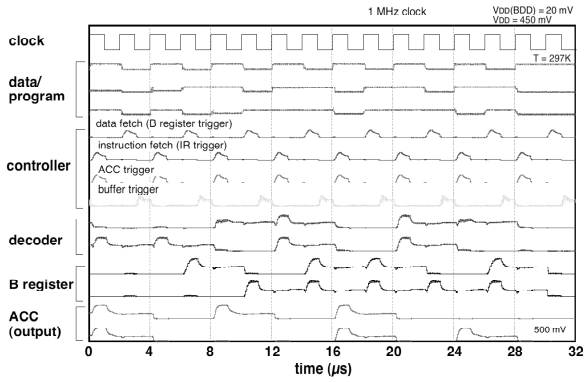


Figure 15. 2-bit NPU operation.

Possible sizes and bench mark of power

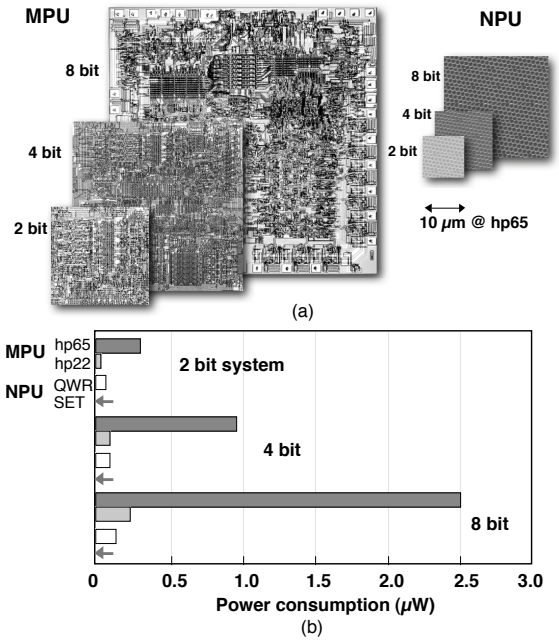


Figure 16. Comparison of (a) size and (b) power consumption between NPUs and MPUs.

consumption of NPUs and MPUs are summarized schematically in **Fig. 16**. In the estimate, a hexagon size is evaluated by $1/(4hp)^2$, where hp is the technology node. Assuming fabrication of the 2-bit NPU using the Si CMOS process technology, the size is expected to be 1/5 smaller than that of the MPU. Combining advanced III-V semiconductor nano-structure fabrication technology [16] and the hexagonal BDD architecture, the NPU will appear in 10 years later by ITRS projection.

Now, our research group has established to form high-density hexagonal nanowire network over 1 Giga nodes/cm^2 by a selective MBE growth technique [16]. New type of path switching devices utilizing electron correlations in single or a-few electron systems in quantum nanostructures have been also intensively investigated [17], which enable to operate with much lower power consumptions in higher temperature.

I. CONCLUSIONS

The novel hexagonal BDD logic quantum circuits and ultra-small-size and ultra-low-power digital logic processor, "nanoprocessor (NPU)", were described. The investigation was carried out utilizing GaAs-based hexagonal nanowire networks controlled by nanometer scale Schottky wrap gates (WPGs). From basic node devices and elementary logic function blocks, fabrication technology of hexagonal BDD quantum circuits with node densities over 45 million nodes/cm^2 has been successfully developed. Their correct operations at low temperatures and room temperature have been confirmed by experiments and simulation. Various subsystems in logic processors, including arithmetic logic unit (ALU), controller and decoders were designed as hexagonal BDD layouts without nanowire crossover. For sequential circuits, WPG-controlled nanowire FETs on hexagonal networks have been investigated, and registers and counters have been implemented, showing correct operation. A hexagonal BDD-based 2-bit nanoprocessor was successfully designed and its correct operation was confirmed by circuit simulation. These results indicate good prospects of NPUs as a core of future ultra-small knowledge vehicles embedded elsewhere.

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