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Hexagonal Binary Decision Diagram Quantum Circuit Approach for Ultra-Low Power III-V Quantum LSIs

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SUMMARY A new approach for ultra-low-power LSIs based on quantum devices is presented and its present status and critical issues are discussed with a brief background review on the semiconductor nanotechnology. It is a hexagonal binary decision diagram (BDD) quantum logic circuit approach suitable for realization of ultra-low-power logic/memory circuits to be used in new applications such as intelligent quantum (IQ) chips embedded in the ubiquitous network environment. The basic concept of the approach, circuit examples showing its feasibility, growth of high density nanostructure networks by molecular beam epitaxy (MBE) for future LSI implementation, and the key processing issues including the device isolation issue are addressed.

key words: *quantum LSI, quantum devices, binary decision diagram (BDD), nanostructure network, intelligent quantum (IQ) chip*

1. Introduction

Revolutionary progress of internet and wireless technology took place in the last ten to twenty years of the 20th century. As a consequence and natural extension of this, a concept of a "ubiquitous network society" is rapidly growing from the beginning of this century where not only human beings but also all sorts of non-human existences on the globe are put into "networks of networks" of various kinds to enhance human activities based on knowledge to hitherto unprecedented levels.

Emergence of such a ubiquitous network society seems to have brought about new directions for device research, although the importance of the Si CMOS devices will still continue along the well-known roadmap [1] based on the scaling law. However, emerging new trends are of "off-roadmap" nature, and include new trends (1) toward nanotechnology and quantum nanoelectronics, (2) toward new materials including Si on Insulators (SOIs), SiGe, SiC, III-V nitrides and other widegap materials such as ZnO, organic semiconductors such as pentacene, carbon nanotubes (CNTs) and DNA and other exotic material, (3) toward sophisticated use of wireless communications for advanced mobile phones, local area networks and radio frequency identification (RFID) tag networks, (4) toward new areas and new functions including nano-chemistry, bio-nano technology and various sensing functions and (5) toward new and unconventional architectures such as neural networks, stochastic schemes and diffusion-reaction architectures. To cope with such new directions of device research covering wider areas of disciplines, new ideas of hardware technologies have to be developed and combined with new ideas of system architectures and software technologies in closely collaborative ways.

Some examples of new class of devices intended for ubiquitous networks and reflecting above trends and being include the smart dusts being developed at University of California at Berkley [2], Si devices for sensor networks developed at Intel Corp. [3], Si μ-chips for RFID networks being developed at Hitachi Ltd. [4] and the intelligent quantum (IQ) chips being developed by author's group at Hokkaido University [5]. The basic concept of the IQ chip is shown in Fig. 1(a) where ultra-small and high-density processors and memories are realized by a new III-V quantum- (Q-) LSI technology and they are combined on chip with capabilities of wireless communication, power supply and sensing. By fully utilizing high performance and small physical sizes of

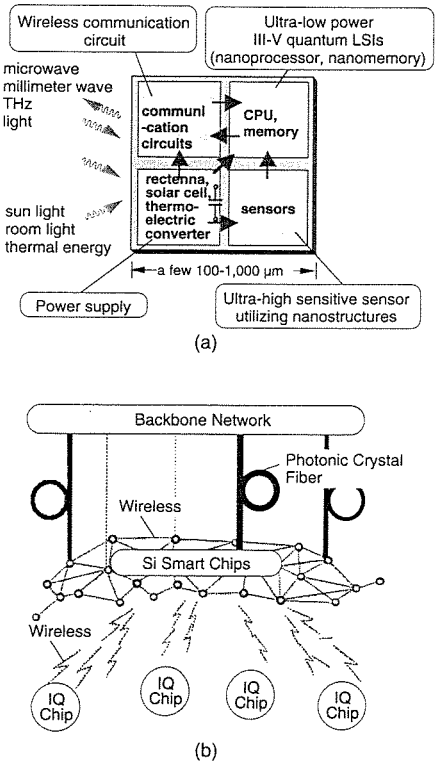

Fig. 1 (a) Basic concept of IQ chip and (b) a ubiquitous meme-media network incorporating IQ chips.

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quantum devices, IQ chips will perform advanced functions of miniature-sized "ubiquitous computers" rather than performing a simple function of identification. An image of a ubiquitous meme-media network incorporating IQ chips is shown in Fig. 1(b). IQ chips are connected to high speed internet backbone networks through Si smart chips produced by the System on Chip (SoC) Si technology. Such a ubiquitous network will enrich the network society of tomorrow in a revolutionary way by embedding IQ chips in all necessary places as miniature knowledge vehicles, and forming ad hoc networks through confederation.

In other words, the development of the IQ chip is an attempt to endow "intelligence" beyond simple identification to RFID chips so that they can be utilized as versatile tiny "knowledge vehicles" in the coming ubiquitous network society. Here, the most serious issue is the power consumption of processors and memories which increases as one tries to endow more and more intelligence into the tiny chip. Use of Si CMOS technology for such purpose is very much limited. To show this, power consumption levels of Intel Si CMOS processors are shown in Fig. 2 vs. the calendar year [6]. It is seen that the power density has remained remarkably constant up to now, being in the range of several W/cm^2, and that it tends to sharply increase towards future. The reason for a constant power density is a natural consequence of the well-known scaling law, and the sharp increase toward future is due to new factors such gate leakage currents by tunneling etc. which are not considered in the scaling law. On the other hand, if one uses on-chip solar cell for power supply, one has to remember that the maximum solar energy is 100 mW/cm^2 under the AM1 condition, and becomes much less after photovoltaic conversion. Energies achievable by small-size rectennas by rectification of rf power are much smaller than the solar energy case [4].

This is the reason why use of quantum devices is considered in the IQ chip. Namely, power consumption of quantum devices can be reduced down to the minimum possible limit allowed by the Heisenberg's uncertainty principle which is still many orders of magnitude smaller than the Si CMOS devices as indicated by a dashed horizontal line in Fig. 2. However, the difficulty is that all of quantum devices proposed up to now still remain at discrete device levels, and there is no well established approach for large scale integration.

The purpose of the present paper is to discuss the present status and key issues of a new approach to build ultra-low power quantum large scale integrated circuits by using III-V quantum devices. It is based on a new hexagonal binary decision diagram (BDD) quantum logic circuit approach. The basic concept, circuit examples to show feasibility of the approach, growth of high density nanostructure networks by molecular beam epitaxy, device isolation issues and the key processing issue are addressed together with some brief overview of semiconductor nanotechnology.

2. A New Approach to Large Scale Integration of III-V Quantum Devices

2.1 Artificial Nanostructures and Quantum Devices

Artificial low dimensional structures such as quantum wires (QWRs) and quantum dots (QDs) having nanometer scale feature sizes comparable to de Broglie wavelengths give rise to novel rich functionalities to materials. This is because quantum confinement in these structures produces artificial quantum state spectra. It also realizes novel radiative and non-radiative state transitions and linear and nonlinear quantum transport phenomena. This has opened up possibilities of various quantum devices and circuits where quantum-mechanical behavior of a single or a few electrons and photons are controlled in various sophisticated ways. Quantum devices so far proposed include quantum wire transistors (QWRTrs), resonant tunneling transistors (RTDs), single electron transistors (SETs) and various spintronic devices. Basic structures of a QWRTr and a SET are shown in Fig. 3(a) in comparison to the classical FET. They are based on quantum transport such as conductance quan-

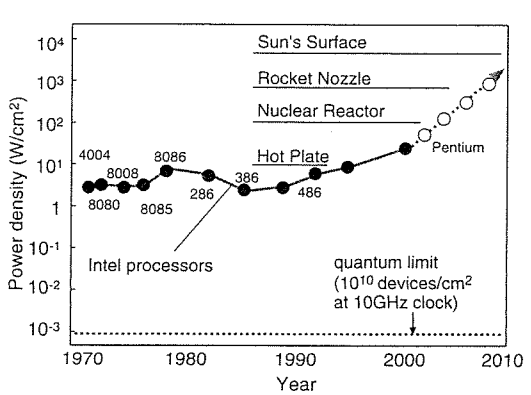

Fig. 2 Power consumption of Intel Si CMOS processors [6]. The power consumption level at the quantum limit obtained by Eq. (2) explained later is shown by the horizontal dashed line for the case of 10^{10} devices/cm^2 with a 10 GHz clock rate.

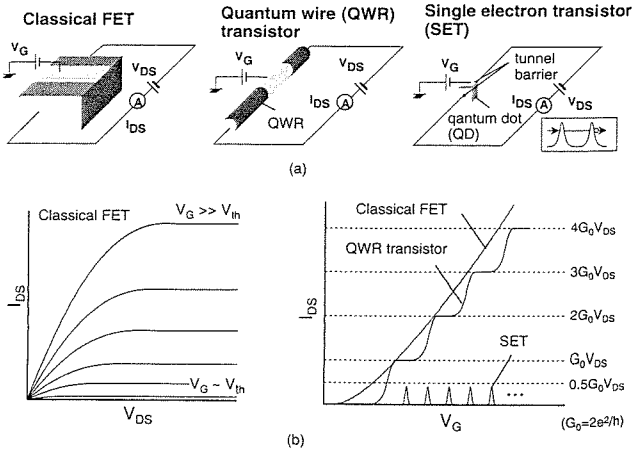

Fig. 3 Basic structures and operations of (a) a classical FET and (b) a QWR transistor and a SET.

tization in a QWR and single electron tunneling in a double barrier structure with a QD. As schematically shown in Fig. 3(b), the drain to source conductance is quantized to an integer multiple of G_o in a QWRTr or limited to periodic peaks with a height of (1/2) G_o as a function of the gate voltage in a SET. Here, G_o is the quantized conductance unit given by

$$G_o = 2e^2/h = 77.481\,\mu\text{S} \tag{1}$$

where h is the Planck's constant. It should be noted that, in this standard notation for G_o, (1/2) G_o is the conductance of one spin-polarized mode of electron transport.

Such quantum devices may play important roles in future information technology (IT) and multi-disciplinary nanotechnology. A specific example is the IQ chip mentioned above. Namely, nanometer scale quantum devices such as QWRTrs and SETs used as "dissipative" switches can realize Boolean logic circuits at smallest possible values of power delay product (PDP) near the quantum limit. This limit is given by

$$\text{PDP} = h/\tau \tag{2}$$

where τ is the switching time. This limit comes from the physical fact that the action (energy multiplied by time) related to switching, where the energy ΔE is dissipated by a single electron within the switching time τ, is quantized by its minimum value of action, h. Use of quantum transport in transport devices provides chances to realize this quantum limit.

In far future, the semiconductor nanotechnology may even realize "non-dissipative" quantum circuits where quantum coherence, extending over entire circuit operation, realizes massively parallel quantum computation and highly sophisticated quantum information processing. As compared with ion traps used for initial demonstration of qu-bit, solid-state forms such as the well-known Si-based nuclear spin computer [7] are much more desirable for realistic implementation. Efforts using coupled quantum wells, coupled QDs and quantum Hall devices are being made to demonstrate basic feasibility of quantum computation. However, substantial progress in the technology as well as in the fundamental computation scheme itself is still required before quantum computation can be practically implemented at sufficiently high qu-bit numbers useful for practical applications. To continue such efforts, success of quantum nanoelectronics based on dissipative switching in a more short-range time scale is desirable.

2.2 A Hexagonal Binary Decision Diagram Quantum Logic Circuit Approach

In spite of the above bright expectations for quantum devices, all of quantum devices proposed up to now still remain at discrete device levels or at very small scales of integration, and there is no well established approach for large scale integration. The major obstacles are 1) lack of a system architecture which is suitable for quantum devices, 2) difficulty of room temperature operation, 3) difficulty of forming position- and size-controlled nanostructures with small feature sizes, and 4) processing difficulty of nanostructure surfaces and interfaces.

Among these, lack of a suitable system architecture seems to be a severest one. Namely, quantum devices have poor current driving capability and poor threshold control due to low-current quantum transport which is extremely structure- and charge-sensitive. Thus, they are totally unsuitable to the "logic gate architecture" most frequently used in Si LSIs. Unless one employs a suitable system architecture, LSIs based on quantum devices seem to be hopeless, and their use will be limited in narrow application areas such as special high-sensitivity sensors, measurement standard devices etc.

To overcome this architecture related difficulty, we have recently proposed a novel hexagonal BDD quantum logic circuit approach [8]–[10] for quantum LSIs (Q-LSIs). The BDD logic architecture itself was originally proposed by Akers [11] in 1978, and has been used as a software tool for logic design on computer. More recently, its hardware implementation in the form of Si CMOS LSIs was proposed and investigated by Yano et al. [12] with favorable conclusions. Use of the BDD architecture in single electron circuits was proposed by Asahi et al. [13] together with its feasibility study on computer. The basic concept of our approach is shown in Fig. 4. Here, gated quantum BDD node devices are formed on a hexagonal planar QWR network. As shown on the right hand side of Fig. 4, each node device selects, according to gate input x_i, one of exit-branches for a single electron or a few electrons coming into the entry branch as the information messenger. Then, the value of the logic function, r_i, is determined by whether the messenger starting from the root terminal for r_i reaches the terminal-1 or to terminal-0 after traveling down the QWR network. It is known that any combinational logic function can be implemented as a BDD circuit. For a large logic system including feedback, the system is divided into fairly large BDD combinational logic blocks with buffer registers so that design can be made at register transfer level.

This approach has following features:

(1) There are no direct output-to-input cascade connections.

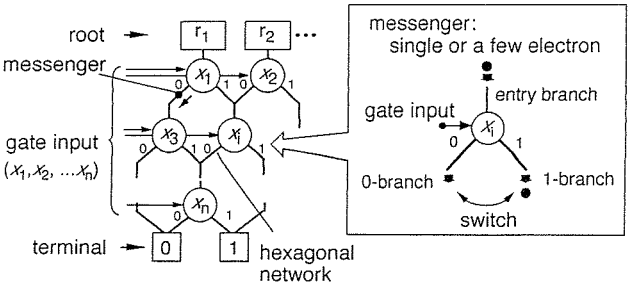

Fig. 4 Basic concept of the hexagonal BDD quantum logic circuit.

(2) A hexagonal close-packed layout is used.
(3) Switching is carried out by gate controlled quantum transport.
(4) Node devices are interconnected by QWRs without source/drain contacts.
(5) Node switches operate as classical switches at high temperatures.

Because of the feature (1), a large voltage gain, precise input-output voltage matching, large fan-in and fan-out numbers, tight threshold control and large current drivability, which are the requirements for Si CMOS transistors, are not required any more. High-density integration is achieved by the feature (2), because the node device has a three-fold symmetry. Very low power operation of the circuit is expected, since each node device realizes the smallest possible PDP values near the quantum limit. The feature (4) avoids the well-known serious contact problem in Si LSIs. Interconnection length and levels are reduced due to absence of cascade connections, use of ungated nanowires as interconnects and regular circuit layouts. Due to the feature (5), BDD circuits operate over a wide temperature range because operation mode continuously changes with temperature from the single electron quantum regime, to a few electron quantum regime, and finally to the many electron classical regime.

2.3 Examples of GaAs-Based Hexagonal BDD Circuits and Speed-Power Performances

The hexagonal BDD quantum logic circuit approach is a general one, being applicable to SOI structures, organic molecular wire networks, carbon nanotubes etc. If fact, quantum wire transistors (QWRTrs) and single electron transistors, based on SOI, III-V and CNT materials, have been demonstrated, at discrete device levels, and they are thus potential candidates for BDD implementation. However, for large scale integration of BDD circuits, the material should allow formation of high density hexagonal networks with nearly ideal quantum transport. Technologies for SOI materials, organic semiconductors and CNTs do not seem to be mature enough to form high density of networks of quantum structures. On the other hand, attempts to form artificial solid-state quantum structures such as QWRs and QDs appeared for the first time in III-V semiconductor research community in late 1980s, and have been intensively continued. III-V nanostructures still seem to remain at the most advanced status of art as compared with other approaches of nanotechnology appeared later. For example, as explained in the next section, the minimum QWR size obtainable by our selective MBE for III-V materials is several nanometers, approaching the size of CNTs. These wires are totally embedded in, and well supported by, the barrier material with superb heterointerfaces, and the resultant structure is still pseudo-planar, being suitable for further metallization by a standard LSI processing. Thus, we believe that the III-V material is the best candidate for the purpose.

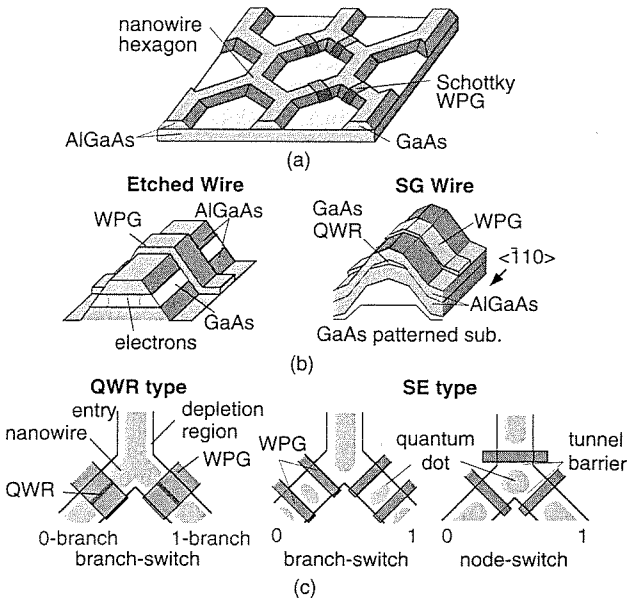

Fig. 5 GaAs-based implementation of BDD quantum node devices. (a) Circuit implementation by hexagonal nanowire network controlled by WPG, (b) basic structure of WPG and (c) WPG-based quantum BDD node devices.

Examples of our GaAs-based implementation of the hexagonal BDD approach are shown in Figs. 5(a)–(c). The circuit is based on nanometer scale Schottky gate control of a hexagonal network as shown in Fig. 5(a). Here, the network can be produced either by electron beam lithography and chemical etching (etched QWRs) or by selectively grown by MBE process as explained in the next section (SG QWRs). For gate control, the Schottky wrap gate (WPG) developed by our group [14] is used as shown in Fig. 5(b) where a short metal gate is wrapped around an etched OWR segment or a selectively grown (SG) QWR segment. It produces a pseudo-planar structure with a tight potential control over the superb AlGaAs/GaAs heterointerface. Three kinds of BDD node devices using this technology are shown in Fig. 5(c). In the first QWRtype device, switching between 0-th and 1st conductance quantization steps is performed in a complementary fashion between left and right branches for path switching at a PDP value near the quantum limit. In the second single electron (SE) type device, two short WPG finger gates on each exit branch produce two tunneling barriers with a QD in between, and the first conductance peak due to single electron resonant tunneling is used again in a complementary fashion between left and right branches for path switching. In the third SE type device, three finger gates produce three tunneling barriers with a QD at the central node point, and switching is carried out in a similar way.

By using GaAs etched QWR networks, QWR-type and SE-type BDD node devices and simple integrated circuits such as AND, OR, XOR, and two-bit and four-bit quantum adders have been successfully fabricated [15]. An SEM photograph of a QWR-type BDD node device and observed

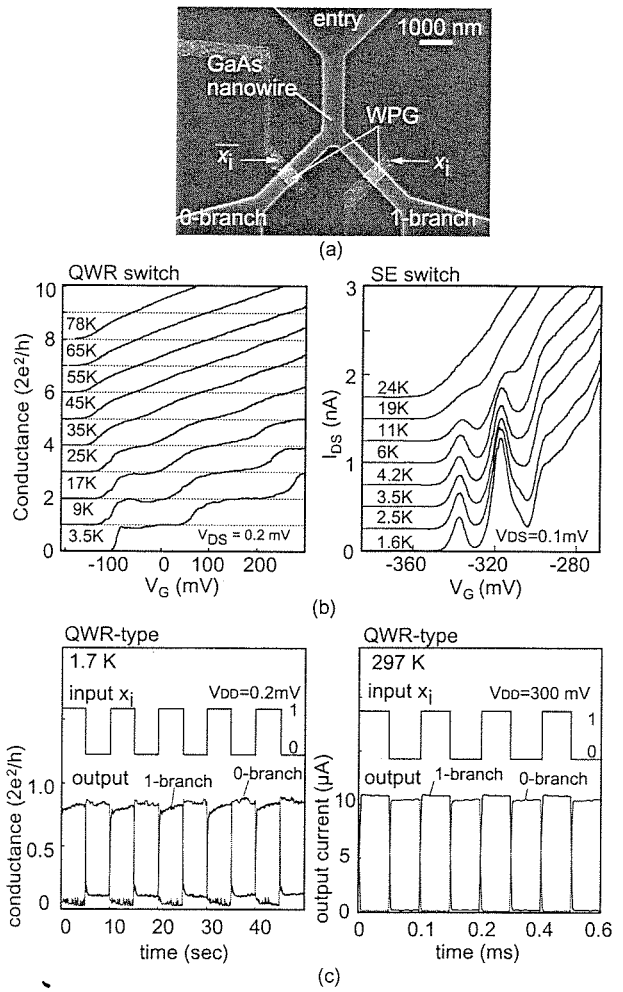

Fig. 6 (a) An SEM photograph of a QWR type BDD node device, (b) observed branch switch behavior of QWR- and SE-type BDD node devices and (c) path switching behavior of QWR-type node device at 1.7 K and room temperature.

branch and path switching behavior of QWR- and SE-type BDD node devices are shown in Figs. 6(a), (b) and (c), respectively. As shown in Fig. 6(b), branches of both types device clearly showed quantum transport behavior. The conductance behavior of the SE-type may look more complex than the simple picture shown in Fig. 3(b). This is because the behavior shown in Fig. 3(b) applies for metal QDs where quantum confinement energy is usually negligible as compared with charging energy due to very short de Broglie wavelengths. In semiconductor QDs, both of charging and quantum confinement energies become comparable, and behavior becomes more complex. A more detailed analysis of conductance peak height and width as a function of temperature has confirmed that the observed peaks seen in Fig. 6(b) are indeed due to single electron resonant tunneling [16]. Data in Fig. 6(c) also shows that fabricated QWR-type BDD node devices show expected path switching behavior not only at low temperatures, but also at room temperature. SE-type BDD node devices also have shown path switching behavior from low temperature up to room temperature. This

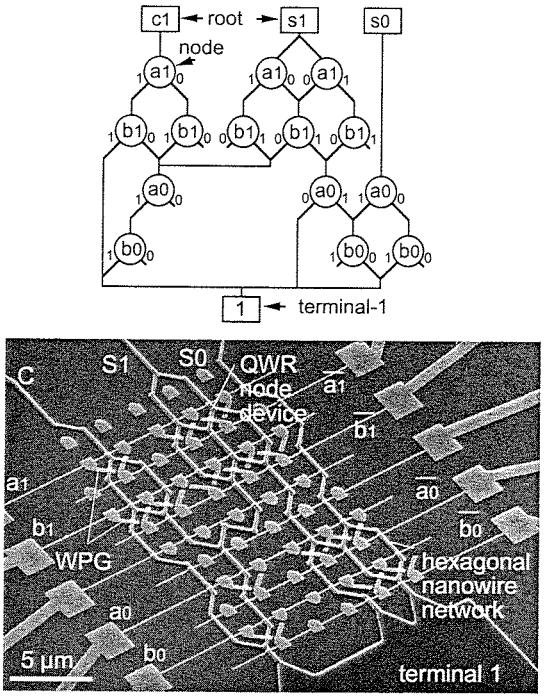

Fig. 7 Fabricated QWR-type BDD 2 bit adder with its circuit diagram.

confirms the feature (5) of the present BDD approach mentioned above. As an example of a small scale integrated circuit, a SEM micrograph of a 2-bit BDD adder using QWR-type node devices is shown in Fig. 7 together with its BDD graph. Here, 14 BDD node devices were integrated and a correct operation was obtained [15]. A circuit diagram and layout of a 2-bit nanoprocessor which we are in the process of fabrication is shown in Fig. 8. Here, the entire circuit is laid out on a hexagonal QWR network with 45×26 hexagons without any wire cross-overs. If the hexagon pitch can be made 100 nm, the total area of the processor will be very small occupying only $4.5 \times 2.6\,\mu m^2$.

The speed and PDP values of the BDD branch switch can be roughly estimated by the following simple equations using the device capacitance, C, and conductance, G.

$$\tau = C/G \tag{3a}$$

and

$$\mathrm{PDP} = C(\Delta V_G)^2 \tag{3b}$$

where ΔV_G is the gate voltage swing required to cause path switching. When $G = (1/2)G_o$ (single mode propagation) and ΔV_G is due to single electron charging, satisfying $C\Delta V_G = e$, Eq. (3b) reduces to the quantum limit given by Eq. (2).

Experimentally, measurement of G is straightforward from the gated I-V characteristics. However, direct measurement of C is rather difficult, since its value is usually small and there is a tendency that it is buried in the stray capacitances. Our approaches to estimate the value of C were the following. In the case of the QWR-type switch, the device capacitance can be estimated by the following formula.

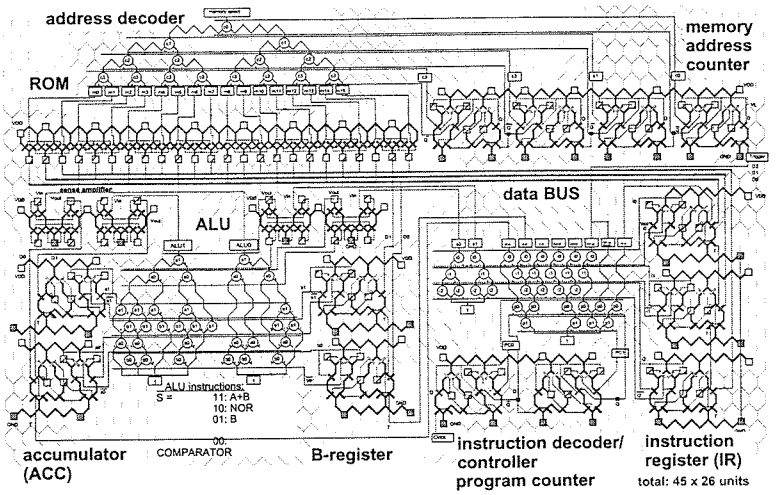

Fig. 8 A circuit diagram and layout of a 2-bit nanoprocessor.

$$C = eL_G\left(\frac{dn_{1D}}{dV_G}\right) \tag{4}$$

where n_{1D} is the line density of electrons in the QWR, and L_G is the WPG length. The value of n_{1D} can be determined by gate-dependent Shubnikov - de Haas (SdH) measurements under application of strong magnetic fields and subsequent analysis of Landau plots, using harmonic potential approximations [17]. In the case of the SE-type device, the effective capacitance can be determined from a Coulomb diamond chart of the switch [10], [18]. Estimates of the switching time, τ along the lines explained here have indicated that GHz clock operation should be possible in both of QWR-type and SE-type devices fabricated on QWR segments with the wire width of several hundred nanometers.

Direct measurement of speed of quantum devices is again not easy, since quantum devices are high impedance devices with small capacitances, and do not fit to 50-ohm measurement systems. To overcome this difficulty, special integrated devices which have many QWR switches in parallel as shown in Fig. 9(a) have been prepared recently, and their switching properties have been measured at room temperature by an Agilent vector network analyzer (8510C) and direct on-chip probing. An example of gain plots for a device with 90 QWRs and $L_G = 110$ nm is shown in Fig. 9(b) which gives $f_T = 2.5$ GHz and $f_{max} = 9$ GHz. It shows that GHz clock operation is possible even in the classical operation mode. The result is expected to improve at low temperatures due to better transport, although such rf-measurements require more sophisticated set-up.

The PDP values estimated using Eq. (3b) are summarized for various QWR- and SE-devices in Table 1 together with the data reported for latest nano-scale Si CMOS devices [19]. As seen in Table 1, PDP values of the present BDD node devices are smaller than those of nano-scale Si CMOS devices, particularly being about 1/10000 of the CMOS device in the case of the SE-type BDD device.

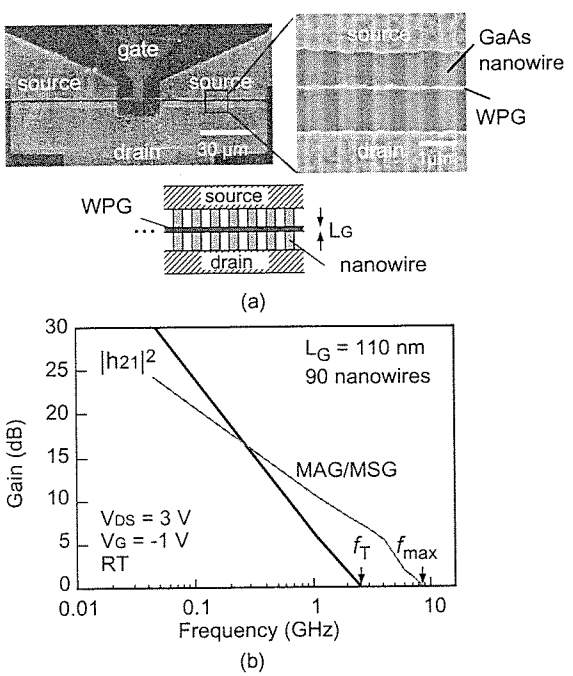

Fig. 9 (a) Special integrated devices which have many QWR switches in parallel and (b) gain plots for a device with 90 QWRs and $L_G = 110$ nm.

Table 1 Estimated PDP values of QWR- and SET-type switches compared with those of the latest Si MOSFET.

	L_G	PDP value
WPG etched QWR switch (1.6 K)	630 nm	10^{-20} J
	65 nm	10^{-21} J
WPG SG QWR switch (1.6 K)	400 nm	10^{-18}J
WPG SET switch (1.6 K)	30 nm	10^{-22} J
Lab. level Si CMOS Tr.(300 K)*	20 nm	10^{-17} J

(SG QWR = selectively grown quantum wire)

3. Preparation of High Density Nanostructure Networks

3.1 Major Approaches for Semiconductor Nanostructure Fabrication

For higher density of integration and operation at room temperature, a suitable semiconductor nanotechnology should be established which allow substantial reduction of the hexagon pitch and QWR width than those achievable by the combination of the electron beam lithography and etching used in the above feasibility study. For this purpose, many approaches are available for nanostructure formation, reflecting recent strong interests in nanotechnology. Major approaches for semiconductor nanostructures include;

(1) Direct Si nanostructure fabrication on silicon or silicon-on-insulator (SOI) wafers by Si ULSI technologies including electron (EB) lithography, dry etching, oxidation etc.
(2) Direct nanostructure fabrication on III-V multi-layer epitaxial wafers by EB lithography and etching.
(3) Use of imprint lithography [20] instead of EB lithography in (1) and (2).
(4) Selective depletion of two-dimensional electron gas (2DEG) in III-V wafers by Schottky split gates.
(5) Selective MBE or MOVPE growth of III-V QWRs and QDs on patterned or masked substrates or on specially prepared templates such as anodized aluminum film.
(6) Self-assembled or self-organized formation of QDs and QWRs by Stranski-Krastanow (S-K) mode in MBE and MOCVD, or by other self-organization mechanisms.
(7) Formation of ultra-fine structures such as Si-dots or carbon nanotubes by CVD processes and various molecular reactions.
(8) Direct fabrication of nanostructures by scanned probe-induced atom manipulation and surface reaction.

These approaches have their own advantages and disadvantages, depending on applications. For integration of quantum transport devices, the method should be capable of forming networks of nanostructures with sufficiently high densities and small enough feature sizes so that quantum effects can be utilized at room temperature at device densities much larger than those of projected Si CMOS densities. Roughly speaking, feature sizes should be reduced down to sub-10 nm range with a pitch of nanostructures also in the nanometer range. Other critical factors include position and size controllability, smooth and defect-free structures and turnaround time of nanostructure fabrication.

Traditionally, III-V quantum transport devices have been made by the above approaches, (2) and (4), using EB lithography and wet chemical etching on MBE/MOCVD 2DEG wafers. In fact, we used the approach (2) for the feasibility study mentioned above. These techniques are simple and straightforward. However, the achievable sizes are rather large, giving feature sizes of several ten to several hundred nm. Furthermore, lithography size fluctuation directly affects geometrical uniformity. Another well-known approach (6) of S-K mode growth of QDs provides smallest feature sizes and highest densities for III-V materials within very short turnaround times. It gave impressive results for QD laser applications. However, for transport devices, control of position and size, as well as the method of post-growth wiring, remain to be difficult problems. The scanned probe approach (8) provides the highest spatial resolution in atomic scale. However, turnaround time is too long. From such considerations, the approach (6) of selective MBE or MOVPE growth of III-V QWRs and QDs on patterned or masked substrates [21]–[25] seems to be best suited for the present purpose.

3.2 Selective MBE Growth of High Density Quantum Wire Networks

From the reasons mentioned above, we have decided to employ the selective MBE growth on pre-patterned substrates [22]–[24] for denser networks. As compared with other approaches, this approach has the following advantages;

(1) Sizes smaller than lithography sizes can be achieved.
(2) Nanostructure boundaries are defined by crystalline facets and independent of lithography fluctuations.
(3) Position and size are controlled.
(4) Interfaces are defect-free high quality hetero-interfaces with steep and high potential barriers.
(5) Growth process is compatible with UHV-based processing and characterization.

The basic principle of our selective MBE approach is shown in Figs. 10(a)–(c). Patterns consisting of mesa stripes with suitable orientations and side facets are formed by EB lithography and etching, as shown in Fig. 10(a). So far

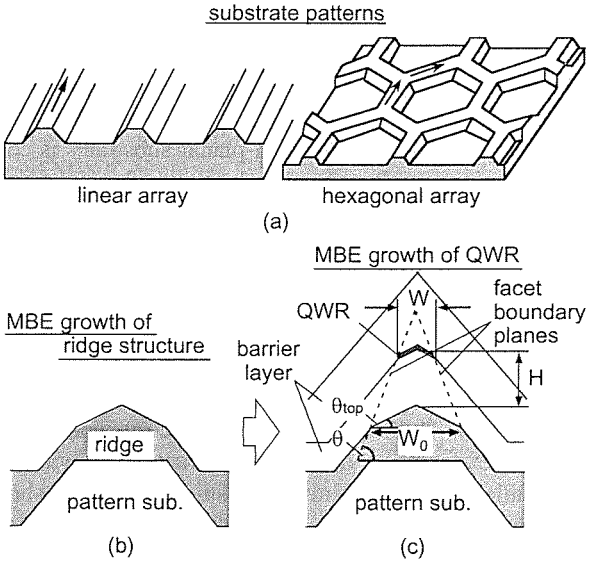

Fig. 10 Basic principle of selective MBE approach for growth of quantum wire networks.

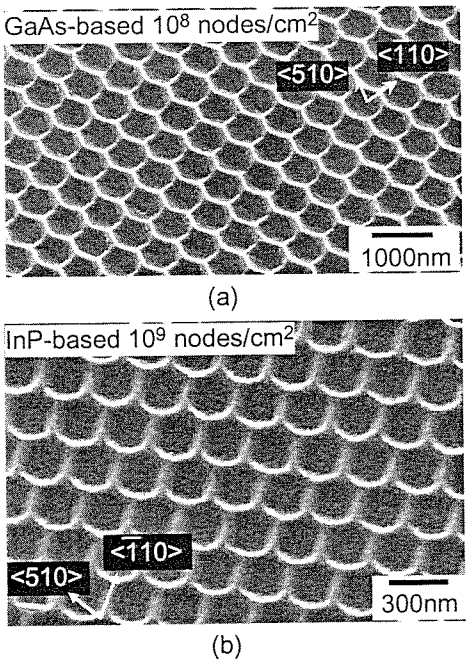

Fig. 11 Examples of high density of QWR networks by selective MBE growth.

(001) and (111)B GaAs, (001) InP and (0001) GaN substrates have been used. After cleaning and removal of surface oxide, ridge structures are grown by MBE on mesa-stripes as shown in Fig. 10(b). For pre-growth oxide removal [26] as well as during ridge growth, irradiation of atomic hydrogen (H*) [27] has been found extremely powerful in improving the facet morphology and uniformity of the ridge structures. Then, by growing a triple-layered structure on the ridge structures by MBE, embedded nanowires with an arrow-headed or flat-top wire cross-section shown in Fig. 10(c) are formed in a self organized way due to built-in selective growth mechanism. GaAs and InGaAs wire arrays thus grown show intense and narrow photoluminescence (PL) peaks with a very large blue shift of several hundred meV [26].

In spite of apparent simplicity of the growth method, the actual growth process on non-planar substrates is complicated due to simultaneous involvement of various high-index facets and related kinetic processes. Thus, proper understanding of the growth mechanism is required for precise control of the shape, feature size and density of nanostructures. A detailed study [28] has shown that the boundaries of two neighboring facets on both sides of the QWR form two continuous facet boundary planes within the barrier layer crystal as schematically shown in Fig. 10. Surprisingly, these boundary planes do not correspond to any of high index facets. A detailed experimental study as well as a detailed computer simulation study [29] have shown that their evolution is the result of difference in the migration and the atom incorporation rates between two neighboring facets. The lateral wire width, W, and the vertical wire height, H, are given by following equations referring to Fig. 10(c).

$$\frac{W}{W_0} = 1 - \beta \cdot t, \quad \beta = 2\frac{g_{top}}{W_0(\tan\theta - \tan\theta_{top})} \tag{5a}$$

$$H = g_{top}t \tag{5b}$$

where g_{top} is the vertical growth rate of the top facet and t is the growth time. Based on this understanding, the position and size of the present QWR can now be kinetically controlled precisely down to sub-10 nm region. Examples of GaAs-based and InP-based high density hexagonal nanowire networks grown by selective MBE are given in Figs. 11(a) and (b), respectively, where hexagonal node densities in the range of 10^9 per cm^2 have been achieved [30]. Node densities of nanostructures achieved by MBE/MOVPE selective growth approaches are plotted vs. calendar year in Fig. 12, and compared with reported Si CMOS transistor densities in Intel processors [31].

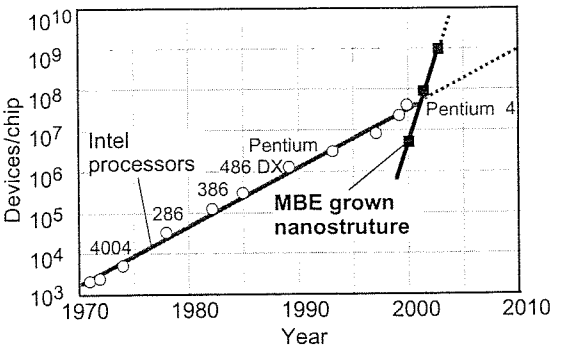

Fig. 12 Node densities of nanostructures achieved by selective MBE growth approach compared with reported Si CMOS transistor densities in Intel processors [31].

4. Key Processing Issues

4.1 Control of Nanostructure Surfaces

In many of quantum devices including our BDD node devices, nano-scale Schottky gates are used to control quantum confinements and quantum transport. It has been found recently [32] that current transport and depletion width control in such contacts are very much affected by Fermi level pinning on the surrounding free surfaces. Particularly, under reverse bias, depletion width becomes deeper and its change with bias becomes less efficient due to depletion in the surrounding region. Examples of calculation are shown in Figs. 13(a) and (b) for the cases of strongly pinned and unpinned surfaces, respectively. Characteristics are totally different between two cases, and the gate on the pinned surface shows only small variations of depletion layer edge with bias. The expected adverse effects of surface states and Fermi level pinning include the following:

(1) Gate control characteristics of quantum devices become much poorer.
(2) Strong Fermi level pinning tends to deplete all the near-surface nanostructures, even if they are ungated.

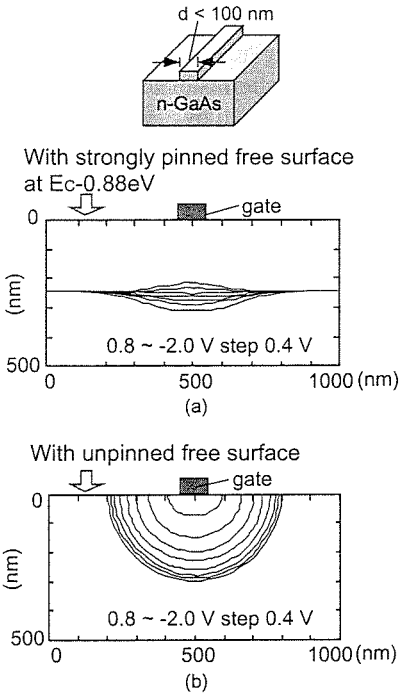

Fig. 13 Gate voltage of depletion layer edge in nano-scale Schottky gates for unpinned and completely pinned cases.

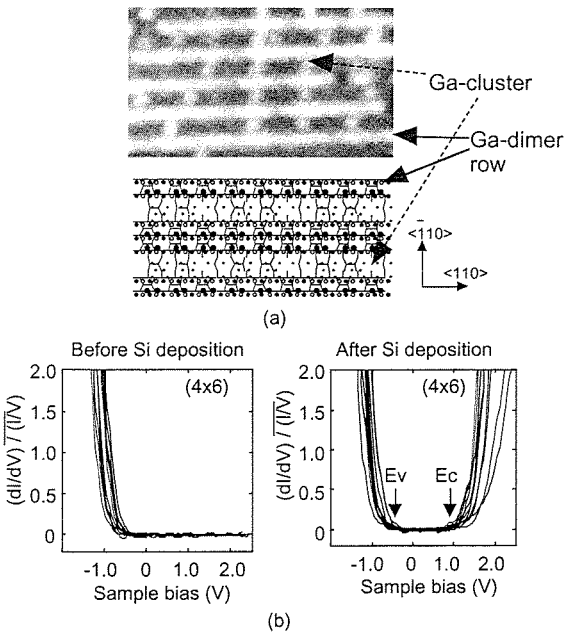

Fig. 14 (a) Filled state STM image taken on (4 × 6) reconstructed GaAs (001) surface and (b) STS spectra of the GaAs surfaces before and after deposition of a monolayer level Si layer.

(3) Electron exchange between quantum confined states of near-surface nanostructures and surface states hinders device operation, generates surface off-set charge and raises reliability issues.
(4) Charged surface states near the metal electrode periphery enhance edge fields and cause surface leakage current by tunneling injection of electrons.

These problems become severer and severer as the gate dimension is reduced. However, removal of surface states in III-V materials is a well known difficult problem, and even on MBE-grown clean III-V surfaces, Fermi level is usually firmly pinned near a characteristic energy due to high density surface states except for carefully cleaved (110) surfaces. In order to overcome this problem, we have been making intensive efforts to understand and control surface states on (001)-oriented GaAs, InP and GaN, using various techniques including UHV STM/STS, contactless C-V, PL and XPS techniques.

Traditionally, As-stabilized GaAs (001) surfaces, either by MBE or by MOVPE, have been technologically most important ones for initiation of device processing, and not much attention has been paid to Ga-rich surfaces. Here, an example of the filled state STM image recently taken on (4 × 6) reconstructed (001) surface is shown in Fig. 14(a). The STS spectra of the same surface are shown in Fig. 14(b) without and with deposition of monolayer level Si layer. Without Si, the spectra shows an anomalously large conductance gap rather than showing GaAs band gap as expected. Similar phenomena were observed in the past on (2 × 4) and c(4 × 4) reconstructed (001) surfaces of GaAs. We explained this anomaly in terms of tip-induced localized charging of surface states [33].

On the other hand, deposition of one ML of Si led to appearance of normal STS conductance gaps [34] as also shown in Fig. 14(b). Here, the ML level Si is transparent in STS measurements since its effective band gap is much larger than that of GaAs due to strain. Similarly, a cubic GaN ICL formed by direct nitridation of GaAs [35] was found to be effective. It was also found that formation of Si ICL and GaN ICL on Ga-rich (4 × 6) surface is much more effective than that on the traditionally As-rich (2 × 4) and c(4 × 4) surfaces in reducing surface states. We believe that this is due to the fact that termination by non-volatile Ga atoms is more ordered and more robust than As-stabilized surfaces. Metal-insulator-semiconductor (MIS) structures having Si and GaN ICLs between GaAs and an outer Si based dielectric film showed complete unpinning of the Fermi level over the entire band gap according to measured MIS C-V curves [35].

4.2 Device Isolation Issue

One of specific processing related critical issues for large scale integration of quantum devices which none of previous studies has addressed so far, is the device isolation issue related to possible interference between two neighboring quantum devices which limits the achievable packing density.

In order to study the device isolation behavior of GaAs QWR-type BDD switches, QWR transistor test structures having a Schottky wrap gate and a Schottky side gate were fabricated by EB lithography and wet chemical etching [36], [37]. The structure of the device is shown in Fig. 15.

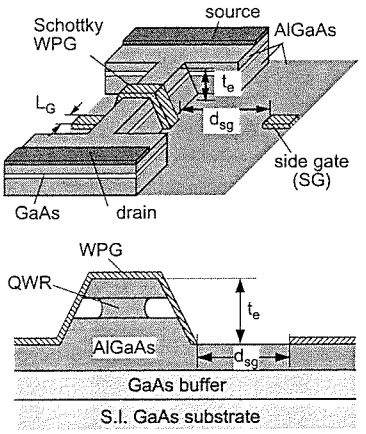

Fig. 15 Test device structure for side gating study.

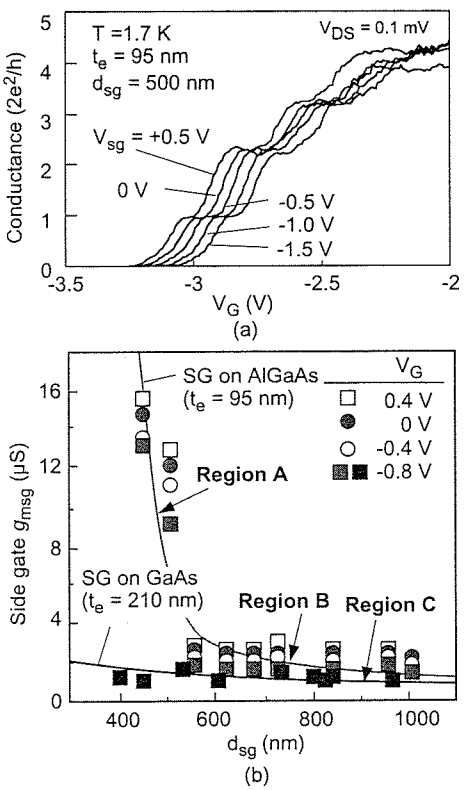

Fig. 16 (a) Side gate effect in quantum regime at low temperature and (b) side gate transconductance as a function of d_{sg}.

Important parameters for the experiment were the distance, d_{sg}, between the side gate and the QWR and the mesa etching depth for device isolation, t_e, as indicated in Fig. 15.

The devices showed clear conductance quantization at low temperatures, as shown in Fig. 16(a). It was also observed that gate voltage values for conductance steps shifted with the side gate voltage. Thus, side gating takes place in the QWR transistors.

In order to understand the mechanism of side gating, detailed study was carried out in the large amplitude FET mode operation of the QWR transistor over a wide temperature range of 1.6–300 K. Devices showed different side gating behavior, depending on the values of t_e and d_{sg}, as summarized in Fig. 16(b) in terms of the side gate transconductance, g_{msg}, which is defined by

$$g_{msg} = dI_{ds}/dV_{sg} \quad (V_g, V_{ds} = \text{const.}) \tag{6}$$

Here I_{ds}, V_{ds}, V_g and V_{gs} are the drain current, drain voltage, gate voltage and side gate voltage, respectively. There exist three Regions A, B and C of side gating characteristics. Region A, observed only on the side gate formed on the AlGaAs surface, exhibited anomalously large side gating with a strong d_{sg}-dependence. On the *I-V* curves, the side gate in Region A acted almost like the main gate, causing current reduction and pinch-off. On the other hand, Regions B and C exhibited weaker and weakly d_{sg}-dependent side gating. On *I-V* curves, side gating caused weak shits of threshold voltage.

By a detailed computer analysis of potential distribution, using our SOR analysis program, the observed weak side gating in Regions B and C could be explained quantitatively in terms of electrostatic sideway depletion into the lower barrier region of the device which weakly modulates the potential from underneath of the quantum wire. However, such a model could not explain the large side-gating in Region A. It was found that the relevant mechanism is related to the adverse effect of surface states (4) mentioned above. Namely, strong Fermi level pinning near the side gate edge produce leakage current by the tunneling mechanism, when d_{sg} becomes small, and this leakage current flows into the quantum wire, modulating the occupancy of traps in the AlGaAs lower barrier, and leading to large side-gating. In Region C with side gate on GaAs surface, leakage current flows, but it does not flow into the quantum wire due to presence of GaAs/AlGaAs heterointerface barrier.

Thus, side-gating can be suppressed by suitable design of device structure and careful control of surfaces.

5. Conclusion

A new hexagonal binary decision diagram (BDD) quantum logic circuit approach for ultra-low-power LSIs based on III-V quantum devices is presented and its present status and critical issues are discussed with a brief background review on the semiconductor nanotechnology. Such an approach seems to be suitable for realization of ultra-low-power logic/memory circuits to be used in new applications such as intelligent quantum (IQ) chips embedded in the ubiquitous network environment. On the basis of the advantageous features of the approach, circuit examples demonstrating feasibility of the approach and successful growth of high density nanostructure networks by selective MBE process, it can be concluded that the approach is a very promising one, and provides a realistic hope for future quantum LSIs for the first time. The obvious next key step is to construct larger BDD circuits on MBE-grown nanowire networks with reduced QWR sizes and hexagon pitches where the key processing issue of control of nanostructure surface

for better gate control and better device isolation will become more and more important. A promising approach for surface control was also mentioned, and it may turn out to be a key technology there.

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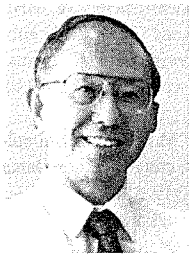

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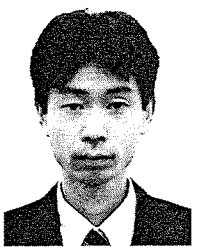

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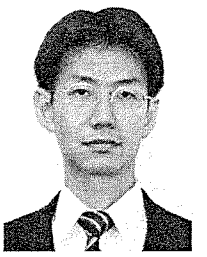

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