Carrier pocket engineering applied to ''strained'' Si/Ge superlattices to design useful thermoelectric materials

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(Received 26 July 1999; accepted for publication 19 August 1999)

The concept of carrier pocket engineering is applied to strained Si/Ge superlattices to obtain a large thermoelectric figure of merit ZT. In this system, the effect of the lattice strain at the Si/Ge interfaces provides another degree of freedom to control the conduction band structure of the superlattice. We explore various geometries and structures to optimize ZT for the whole three-dimensional superlattice. The resultant ZT, calculated for a symmetrized Si(20 Å)/Ge(20 Å) superlattice grown on a (111) oriented $Si_{0.5}Ge_{0.5}$ substrate, is 0.96 at 300 K and is shown to increase significantly at elevated temperatures. Such a superlattice can be grown using molecular beam epitaxy. © *1999 American Institute of Physics.* [S0003-6951(99)04042-5]

The use of low-dimensional structures, as realized in the form of two-dimensional (2D) quantum wells[1–13] and one-dimensional (1D) quantum wires,[14–18] has been shown to provide a promising strategy for designing materials with a large thermoelectric figure of merit ZT. The original proposal that a large enhancement in ZT should be possible in reduced dimensionalities used a simple model for isolated systems.[1,14] Although this is a reasonable model for quantum wire arrays embedded in a porous almina template[16–18] and multiple quantum wells (MQWs) with very thick and/or infinitely high (potential) barriers,[3–6] revision of the model is needed to describe the thermoelectric properties of other quasi-two-dimensional systems, such as MQWs with finite barrier heights and thicknesses, including the effect of tunneling of the carriers through the barrier layers and of parasitic thermal conduction in the barrier layers.[3–13] It is these latter systems that are currently of interest for actual thermoelectric applications.

Recently, the thermoelectric properties of short period GaAs/AlAs superlattices (SLs) have been calculated, first considering only the coupling of the Γ point valley between the well and the barrier layers, and then also considering the contributions from the X and L valleys in the Brillouin zone (BZ).[12] It was shown that ZT for the whole SL, including the contributions from the X and L valleys, could be about 50 times higher than that for the corresponding bulk GaAs, if the geometry and structure of the SLs are carefully engineered so that both GaAs and AlAs layers can contribute to the thermoelectric transport. We refer to such a design process as ''carrier pocket engineering.'' [12]

In the present letter, it is shown that the concept of carrier pocket engineering yields even better results for the Si/Ge SL. The reasons to study the thermoelectric properties of Si/Ge SLs include: (1) Si and Ge have a large number of conduction band valleys (six and four at the Δ and L points in the BZ, respectively), (2) the SiGe alloy is already a good thermoelectric material, (3) the reduction of the lattice thermal conductivity κ_{ph} due to interface scattering of phonons has been studied extensively,[19] and (4) the effect of lattice strain due to lattice mismatch at the Si/Ge interfaces[20,21] provides additional control over the conduction band structure of the SL as discussed below. The general scheme of our theoretical modeling has been described elsewhere.[12] Briefly, the density of electronic states (DOS) is calculated for various high symmetry valleys in the BZ (L and Δ points in the present work) using the Krönig–Penney model[22] and the band parameters listed in Table I. Using this DOS and the constant relaxation time approximation, various thermoelectric transport coefficients are then calculated. In this letter, we first discuss the effect of uniaxial strain on the energy of the Δ and L point valleys in Si and Ge, and then how to incorporate this effect in our model.

While uniaxial strain along the (001) direction, as is realized in the (001) oriented Si/Ge superlattices, has no effect on the position of the L-point valley extrema, it leads to a splitting of the conduction band minima at the Δ point in the BZ (called the Δ valleys) that are degenerate in the absence

TABLE I. Parameters used for Si/Ge superlattices.

Band Parameter	Si	Ge
a_0 (Å)[a]	5.4307	5.6579
m_t/m[a]	0.19	0.082
m_l/m[a]	0.92	1.59
Ξ_u^{Δ} (eV)[b]	9.16	9.42
Ξ_u^{L} (eV)[b]	16.14	15.13
μ ($cm^2/V\,s$)[c]	1350	3600
κ_{ph} (W/m K)[d]	7.3	
ΔE_c^{Si-Ge} (eV)[e]	0.25	

[a]Data taken from Ref. 23.
[b]Data taken from Ref. 21.
[c]Bulk carrier mobilities at 300 K from Ref. 23.
[d]Conservative estimate for the lattice thermal conductivity for the Si/Ge superlattice used in the present calculation. The experimental values found in the literature are somewhat smaller than this value (see Ref. 19).
[e]Conduction band offset between the average position for Si Δ valleys and the average position for Ge L valleys. The literature values for ΔE_c^{Si-Ge} are between 0.15 and 0.35 eV (Ref. 20) depending on the hydrostatic component of the strain in the superlattice.

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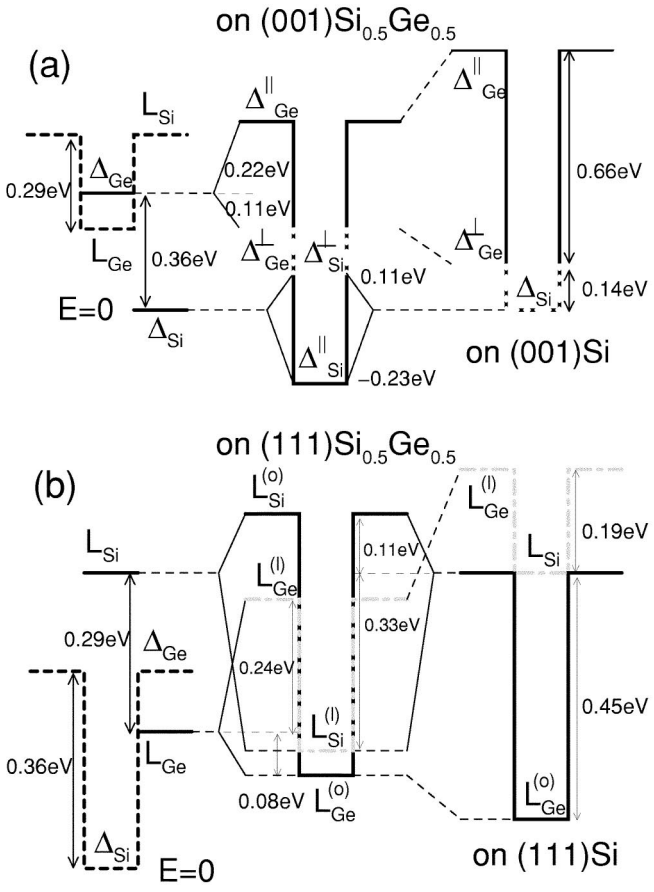

FIG. 1. Conduction band offset diagrams for (a) (001) and (b) (111) oriented Si/Ge superlattices. The band offsets formed at the Δ^{001} and $\Delta^{100,010}$ valleys (denoted by $\Delta^{\|}$ and $\Delta^{\perp}$, respectively) and at the L^{111} and $L^{\bar{1}\bar{1}\bar{1},1\bar{1}\bar{1},\bar{1}1\bar{1}}$ valleys (denoted by $L^{(l)}$ and $L^{(o)}$, respectively) are shown by the black solid and the gray dash-dotted lines in (a) and (b), respectively. The left, middle, and right diagrams denote the band offsets for the unstrained layers, for a superlattice grown on a $Si_{0.5}Ge_{0.5}$ substrate, and for a superlattice grown on a Si substrate, respectively. The band offsets at L and Δ are also shown by the black dashed lines in the left diagrams of (a) and (b), respectively, for comparison.

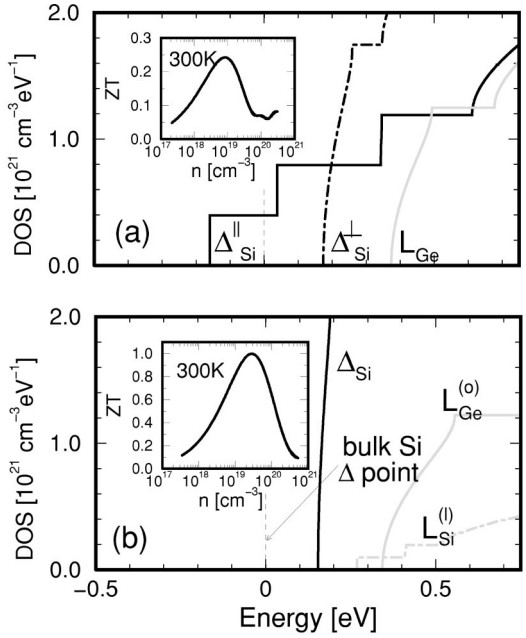

FIG. 2. Calculated density of electronic states for (a) the symmetrized (001) oriented Si(20 Å)/Ge(20 Å) superlattice and (b) the symmetrized (111) oriented Si(15 Å)/Ge(20 Å) superlattice as a function of energy relative to the Δ point of the unstrained bulk Si. The valleys from which the pertinent subband is derived are indicated using the same notation as in Fig. 1. The calculated ZTs as a function of carrier concentration are shown in the insets.

of strain.[21] The magnitudes of these splittings are given by $\Delta E_c^{001}=\frac{2}{3}\Xi_u^{\Delta}(\epsilon_{\perp}-\epsilon_{\|})$ and $\Delta E_c^{100,010}=-\frac{1}{3}\Xi_u^{\Delta}(\epsilon_{\perp}-\epsilon_{\|})$, where the superscripts to ΔE_c denote the alignment direction for the pertinent valley, Ξ_u^{Δ} is the strain deformation potential for the Δ valley (likewise, the notation Ξ_u^{L} is used to denote the L valley), and $\epsilon_{\perp}$ ($\epsilon_{\|}$) is the component for the lattice strain tensor perpendicular (parallel) to the interface. Similarly, under uniaxial strain along the (111) direction, as is realized in (111) oriented Si/Ge superlattices, the energy of the Δ point valleys is not affected, while the energy of the L-point valleys splits according to $\Delta E_c^{111}=\frac{2}{3}\Xi_u^{L}(\epsilon_{\perp}-\epsilon_{\|})$ and $\Delta E_c^{\bar{1}\bar{1}\bar{1},1\bar{1}\bar{1},\bar{1}1\bar{1}}=-\frac{2}{9}\Xi_u^{L}(\epsilon_{\perp}-\epsilon_{\|})$.[21] The values for $\epsilon_{\perp}$ and $\epsilon_{\|}$ are calculated assuming that the lateral lattice constant ($\|$ to the interfaces) for the strained layer is equal to that of the substrate, where a linear interpolation scheme is utilized to determine the lattice constant of the SiGe alloy.

Shown in Fig. 1(a) is the effect of the uniaxial lattice strain on the position of the Δ valley minima calculated for the (001) oriented Si/Ge superlattices grown on (001) $Si_{0.5}Ge_{0.5}$ and on (001) Si substrates. When the SL is grown on a (001) $Si_{0.5}Ge_{0.5}$ substrate, the Si and Ge layers experience tensile and compressive stresses, respectively. Therefore, the energy for the Ge (Si) Δ^{001} valley is shifted upward (downward) and the Ge (Si) $\Delta^{100,010}$ valley is shifted downward (upward), which makes the effective barrier height larger (smaller) for the quantum well derived from the Δ^{001} ($\Delta^{100,010}$) valley. Here, the superscript on Δ denotes the orientation along which the pertinent valley is aligned. The resulting DOS for electrons, shown in Fig. 2(a), is calculated for a (001) oriented Si(20 Å)/Ge(20 Å) SL grown on a (001) $Si_{0.5}Ge_{0.5}$ substrate, where the thicknesses for the Si and Ge layers (20 Å) are chosen so that the resulting ZT is maximized. It is noted that the quantum wells for the Δ and L valleys are formed in the Si and Ge layers, respectively. Therefore, there is a possibility for realization of the carrier pocket engineering concept for the (001) Si/Ge superlattice. However, for this particular case, L-point carriers make a negligible contribution to the transport, because the energy for the L-point subband edge is very high ($\sim$200 mV) relative to the $\Delta^{100,010}$ subband edge. The resultant ZT calculated with this superlattice structure is $Z_{3D}T$ 0.24 at 300 K, which is rather small, although much larger than the corresponding ZT for bulk Si ($ZT=0.014$ at 300 K).

We propose the following two approaches that can be used to increase ZT even further for the Si/Ge SLs. The first method is to grow the SL on a (001) Si substrate so that the effective barrier height for the quantum wells derived from the Δ^{001} valley will be larger due to the compressive stress on the Ge layer [see the right hand diagram in Fig. 1(a)]. Under these circumstances, the Δ^{001} ($\Delta^{100,010}$) valley in the Ge layer is shifted to higher (lower) energy because of the uniaxial strain along the (001) direction, while the Si Δ valleys remain degenerate, since the Si layer is unstrained. The calculation of the DOS for a Si(20 Å)/Ge(20 Å) SL grown on a (001) Si substrate shows that the subband levels associated with the Δ^{001} valley and the $\Delta^{100,010}$ valleys, respectively,

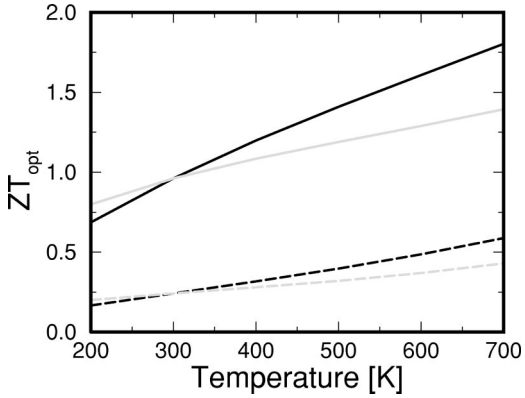

FIG. 3. Calculated values for ZT at the optimum doping conditions for the symmetrized (001) and (111) oriented Si(20 Å)/Ge(20 Å) superlattices (denoted by the dashed and solid curves, respectively). The T dependence of μ/κ_{ph} is taken to be $T^{-1.5}$ (gray curves) and T^{-1} (black curves).

stay very close to each other in energy, because the large effective mass along the (001) direction (confinement direction) for the Δ^{001} valley is compensated by the large barrier height of the quantum wells. The resulting ZT calculated for this SL is 0.78 at 300 K, which represents more than a factor of three enhancement relative to the corresponding ZT for the SL grown on a (001) $Si_{0.5}Ge_{0.5}$ substrate. One drawback for this SL design is that the SL is not symmetrized, i.e., the lattice constant for the completely relaxed Si(20 Å)/Ge(20 Å) SL is different from that for the substrate (Si in this case). Thus, the Si(20 Å)/Ge(20 Å) SL can be grown on (001) Si only up to a certain critical thickness before a large number of crystalline defects and dislocations are introduced.

The second method proposed to increase $Z_{3D}T$ for the Si/Ge SL is to grow the SL in the (111) direction [see the middle diagram in Fig. 1(b)]. For a SL grown in this direction, the subbands derived from the Δ valleys of Si and Ge remain degenerate due to symmetry. The resulting ZT for the (111) oriented Si(15 Å)/Ge(20 Å) SL grown on (111) $Si_{0.5}Ge_{0.5}$ is calculated to be 0.98 at 300 K [see Fig. 2(b)], which is a factor of four enhancement relative to the ZT calculated for the (001) oriented Si(20 Å)/Ge(20 Å) SL grown on (001) $Si_{0.5}Ge_{0.5}$. Even a larger ZT is expected if the superlattice is designed such that the subbands derived from the Δ valley and the $L^{1\,11,111,11\,1}$ valleys stay very close to each other in energy. This situation is conceptually realized by growing a Si(15 Å)/Ge(40 Å) SL on (111) oriented Si [see the right hand diagram in Fig. 1(b)]. Since the Ge layers in this SL are compressively strained while the Si layer is unstrained, only the Ge L-point valleys are split into a L^{111} valley (higher in energy) and $L^{1\,11,111,11\,1}$ valleys (lower in energy). The resulting ZT calculated for this structure is 1.25, which is a factor of five enhancement relative to the ZT for the Si(20 Å)/Ge(20 Å) SL grown on (001) $Si_{0.5}Ge_{0.5}$. It should be noted that the growth of such a nonsymmetrized SL is not yet possible with current MBE technology, and awaits future developments in material science.

It is of practical interest to see how ZT increases as the temperature is increased. Shown in Fig. 3 is the calculated ZT as a function of temperature for the symmetrized (001) oriented Si(20 Å)/Ge(20 Å) SL grown on (001) $Si_{0.5}Ge_{0.5}$ as well as the symmetrized (111) oriented Si(20 Å)/Ge(20 Å) SL grown on (111) $Si_{0.5}Ge_{0.5}$. The calculation was made assuming a $T^{-\nu}$ dependence for μ/κ_{ph} with $\nu=1.5$ (acoustic phonon scattering) and $\nu=1$ (empirical value for doped Si),[23] where μ is the electron mobility and κ_{ph} is assumed to be independent of T. In Fig. 3, we find that ZT increases significantly as the temperature is increased for the symmetrized (111) oriented Si(20 Å)/Ge(20 Å) superlattice, so that $ZT \simeq 1.5$ is expected at ~ 600 K for such a superlattice.

In summary, the concept of carrier pocket engineering is applied to strained Si/Ge superlattices to design materials with an enhanced ZT. The effect of the lattice strain at the Si/Ge interfaces is shown to be utilized as an additional tool to control the conduction band structure of the superlattice. The ZT calculated for the symmetrized (111) oriented Si(20 Å)/Ge(20 Å) superlattice is 0.96 at 300 K and is shown to increase significantly at elevated temperatures.

The authors would like to thank Professor G. Chen, Professor K. L. Wang and Dr. G. Dresselhaus for valuable discussions. The authors gratefully acknowledge support from ONR under MURI Subcontract No. 205-G-7A114-01 and the U.S. Navy under Contract No. N00167-98-K-0024.

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