Carrier pocket engineering applied to “strained” Si/Ge superlattices to design useful thermoelectric materials

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The concept of carrier pocket engineering is applied to strained Si/Ge superlattices to obtain a large thermoelectric figure of merit $ZT$. In this system, the effect of the lattice strain at the Si/Ge interfaces provides another degree of freedom to control the conduction band structure of the superlattice. We explore various geometries and structures to optimize $ZT$ for the whole three-dimensional superlattice. The resultant $ZT$, calculated for a symmetrized Si(20 Å)/Ge(20 Å) superlattice grown on a (111) oriented Si$_{0.5}$Ge$_{0.5}$ substrate, is 0.96 at 300 K and is shown to increase significantly at elevated temperatures. Such a superlattice can be grown using molecular beam epitaxy. © 1999 American Institute of Physics. [S0003-6951(99)04042-5]

The use of low-dimensional structures, as realized in the form of two-dimensional (2D) quantum wells and one-dimensional (1D) quantum wires, has been shown to provide a promising strategy for designing materials with a large thermoelectric figure of merit $ZT$. The original proposal that a large enhancement in $ZT$ should be possible in reduced dimensionalities used a simple model for isolated systems. Although this is a reasonable model for quantum wire arrays embedded in a porous almina template and multiple quantum wells (MQWs) with very thick and/or infinitely high (potential) barriers, revision of the model is needed to describe the thermoelectric properties of other quasi-two-dimensional systems, such as MQWs with finite barrier heights and thicknesses, including the effect of tunneling of the carriers through the barrier layers and of parasitic thermal conduction in the barrier layers. It is these latter systems that are currently of interest for actual thermoelectric applications.

Recently, the thermoelectric properties of short period GaAs/AlAs superlattices (SLs) have been calculated, first considering only the coupling of the $\Gamma$ point valley between the well and the barrier layers, and then also considering the contributions from the $X$ and $L$ valleys in the Brillouin zone (BZ). It was shown that $ZT$ for the whole SL, including the contributions from the $X$ and $L$ valleys, could be about 50 times higher than that for the corresponding bulk GaAs, if the geometry and structure of the SLs are carefully engineered so that both GaAs and AlAs layers can contribute to the thermoelectric transport. We refer to such a design process as “carrier pocket engineering.”

In the present letter, it is shown that the concept of carrier pocket engineering yields even better results for the Si/Ge SL. The reasons to study the thermoelectric properties of Si/Ge SLs include: (1) Si and Ge have a large number of conduction band valleys (six and four at the $\Delta$ and $L$ points in the BZ, respectively), (2) the SiGe alloy is already a good thermoelectric material, (3) the reduction of the lattice thermal conductivity $\kappa_{\text{ph}}$ due to interface scattering of phonons has been studied extensively, and (4) the effect of lattice strain due to lattice mismatch at the Si/Ge interfaces provides additional control over the conduction band structure of the SL as discussed below. The general scheme of our theoretical modeling has been described elsewhere. Briefly, the density of electronic states (DOS) is calculated for various high symmetry valleys in the BZ ($L$ and $\Delta$ points in the present work) using the Kronig–Penney model and the band parameters listed in Table I. Using this DOS and the constant relaxation time approximation, various thermoelectric transport coefficients are then calculated. In this letter, we first discuss the effect of uniaxial strain on the energy of the $\Delta$ and $L$ point valleys in Si and Ge, and then how to incorporate this effect in our model.

While uniaxial strain along the (001) direction, as is realized in the (001) oriented Si/Ge superlattices, has no effect on the position of the $L$-point valley extrema, it leads to a splitting of the conduction band minima at the $\Delta$ point in the BZ (called the $\Delta$ valleys) that are degenerate in the absence

<table>
<thead>
<tr>
<th>Band Parameter</th>
<th>Si</th>
<th>Ge</th>
</tr>
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<tbody>
<tr>
<td>$a_0$ (Å)$^a$</td>
<td>5.4307</td>
<td>5.6579</td>
</tr>
<tr>
<td>$m_1/m^*$</td>
<td>0.19</td>
<td>0.082</td>
</tr>
<tr>
<td>$m_2/m^*$</td>
<td>0.92</td>
<td>1.59</td>
</tr>
<tr>
<td>$E_{\text{g}}^\Delta$ (eV)$^b$</td>
<td>9.16</td>
<td>9.42</td>
</tr>
<tr>
<td>$E_{\text{g}}^L$ (eV)$^b$</td>
<td>16.14</td>
<td>15.13</td>
</tr>
<tr>
<td>$\mu$ (cm$^2$/Vs)$^c$</td>
<td>1350</td>
<td>3600</td>
</tr>
<tr>
<td>$\kappa_{\text{ph}}$ (W/m K)$^d$</td>
<td>7.3</td>
<td>3.25</td>
</tr>
<tr>
<td>$\Delta E_{\text{g}}^{\Delta-\Delta}$ (eV)$^d$</td>
<td>0.15</td>
<td>0.35</td>
</tr>
</tbody>
</table>

$^a$Data taken from Ref. 23.

$^b$Data taken from Ref. 21.

$^c$Bulk carrier mobilities at 300 K from Ref. 23.

$^d$Conservative estimate for the lattice thermal conductivity for the Si/Ge superlattice used in the present calculation. The experimental values found in the literature are somewhat smaller than this value (see Ref. 19).

$^e$Conduction band offset between the average position for Si $\Delta$ valleys and the average position for Ge $L$ valleys. The literature values for $\Delta E_{\text{g}}^{\Delta-\Delta}$ are between 0.15 and 0.35 eV (Ref. 20) depending on the hydrostatic component of the strain in the superlattice.

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of strain. The magnitudes of these splittings are given by
\[ \Delta E_c = \Xi^L_\perp (\epsilon_{\perp} - \epsilon_e), \]
and
\[ \Delta E_c = -\Xi^L_\parallel (\epsilon_{\perp} - \epsilon_e), \]
where the superscripts to \( \Delta E_c \) denote the alignment direction for the pertinent valley, \( \Xi^L_\parallel \) is the strain deformation potential for the valley (likewise, the notation \( \Xi^L_\perp \) is used to denote the \( L \) valley), and \( \epsilon_{\perp} (\epsilon_e) \) is the component for the lattice strain tensor perpendicular (parallel) to the interface. Similarly, under uniaxial strain along the \( (111) \) direction, as is realized in \( (111) \) oriented \( Si/Ge \) superlattices, the energy of the \( D \) point valleys is not affected, while the energy of the \( L \)-point valleys splits according to
\[ \Delta E_c = \Xi^L_\perp (\epsilon_{\perp} - \epsilon_e) \]
and
\[ \Delta E_c = -\Xi^L_\parallel (\epsilon_{\perp} - \epsilon_e). \]
The values for \( \epsilon_{\perp} \) and \( \epsilon_e \) are calculated assuming that the lattice constant \( (l) \) to the interfaces) for the strained layer is equal to that of the substrate, where a linear interpolation scheme is utilized to determine the lattice constant of the SiGe alloy.

Shown in Fig. 1(a) is the effect of the uniaxial lattice strain on the position of the \( D \) valley minima calculated for the \( (001) \) oriented \( Si/Ge \) superlattices grown on \( Si_{0.5}Ge_{0.5} \) and on \( Si \) substrates. When the SL is grown on a \( Si_{0.5}Ge_{0.5} \) substrate, the \( Si \) and \( Ge \) layers experience tensile and compressive stresses, respectively. Therefore, the energy for the \( Ge \) valley \( D^{011} \) is shifted upward (downward) and the \( Ge \) valley \( D^{100,010} \) is shifted downward (upward), which makes the effective barrier height smaller (larger) for the quantum well derived from the \( D^{011} \) valley. Here, the superscript on \( D \) denotes the orientation along which the pertinent valley is aligned. The resulting DOS for electrons, shown in Fig. 2(a), is calculated for a \( (001) \) oriented \( Si/Ge \) SL grown on a \( Si_{0.5}Ge_{0.5} \) substrate, where the thicknesses for the \( Si \) and \( Ge \) layers \( (20 \AA) \) are chosen so that the resulting \( ZT \) is maximized. It is noted that the quantum wells for the \( D \) and \( L \) valleys are formed in the \( Si \) and \( Ge \) layers, respectively. Therefore, there is a possibility for realization of the carrier pocket engineering concept for the \( (001) Si/Ge \) superlattice. However, for this particular case, \( L \)-point carriers make a negligible contribution to the transport, because the energy for the \( L \)-point subband edge is very high \( (\sim 200 mV) \) relative to the \( 100,010 \) subband edge. The resultant \( ZT \) calculated with this superlattice structure is \( ZT = 0.24 \) at \( 300 K \), which is rather small, although much larger than the corresponding \( ZT \) for bulk \( Si \) \( (ZT = 0.014 \) at \( 300 K \)).

We propose the following two approaches that can be used to increase \( ZT \) even further for the \( Si/Ge \) SLs. The first method is to grow the SL on a \( (001) \) substrate so that the effective barrier height for the quantum wells derived from the \( 001 \) valley will be larger due to the compressive stress on the \( Ge \) layer [see the right hand diagram in Fig. 1(a)]. Under these circumstances, the \( (001) (100,010) \) valley in the \( Ge \) layer is shifted to higher (lower) energy because of the uniaxial strain along the \( (001) \) direction, while the \( Si \) \( D \) valleys remain degenerate, since the \( Si \) layer is unstrained. The calculation of the DOS for a \( Si/Ge \) SL grown on a \( (001) \) substrate shows that the subband levels associated with the \( 001 \) valley and the \( 100,010 \) valleys, respectively,
stay very close to each other in energy, because the large effective mass along the (001) direction (confinement direction) for the $\Delta^{001}$ valley is compensated by the large barrier height of the quantum wells. The resulting $ZT$ calculated for this SL is 0.78 at 300 K, which represents more than a factor of three enhancement relative to the corresponding $ZT$ for the SL grown on a (001) Si$_{0.5}$Ge$_{0.5}$ substrate. One drawback for this SL design is that the SL is not symmetrized, i.e., the lattice constant for the completely relaxed Si(20 Å)/Ge(20 Å) SL is different from that for the substrate (Si in this case). Thus, the Si(20 Å)/Ge(20 Å) SL can be grown on (001) Si only up to a certain critical thickness before a large number of crystalline defects and dislocations are introduced.

The second method proposed to increase $ZT$ for the Si/Ge SL is to grow the SL in the (111) direction [see the middle diagram in Fig. 1(b)]. For a SL grown in this direction, the subbands derived from the $\Delta$ valleys of Si and Ge remain degenerate due to symmetry. The resulting $ZT$ for the (111) oriented Si(15 Å)/Ge(20 Å) SL grown on (111) Si$_{0.5}$Ge$_{0.5}$ is calculated to be 0.98 at 300 K [see Fig. 2(b)], which is a factor of four enhancement relative to the $ZT$ calculated for the (001) oriented Si(20 Å)/Ge(20 Å) SL grown on (001) Si$_{0.5}$Ge$_{0.5}$. Even a larger $ZT$ is expected if the superlattice is designed such that the subbands derived from the $\Delta$ valley and the $L^{111,111,111}$ valleys stay very close to each other in energy. This situation is conceptually realized by growing a Si(15 Å)/Ge(40 Å) SL on (111) oriented Si [see the right hand diagram in Fig. 1(b)]. Since the Ge layers in this SL are compressively strained while the Si layer is unstrained, only the Ge $L$-point valleys are split into a $L^{111}$ valley (higher in energy) and $L^{111,111,111}$ valleys (lower in energy). The resulting $ZT$ calculated for this structure is 1.25, which is a factor of five enhancement relative to the $ZT$ for the Si(20 Å)/Ge(20 Å) SL grown on (001) Si$_{0.5}$Ge$_{0.5}$. It should be noted that the growth of such a non-symmetrized SL is not yet possible with current MBE technology, and awaits future developments in material science.

It is of practical interest to see how $ZT$ increases as the temperature is increased. Shown in Fig. 3 is the calculated $ZT$ as a function of temperature for the symmetrized (001) oriented Si(20 Å)/Ge(20 Å) SL grown on (001) Si$_{0.5}$Ge$_{0.5}$ as well as the symmetrized (111) oriented Si(20 Å)/Ge(20 Å) SL grown on (111) Si$_{0.5}$Ge$_{0.5}$. The calculation was made assuming a $T^{-\nu}$ dependence for $\mu/k_B$ with $\nu=1.5$ (acoustic phonon scattering) and $\nu=1$ (empirical value for doped Si), where $\mu$ is the electron mobility and $k_B$ is assumed to be independent of $T$. In Fig. 3, we find that $ZT$ increases significantly as the temperature is increased for the symmetrized (111) oriented Si(20 Å)/Ge(20 Å) superlattice, so that $ZT=1.5$ is expected at ~600 K for such a superlattice.

In summary, the concept of carrier pocket engineering is applied to strained Si/Ge superlattices to design materials with an enhanced $ZT$. The effect of the lattice strain at the Si/Ge interfaces is shown to be utilized as an additional tool to control the conduction band structure of the superlattice. The $ZT$ calculated for the symmetrized (111) oriented Si(20 Å)/Ge(20 Å) superlattice is 0.96 at 300 K and is shown to increase significantly at elevated temperatures.

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