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Formation of ultrathin SiN_x/Si interface control double layer on (001) and (111) GaAs surfaces for *ex situ* deposition of high-*k* dielectrics

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In order to realize pinning-free high-*k* dielectric metal-insulator-semiconductor (MIS) gate stack on (001) and (111)*B* oriented GaAs surfaces using the Si interface control layer (Si ICL) concept, formation of a SiN_x/Si ICL double layer was investigated as a chemically stable structure on (001) and (111)*B* surfaces which allows *ex situ* deposition of HfO₂ high-*k* dielectric films without losing the benefit of Si ICL. First, Si ICLs grown by molecular beam epitaxy (MBE) on (001) and (111)*B* GaAs surfaces with various initial surface reconstructions were investigated in detail by reflection high energy electron diffraction and x-ray photoelectron spectroscopy (XPS) investigations at each step of the interface formation. Large shifts of the surface Fermi level position toward unpinning were observed after Si ICL growth on appropriately formed Ga-stabilized surfaces. It was found that Si layers grow epitaxially with Si–Ga bonds at the Si/GaAs interface and Si–As termination on top, suggesting surfactant roles played by As atoms. Then, an ultrathin SiN_x buffer film was formed on the Si ICL by its *in situ* partial nitridation in the MBE chamber. An XPS analysis of the resultant SiN_x/Si ICL double layer formed on (001) and (111)*B* surface indicated that the structure is chemically stable against air exposure on both surfaces in the sense that it prevents the host GaAs surface from subcutaneous oxidation, although SiN_x film itself partially turns into SiO_xN_y. Finally, high-*k* MIS capacitors were formed by *ex situ* deposition of HfO₂ on the SiN_x/Si ICL/GaAs structure after transferring the sample through air. The capacitance-voltage (*C-V*) analysis indicated that the MIS interface is completely pinning-free with a minimum interface state density in the range of low 10¹¹ cm⁻² eV⁻¹. © 2007 American Vacuum Society. [DOI: 10.1116/1.2750344]

I. INTRODUCTION

Recognition of near-future occurrence of ultimate scaling limit of Si complementary metal-oxide-semiconductor (CMOS) technology by Si industries such as Intel Corp.¹ has recently stimulated strong revived interests in III-V metal-insulator-semiconductor (MIS) transistors such as InAlSb/InSb MIS-heterojunction-field-effect transistors,² nanoscale GaAs MOS transistors using Ga₂O₃/Gd₂O₃, etc.,^{3,4} and MIS-field-effect transistors on vertical InAs nanowires by vapor-liquid-solid (VLS) growth.⁵ The well-known problem here is that free surfaces and MIS interfaces of III-V semiconductors generally possess high density of surface/interface states which pin the Fermi level and cause various unwanted problems. In nanoscale devices controlled by nanoscale electrodes, the surface-to-volume ratio is increased, and such problems become more serious. For example, surface states reduce control efficiency of Schottky gates,⁶ cause hysteresis effects and drain current instability, deplete near-surface carriers, cause field-induced current leakage and related side gating,⁷ and reduce quantum efficiencies of optoelectronic devices through surface recombination.^{8,9} In vertically standing GaAs nanowires produced by the VLS method or its catalyst-free modification, for example, it is difficult to obtain useful electrical conduction due to carrier depletion caused by surface Fermi level

pinning near midgap, whereas InAs nanowires show respectable conduction due to Fermi level pinning within the conduction band. Thus, success of future III-V nanoelectronics strongly depends on availability of surface passivation which can remove or control Fermi level pinning.

As an appropriate way to control III-V semiconductor surfaces, our group proposed in 1988 the use of a molecular beam epitaxy (MBE)-grown ultrathin Si layer as an interface control layer (ICL) for surface passivation.^{10,11} In the same year, two other groups also made similar proposals.^{12,13} Since then, we have been continuously investigating various aspects of the Si ICL-based passivation method for basic understanding and process optimization as well as expanding its applicability to wider range of III-V materials. These efforts are summarized in a review paper.¹⁴ On the other hand, attempts to control GaAs and InGaAs surfaces by Si ICL and Si/Ge ICL have also been made by other groups such as Morkoç and co-workers^{15–17} and, more recently, Lee and co-workers^{18,19} in order to realize high performance GaAs MOS transistors.

As for surface passivation of nanostructures which will become increasingly important as stated above, we have shown very recently the effectiveness of the Si ICL method for passivation of embedded AlGaAs/GaAs quantum wires⁹ (QWRs) as well as for removal of the surface-state-induced side-gating problem in GaAs QWR transistors.⁷ However, in

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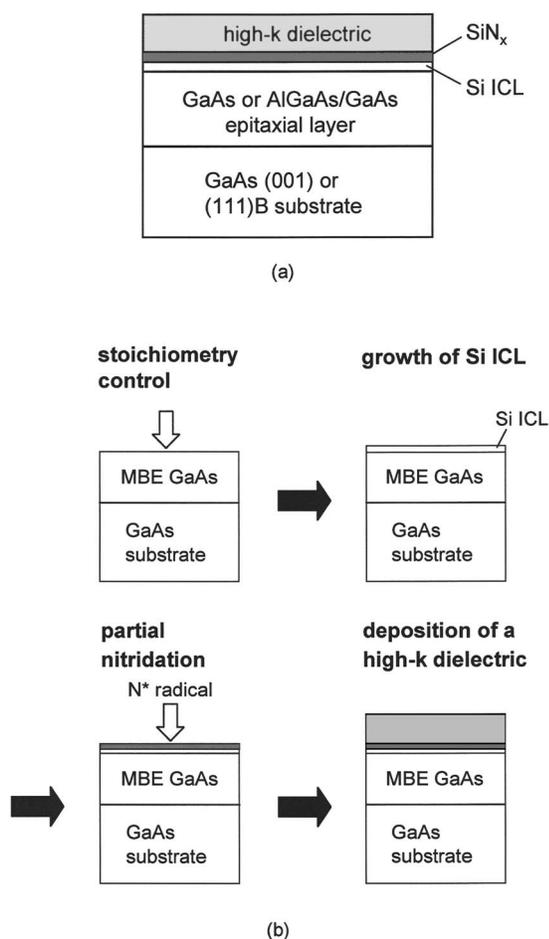


FIG. 1. (a) Structure of the Si ICL-based passivation and (b) fabrication sequence of the Si ICL-based passivation.

such applications, the Si ICL is solely used for “passivation” purpose and does not play an active role in the device operation.

In order to use the Si ICL technique more actively for MIS gate control of nanodevices, it should be compatible with the use of high-*k* dielectrics from the same reason with Si MOS gate stacks, being irrespective of whether nanodevices are classical nanoscale field-effect transistors or emerging quantum devices. Thus, compatibility with high-*k* dielectrics is an important research direction for the Si ICL method.

Another research direction is to expand the applicability of the Si ICL method to non-(001) surface orientations on which the method is applied. Our previous works have been mainly carried out on the (001) surface because of its industrial importance. However, recent great progress of III-V semiconductor nanotechnology has succeeded in producing varieties of III-V nanostructures with various high index facets on substrates with various orientations. For example, currently popular vertically standing III-V nanowires are grown on (111)*B* or (111)*A* oriented substrates and exhibit {110} facets.²⁰ Another example is our horizontally laid-out nanowire networks grown on (111)*B* substrates by selective MBE (Ref. 21) for use in a hexagonal binary decision

diagram quantum circuits.²² The latter nanowire networks possess (111)*B*, {−5, 1, −2}, and {−3, 1, 1} facets. According to the latest international technology road map for semiconductors,²³ such nanowire devices are most highly ranked as the promising emerging research devices beyond the scaling limit of the Si CMOS transistor. Thus, successful surface passivation of non-(001) surfaces is an important research target for future nanoelectronics.

With this background, the purpose of this article is to fabricate chemically stable SiN_x/Si ICL double-layer structures on (001) and (111)*B* surfaces for realization of pinning-free high-*k* MIS gate stack in such a way that the structure allows *ex situ* deposition of high-*k* dielectric films without losing benefits of Si ICL. If such an *ex situ* processing becomes possible, then the applicability of the present MBE-grown Si ICL is greatly enhanced, because formation of the basic Si ICL structure can be done *in situ* in the MBE chamber as a part of wafer growth, while device processing steps including formation of the MIS gate stack and others can be done *ex situ* in separate chambers after sample transfer through air.

In this article, Si ICLs grown by MBE on (001) and (111)*B* GaAs surfaces with various initial surface reconstructions were investigated in detail first by reflection high-energy electron diffraction (RHEED) and x-ray photoelectron spectroscopy (XPS) investigations at each step of the interface formation. Then, XPS analysis of an ultrathin SiN_x buffer film formed by partial nitridation of Si ICL was carried out. Finally, high-*k* MIS capacitors were formed by *ex situ* deposition of HfO₂ on the SiN_x/Si ICL/GaAs structure after transferring the sample through air. The *C-V* analysis indicated that the MIS interface is completely pinning-free with a minimum interface state density in the range of low 10¹¹ cm^{−2} eV^{−1}.

II. EXPERIMENT

The basic structure of the Si ICL-based surface passivation method using a high-*k* dielectric film is shown in Fig. 1(a). The role of the Si ICL is to terminate dangling bonds of the III-V semiconductor with Si atoms and to realize an ordered Si surface without Fermi level pinning. Then, Si atoms on the Si ICL are to be terminated by an ultrathin SiN_x layer formed by direct nitridation of the Si ICL by a nitrogen radical beam. Finally, a high-*k* dielectric is deposited as the main passivation dielectric to make the whole structure useful for device applications. Although the present study focuses on GaAs, application to AlGaAs/GaAs structure is a very interesting one in realizing MIS-high-electron-mobility transistors (MISHEMTs), as also indicated in Fig. 1(a).

In the above structure, the role of the SiN_x layer is first to successfully terminate Si ICL and second to serve as an effective buffer to protect Si ICL from defect formation during further deposition of the main dielectric. Even in our previous structure where Si-based insulators such as SiO₂ and Si₃N₄ were used as the main passivation dielectric, direct deposition of such Si-based insulators by thermal, plasma-enhanced, or photochemical vapor deposition (CVD) process

has been found to cause damage to the Si ICL and the use of the SiN_x layer mentioned above has been found extremely useful.¹⁴ Thus, one of the key points of the present study is to clarify whether such a SiN_x layer is chemically stable against *ex situ* deposition of high-*k* dielectric in a separate chamber where air exposure is inevitable for sample transfer.

The actual process sequence used in this study for Si ICL passivation of GaAs surfaces is shown in Fig. 1(b). Most of the sample fabrication steps were carried out in an ultrahigh-vacuum (UHV) multichamber system with a common UHV transfer chamber.

At first, *n*-type GaAs were prepared by standard MBE growth. Then, their surface reconstruction and stoichiometry were controlled in the following way. For (001) surfaces, the As-stabilized surface showing a (2×4) RHEED pattern was obtained by a standard growth condition, and it was maintained down to low temperatures by gradually reducing the As pressure during cooling. The As-rich *c*(4×4) surface was obtained by cooling without reducing the As pressure. The Ga-rich (4×6) surface was prepared by irradiating the (2×4) surface with a Ga flux after the MBE growth. On the other hand, GaAs and Al_{0.3}Ga_{0.7}As samples grown on (111)*B* substrates showed well-defined group-III stabilized ($\sqrt{19} \times \sqrt{19}$) RHEED patterns during growth at 670–700 °C. This pattern could be maintained down to room temperature by annealing the sample at 500 °C with the As flux shut off. Additionally, when the substrate temperature was lowered down to 500 °C with irradiating the As flux, the patterns changed to an As-stabilized (2×2) reconstruction, and this pattern could be maintained down to room temperature. These results are in agreement with the previous works.^{24,25} Furthermore, a Ga-stabilized (1×1) surface was obtained by depositing Ga atoms at 500 °C.

Subsequently, Si ICL was grown. For this, the As vapor in the MBE chamber was evacuated, and a 1-nm-thick Si ICL was grown by MBE at the growth temperature of 300 °C, supplying Si atoms from the *K* cell for 120 min. The RHEED pattern observed for Si ICL on (001) surface orientation turned into a (2×1) pattern from the initial one at an early stage of the growth and gradually changed to (1×1). However, the final pattern still contained very weak intermediate lines between the main bright lines, so that it could be interpreted as a weak (2×1) pattern. On the other hand, for (111)*B* surfaces, the RHEED pattern changed to (1×1) pattern at the early stage of Si growth, being independent of the initial reconstruction pattern, and it was maintained during Si growth. Both results strongly indicate that the Si film grows epitaxially. Observed exit angle dependences of the XPS Ga 3*p* spectra indicated that a uniform Si layer was formed on GaAs surfaces. Quantitatively, the thickness of the Si ICL was found to be 1 nm for all the samples. This value agreed with the intended thickness adjusted through the Si beam-flux and time.

Then, a part of the Si ICL was converted to an ultrathin SiN_x film by direct nitridation with irradiation of a nitrogen radical beam at room temperature. This was done at room

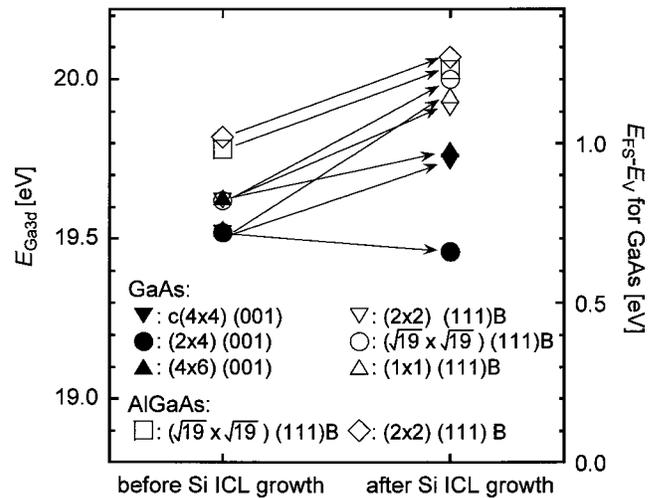


Fig. 2. Changes of Ga 3*d* peak positions and surface Fermi level positions caused by Si growth.

temperature with the nitrogen flow rate of 0.4 SCCM (SCCM denotes cubic centimeter per minute at STP) in the same MBE chamber.

Finally, deposition of a HfO₂ film was made *ex situ* in a separate chamber. Deposition was done by electron beam evaporation in oxygen ambient of 10⁻⁴ Torr at room temperature without heating the substrate. The source was a solid HfO₂ pellet. The deposition rate here was around 1 nm/s. For the sample having an outer SiO₂ layer, SiO₂ was deposited subsequently by standard plasma CVD process at 300 °C. After insulator deposition, the sample was annealed in N₂ at 400 °C for 30 min. For fabrication of MIS capacitors, Al films were deposited as field plates.

Surface structure and surface Fermi level position were investigated at each step of processing by *in situ* XPS using the Al *K*α x-ray source (1486.6 eV).

III. RESULTS AND DISCUSSIONS

A. Band bending change caused by Si ICL growth

The positions of the surface Fermi level *E*_{FS} were determined from the positions of Ga 3*d* and As 3*d* core level peaks. The energy resolution of the XPS equipment was about ±10 meV. To convert the core level position to energy position in the band gap, Ga 3*d* peak = VBM - 18.80 eV and As 3*d* peak = VBM - 40.78 eV by Kraut²⁶ were used. The same *E*_{FS} values were obtained from positions of Ga 3*d* and As 3*d* core level peaks, indicating that shifts were really due to those of the surface Fermi level. The results are summarized in Fig. 2 for various GaAs and AlGaAs (001) and (111)*B* surfaces before and after Si ICL growth. It is seen in Fig. 2 that the surface Fermi level is strongly pinned at 600–800 meV above valence band minimum (VBM) on all the MBE-grown clean *n*-type GaAs (001) and (111)*B* surfaces in spite of the fact that these surfaces give well-defined surface reconstruction patterns and well-ordered scanning tunneling microscope images. The observed Fermi level positions are almost the same with those of the chemically

etched surfaces. A similar pinning situation was also observed for AlGaAs surfaces, although ($E_{\text{FS}} - E_{\text{V}}$) was not evaluated because of lack of information for the value of ($\text{VBM} - E_{\text{Ga } 3d}$).

On the other hand, as also seen in Fig. 2, large shifts of core level spectra corresponding to movement of E_{FS} toward E_{C} take place after Si ICL growth. Thus, remarkable reduction of the band bending was achieved by the Si ICL growth. Especially, a shift of 420 meV was seen on GaAs (111)*B* surfaces, and the resultant E_{FS} corresponded almost to the flatband condition. A similar situation took place on AlGaAs (111)*B* surfaces, showing a large E_{FS} shift of 250 meV for (2×2) and ($\sqrt{19} \times \sqrt{19}$) surfaces. This preliminary result seems to be promising for future application of the Si ICL method for realization of MISHEMT devices.

The only exception was the (001) surface with the As-stabilized (2×4) reconstruction pattern where a slight increase of pinning took place. Thus, the best known and the most traditional As-rich (2×4) surface seems to be actually the most difficult one to control, most probably due to complex missing dimer reconstruction structure and volatile nature of As atoms in agreement with our previous result²⁷ and also with a more detailed study by Chambers and Loeb.²⁸

As for the observed band bending change, it was previously argued^{28,29} that it is not due to surface state removal but due to compensation of negative surface state charge by positive charge of As donors incorporated in the Si layer. However, such a simplistic view does not seem to be valid, firstly because the amount of As atoms incorporated into Si is at most in the range of 10^{11} cm^{-2} , and not large enough to compensate 10^{13} cm^{-2} level interface state charge, and secondly, and more importantly, because of difficulty of donor ionization in the present structure. Namely, the band gap of the Si layer is very much reduced by tensile stress.¹⁴ Furthermore, Si forms a surface quantum well where the first confined electron state lies high above the lowered Si conduction band edge.¹⁴ These two facts make the ionization of shallow donors difficult. On the other hand, we have recently directly shown³⁰ by scanning tunneling microscopy and spectroscopy studies of the Si ICL formed on a Ga-rich (001)-(4×6) surface of GaAs that the Si ICL grows epitaxially, and the surface becomes completely free of surface states and Fermi level pinning. Furthermore, the results showed strong correlation with macroscopic band bending measurements by XPS.³¹ Thus, considering the achievement of a nearly flatband in the (111)*B* samples, it is highly likely that the Si ICL is an ultrathin pseudomorphic single crystal layer and its ordered structure removes surface states from GaAs surfaces as well as its own surface.

B. Interface structure and growth mechanism of Si ICL

In order to get information on interface structure, deconvolution of Ga 3*d*, As 3*d*, and Si 2*p* core level spectra obtained at each process step was attempted by using Voigt fitting functions for spin split doublets with published values of spin-orbit splitting and branching ratio together with

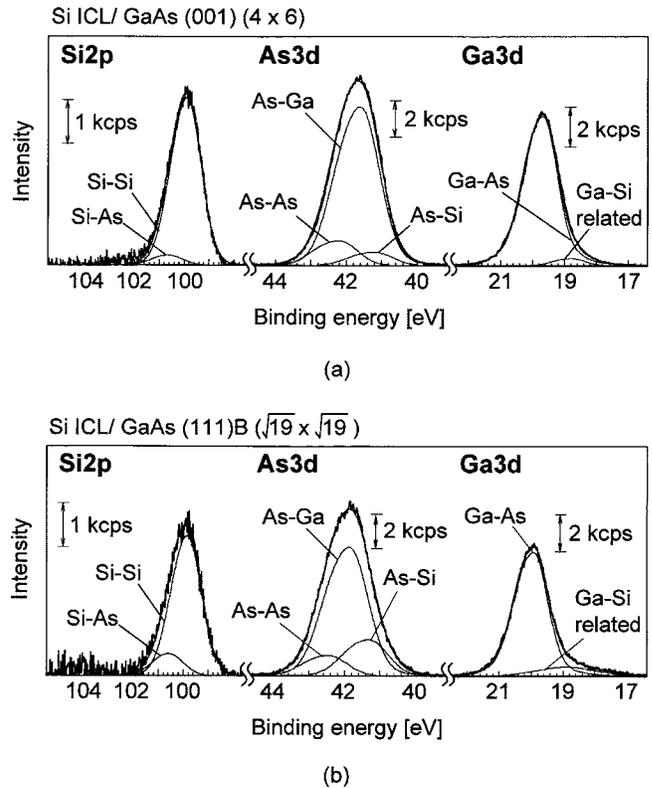


Fig. 3. Si 2*p*, As 3*d*, and Ga 3*d* spectra obtained by *in situ* XPS for (a) Si ICL/GaAs (001)-(4×6) and (b) Si ICL/GaAs (111)*B*-($\sqrt{19} \times \sqrt{19}$) structures.

certain values of disorder-induced broadening. Chemical-shift values reported in the literature²⁹ were also used when they were appropriate. Results of such an analysis are shown in Figs. 3(a) and 3(b) for GaAs (001)-(4×6) and (111)*B*-($\sqrt{19} \times \sqrt{19}$) initial surface reconstructions, respectively. Similar results were obtained on other surfaces of (001) and (111)*B* surfaces with different initial surface reconstructions. As seen in Figs. 3(a) and 3(b) a monolayer level broad peak appeared on the lower energy side in Ga 3*d* spectra after Si growth, which we interpreted as a Ga–Si related peak with possible inclusion of Ga–Ga component. In the As 3*d* spectra, a larger As–Si component was detected at the sample surface together with an As–As component. These results seem to be consistent with the work by Huen *et al.*,²⁹ although the interpretation of the band bending change is very different. In Si 2*p* peak, only As–Si component could be separated, since Ga–Si peak, if it exists, has a peak very close to the Si–Si peak.³²

Figure 4 summarizes the intensity changes of Ga–Si, As–Si, and As–As components for (111)*B* and (001) samples. A remarkable and suggestive change was observed for (111)*B* surface as seen in Fig. 4(a). After surface nitridation, the As–Si component on (111)*B* disappeared completely. This indicates that As–Si bonds were replaced with N–Si bonds. On the other hand, the peak corresponding to As–As bonds became more intense after nitridation. Since this peak disappeared completely by thermal annealing, it most likely corresponds to physisorbed As atoms on the SiN_x layer. Further-

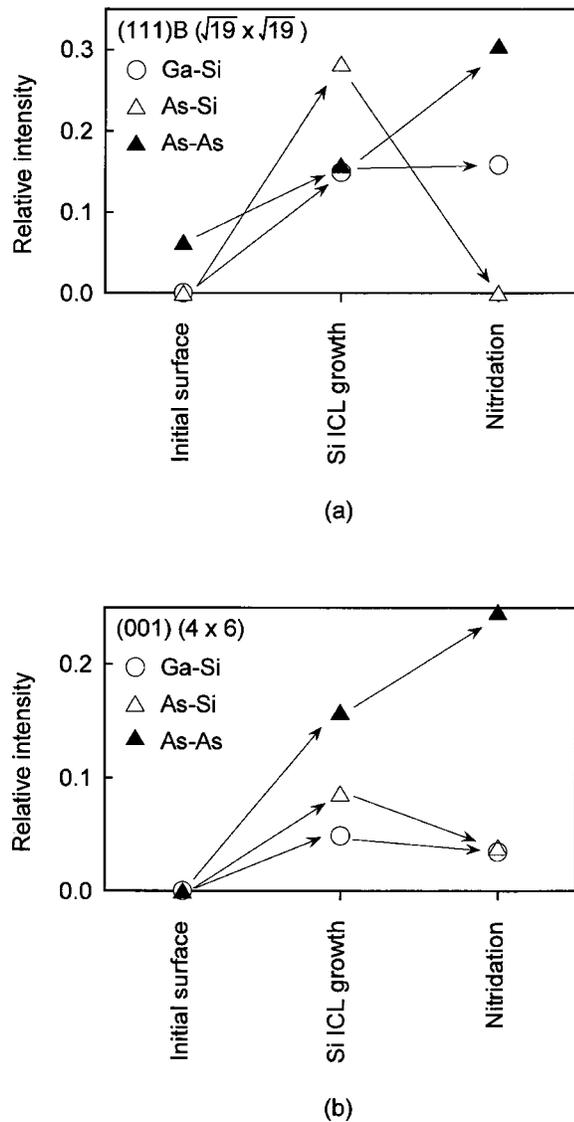


FIG. 4. Relative intensity transition of Ga-Si, As-Si, and As-As components observed on (a) (111)B-($\sqrt{19} \times \sqrt{19}$) and (b) (001)-(4 \times 6) samples at each step of the SiN_x/Si ICL/GaAs formation process.

more, Ga-Si component persisted throughout the following processes consistent with the interpretation that the Ga-Si bonds exist at the Si/GaAs interface. The similar transition was also observed for (001) samples as is also shown in Fig. 4(b). Thus, most likely, the basic bonding sequence of (GaAs)-Ga-Si-(Si ICL)-Si-As-(As top layer), as shown schematically on the top of Fig. 5, was achieved for both (001) and (111)B surfaces. After nitridation, the bonding sequence changes to that shown on the bottom of Fig. 5.

Our interpretation for the observed spectra is that the Si layer grows mostly on Ga atoms and is terminated by As atoms on top. Owing to the previously published reports, the As-terminated (111) and (001) Si surfaces are known to exhibit (1 \times 1) and (2 \times 1) RHEED patterns,³² respectively. Then the interpretation described above is consistent with the observed RHEED patterns explained in the previous section.

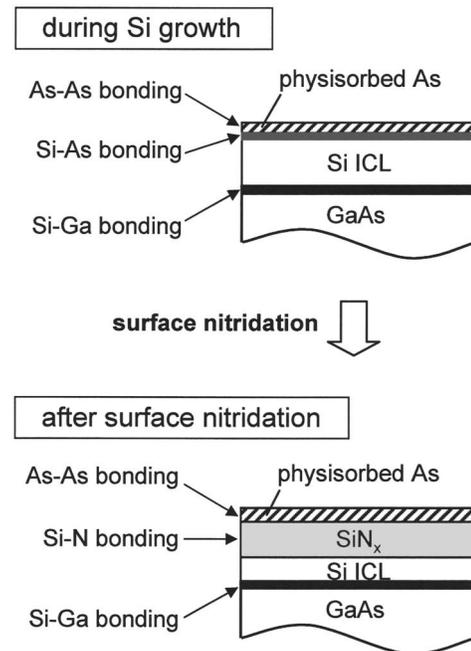


FIG. 5. Most likely bonding configurations in the vicinity of the Si ICL on GaAs during Si growth and after surface nitridation.

Since it has been reported that As atoms can take roles of surfactants for Si epitaxial growth³³ and that a highly stable As-terminated surface can be formed at 300 °C,³² it is naturally inferred that As atoms should have acted as surfactants in the present case, enhancing Si MBE growth at a low temperature. Thus, Ga-terminated flat surfaces give better epitaxy and give rise to large reduction of band bending, whereas layer-by-layer epitaxy is difficult on the complex missing dimer structure of the As-stabilized (001)-(2 \times 4) surface.

C. Structure of SiN_x/Si ICL interface and its chemical stability against air exposure

XPS characterization was made on SiN_x/Si double layers formed on (001) and (111)B GaAs surfaces before and after exposure in order to clarify their structures and their changes after air exposure.

The measured Si 2*p* spectrum is shown in Fig. 6(a) for SiN_x/Si ICL/(001) GaAs sample just after surface nitridation. Here, to avoid overlap with the Ga 3*p* peak, the Si peak was obtained by subtracting the Ga 3*p* reference spectrum from the measured spectra. This Si 2*p* spectrum was further decomposed into the Si-Si bond component and the other SiN_x-related components (Si-Si_nN_{4-n}, $n=0,1,2,3$) using the chemical-shift values reported in Ref. 34. After decomposition, these SiN_x-related components were recombined and shown as a single SiN_x peak in Fig. 6(a) for simplicity. Appearance of such a SiN_x peak was also confirmed by new appearance of an N 1*s* peak in the XPS spectra obtained after nitridation. The persistent Si-Si component showed that the Si layer still remained, indicating the successful partial nitridation. The

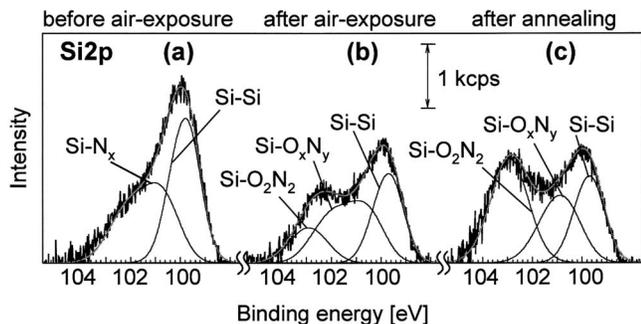


FIG. 6. XPS Si 2p spectra from the SiN_x/Si ICL/GaAs (001) (4×6) sample. Each was obtained (a) before air exposure, (b) after air exposure, and (c) after UHV annealing at 400 °C for 10 min.

average composition of the nitride layer was estimated to be close to Si₃N₂ rather than to Si₃N₄. In the Si 2p spectra after air exposure of 30 min in Fig. 6(b) and after subsequent annealing in UHV for 10 min at 400 °C in Fig. 6(c), appearance of a new peak at the highest energy position had to be assumed in both cases. Judging from the value of the chemical shift of 3.2 eV from the Si–Si peak, this peak seems to originate mainly from the Si–O₂N₂ bond.³⁴ In the intermediate region between Si–O₂N₂ and Si–Si peaks, several components, i.e., such as Si–Si_{4–n}N_n ($n=1, 2, 3, 4$), Si–Si_{4–n}O_n ($n=1, 2, 3$), Si–Si₂ON, Si–SiON₂, Si–SiO₂N, and Si–ON₃, may exist. Since an exact assignment for this region is difficult, the peak consisting of these residual components is labeled as SiO_xN_y. As seen in Figs. 6(b) and 6(c), a Si–Si peak persisted even after air exposure and annealing, indicating the existence of the Si ICL at the interface. Additionally, there was no indication of subcutaneous oxidation in all of the Ga and As related peaks after air exposure and UHV annealing at 400 °C in the MBE chamber, as shown in Figs. 7(a) and 7(b). It can be seen that Ga–Si related component persisted after entire process, whereas the As–Si component disappeared. Though As–As component was left with a reduced intensity in comparison to those in Figs. 3 and 4, we found that it can be removed completely by further air exposure and annealing. Still there was no component that can be assigned as oxide component in both of Ga 3d and As 3d spectra. Therefore, oxidation of the GaAs surface was perfectly prevented by the Si ICL covered with an ultrathin SiN_x

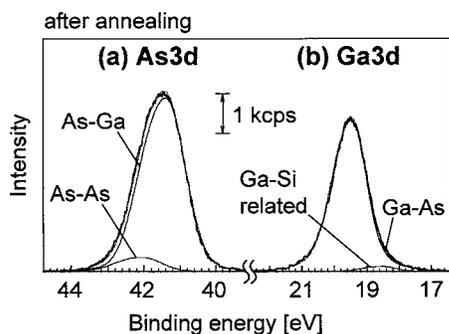


FIG. 7. XPS (a) Ga 3d and (b) As 3d spectra obtained for the SiN_x/Si ICL/GaAs (001) (4×6) sample after UHV annealing of air exposed sample.

layer. It was also confirmed that oxidation of the GaAs surface was prevented after further air exposure for many hours and even further after heating up to 200 °C in air in order to remove the samples from the ordinary Mo-block sample holder by melting the In paste. These results indicate that the present oxynitride/Si ICL passivation structure permits ordinary *ex situ* processes including those necessary for high-*k* dielectric deposition.

It should be noted that the present SiN_x/Si ICL structure behaves very differently from the SiO₂/Si ICL structure. Namely, our previous observation¹⁴ has shown that SiO₂ deposition or even air exposure quickly oxidizes the whole Si ICL with a thickness of 1 nm or so, and furthermore significant subcutaneous oxidation takes place into GaAs underneath. A similar observation was also made previously by Freeouf *et al.*³⁵ As compared with this, the chemical stability of the present ultrathin SiN_x/Si double layer is very remarkable. We believe that the chemical stability of the present SiN_x/Si ICL structure is the key factor for the photoluminescence (PL) intensity enhancement⁹ we observed on air-exposed SiN_x/Si ICL/AlGaAs/GaAs QWRs where the remaining Si ICL at the interface maintained interface order and reduced interface states.

D. Formation of MIS interfaces having HfO₂ dielectric and C-V characterization

Finally, in order to see whether the present SiN_x/Si ICL double-layer structure is compatible with *ex situ* deposition of high-*k* dielectric films and can realize reasonably well-behaved MIS interfaces, MIS capacitors were formed on (001) GaAs surfaces with (4×6) initial reconstruction by depositing a HfO₂ film on the air-exposed double-layer structure. Before HfO₂ deposition, the physisorbed As layer, which we observed after annealing in the MBE chamber as shown in Fig. 7, was completely removed by heating the sample in the deposition chamber. A separate XPS study confirmed its complete removal.

Although similar structures could also be made on (111)B surfaces, attempts of C-V study were not made in this study due to difficulty of doping control in the MBE layer which is essential for electrical characterization.

The sample structures used for the above purpose are shown in Figs. 8(a)–8(c). The structure in Fig. 8(a) is Al/HfO₂/SiO_xN_y/Si ICL/GaAs MIS capacitor with a HfO₂ film thickness of 33 nm. However, due to still not fully optimized deposition technique of HfO₂, our HfO₂ film showed premature breakdown at low field plate voltage with sudden increase of leakage current. To cope with this situation, Al/SiO₂/HfO₂/SiO_xN_y/Si ICL/GaAs structure shown in Fig. 8(b) was also prepared by additionally depositing a 12-nm-thick SiO₂ film by standard plasma CVD process. This combination formed a satisfactory stacked insulator for C-V measurement which had a effective resistivity of 10¹⁵ Ω cm, a breakdown field of 2 MV/cm, and a mean dielectric constant of 9.7.

In order to see the effect of insertion of the present SiN_x/Si ICL double layer at the MIS interface, our previous

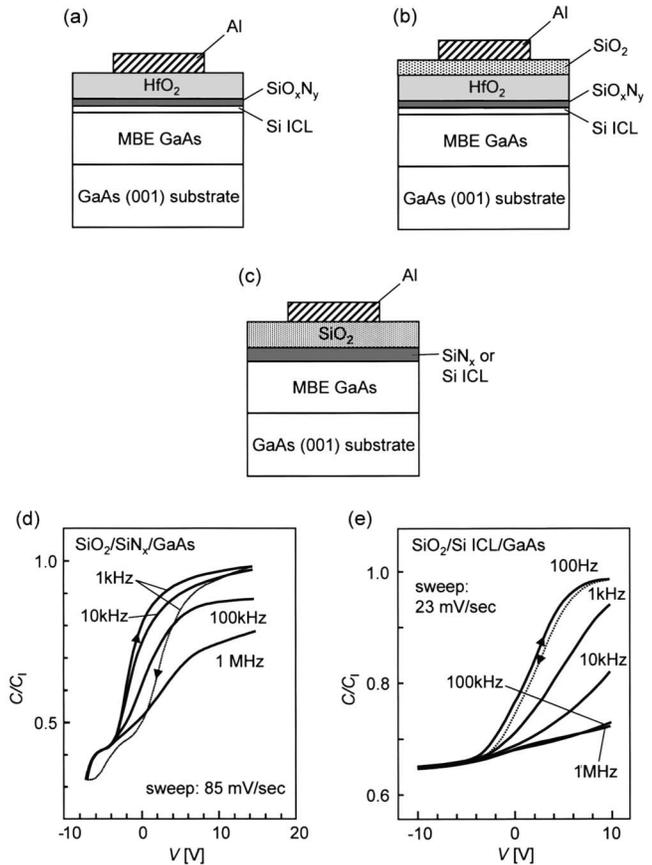


FIG. 8. Sample structures of (a) Al/HfO₂/SiO_xN_y/Si ICL/GaAs, (b) Al/SiO₂/HfO₂/SiO_xN_y/Si ICL/GaAs, and (c) Al/SiO₂/SiN_x (or Si ICL)/GaAs MIS capacitors. (d) and (e) show reference C - V curves obtained for the structures of (c).

C - V data on two structures were used as references. One is an Al/SiO₂/SiN_x/GaAs MIS capacitor without Si ICL formed on (001) GaAs surfaces with Ga-stabilized (4×6) initial reconstruction³⁶ and the other is an Al/SiO₂/Si ICL formed on (001) GaAs surfaces with As-stabilized (2×4) initial reconstruction.¹⁰ The structures of these samples are shown in Fig. 8(c) and their C - V curves are shown in Figs. 8(d) and 8(e), respectively. It is noted in Fig. 8(e) that the SiO₂/Si ICL structure shows poor C - V curves with very strong frequency dispersion and an anomalously low 1 MHz capacitance, both of which are routinely observed on conventional SiO₂/GaAs and Si₃N₄/GaAs MIS structures formed on standard As-stabilized (001) surfaces.³⁷ This is because the Si ICL is totally oxidized in the SiO₂/Si ICL structure during SiO₂ deposition which is further followed by subcutaneous oxidation, as already mentioned. Compared to this, C - V curves of the other reference sample with a SiO₂/SiN_x/GaAs structure are much better behaved. This is related to our previous finding³¹ that C - V curves of samples formed on (001)-(4×6) surface are usually much better behaved than those formed on the standard As-rich (001)-(2×4) surface in agreement with the movement of Fermi level.

The C - V curves obtained on the Al/HfO₂/SiO_xN_y/Si ICL/GaAs and Al/SiO₂/HfO₂/SiO_xN_y/Si ICL/GaAs MIS

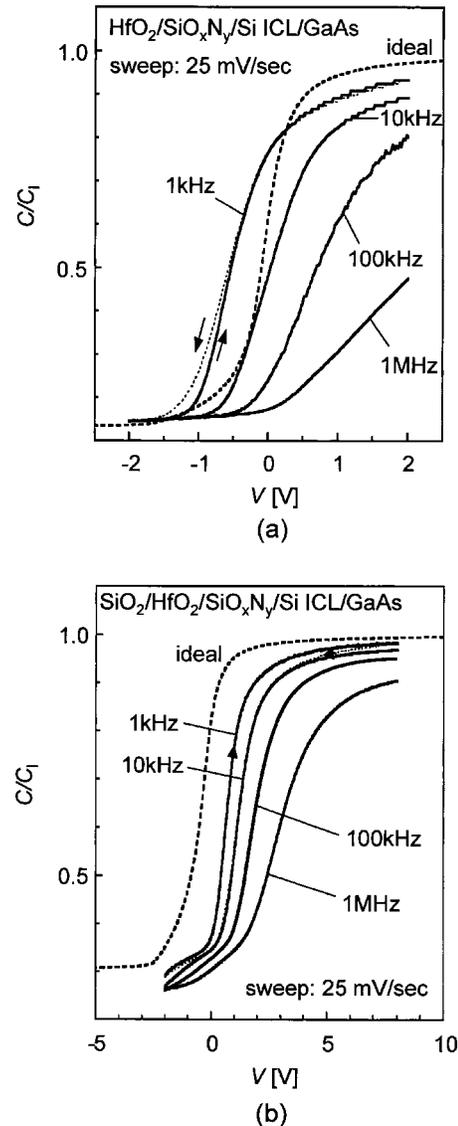


FIG. 9. C - V curves obtained for (a) Al/HfO₂/SiO_xN_y/Si ICL/GaAs and (b) Al/SiO₂/HfO₂/SiO_xN_y/Si ICL/GaAs MIS capacitors.

capacitors are shown in Figs. 9(a) and 9(b), respectively. The values of the field plate area A and the oxide capacitance C_i were $A = 3.14 \times 10^{-4} \text{ cm}^2$ and $C_i = 382 \text{ nF cm}^{-2}$ for Fig. 9(a) and $A = 3.14 \times 10^{-4} \text{ cm}^2$ and $C_i = 191 \text{ nF cm}^{-2}$ for Fig. 9(b). In order to determine the accurate values of the doping density underneath the field plate for each MIS sample, the method using the high and low capacitance ratio³⁸ together with the deep depletion sweep method of C - V curves at high bias sweep rates were combined. The resultant most likely values of doping thus determined were $N_D = 5.8 \times 10^{16} \text{ cm}^{-3}$ for Fig. 9(a) and $N_D = 1.1 \times 10^{17} \text{ cm}^{-3}$ for Fig. 9(b), respectively. Ideal C - V curves based on these are also shown in Figs. 9(a) and 9(b). As compared with the C - V curves of the reference samples without Si ICL and with a SiO₂/Si ICL structure, those of the present two types of high- k MIS capacitors are much better behaved. Namely, frequency disper-

sions are much reduced, and magnitudes of hysteresis, which are shown for 1 kHz curves for convenience, are also much reduced.

The frequency dispersion behavior of our present samples is somewhat similar to that of a HfO₂/Si ICL/GaAs MOS structure recently reported by Ok *et al.*¹⁹ and to that of a Si₃N₄/(NH₄)₂S-treated GaAs MIS structure recently reported by Jaouad *et al.*³⁹ Namely, *C-V* curves show both rightward and downward shifts of *C-V* curves with frequency. The magnitude of frequency dispersion of our sample is much smaller than that of the sulfur-treated sample³⁹ but larger than the optimized *C-V* curves in Ref. 19. Since Ok *et al.* realized very small frequency dispersion by optimization of the annealing procedure, the frequency dispersion of our sample may be further reduced by further annealing optimization. Additionally, our preliminary study on a SiO₂/HfO₂/Si structure has indicated that a part of downward frequency dispersion in Fig. 9(b) comes from that of the dielectric stack which should therefore reduce by further process optimization. At the same time, a very large sweep rate of 500 mV/s used in Ref. 19 leaves us a question whether it is sufficiently slow to establish quasiequilibrium status for the measurement. Namely, if nonequilibrium sweeps are used, they will reduce the number of participating states and, thus, gives rise to apparent reduction of frequency dispersion.

On the other hand, the frequency dispersion observed in the Gd_{0.3}Ga_{0.1}O_{0.6}/Ga₂O₃/GaAs high-*k* MIS structure reported by Passlack⁴⁰ is markedly different, showing a very large downward shift but a negligibly small rightward shift. Such differences of frequency dispersion behavior seem to be reflecting the differences in the energy and spatial distributions of interface states from the viewpoint of the disorder-induced gap state (DIGS) model,⁴¹ where DIGS continuum explains time constant dispersion and the hysteresis behavior of III-V MIS capacitors.⁴²

Distributions of the surface state density N_{ss} in the present high-*k* MIS capacitors are shown in Fig. 10 by solid curves. They were obtained by applying the Terman's method to 1 MHz *C-V* curves shown in Figs. 9(a) and 9(b). For comparison, N_{ss} distributions of several other structures, including those reported recently, are also shown by dotted curves in Fig. 10. They include the SiO₂/Si ICL/GaAs structure shown in Fig. 8(e), the SiO₂/SiN_x/GaAs structure shown in Fig. 8(d), the non-high-*k* SiO₂/SiN_x/Si ICL/GaAs structure reported in Ref. 36, the Si₃N₄/(NH₄)₂S-treated GaAs structure reported in Ref. 39, and the Gd_{0.3}Ga_{0.1}O_{0.6}/Ga₂O₃/GaAs structure reported in Ref. 40. All of the dotted curves were also obtained by applying the Terman's method to 1 MHz curves.

By comparing solid curves and dotted curves, it can be seen that the present high-*k* MIS structures exhibit low and broad N_{ss} distributions with minimum N_{ss} values of (6–8) × 10¹⁰ cm⁻² eV⁻¹, indicating that the interface is completely pinning-free and allows full excursion of Fermi level. In Fig. 10, these N_{ss} distribution curves are close to our previous best result obtained on the non-high-*k* SiO₂/SiN_x/Si ICL/

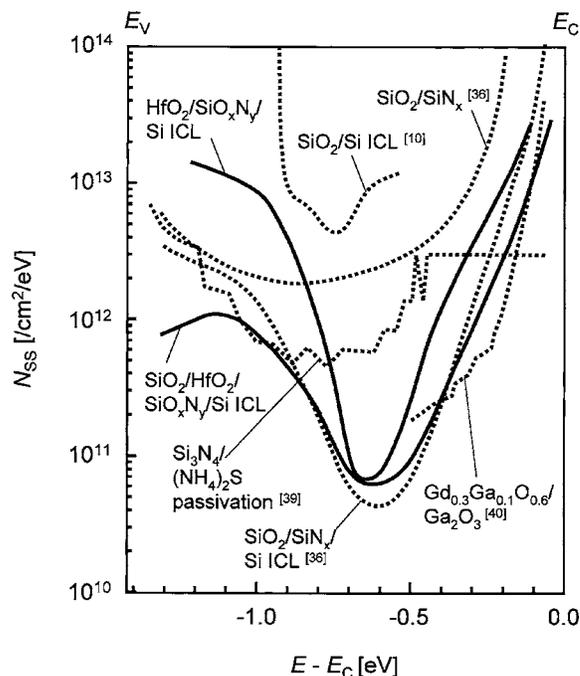


FIG. 10. Surface state density distribution evaluated for various GaAs MIS samples. Dotted lines are results by other reports with reference numbers in brackets. It can be seen that all the samples with the Si ICL indicate low interface state density distributions.

GaAs structure and also to the curve taken on the Gd_{0.3}Ga_{0.1}O_{0.6}/Ga₂O₃/GaAs structure, whereas other samples show much higher N_{ss} values. This is a remarkable and encouraging result, because our HfO₂ deposition process has not been optimized so far.

However, the validity of the observed minimum values in the 10¹⁰ cm⁻² eV⁻¹ range needs further verification by a more sensitive technique such as the conductance method, because it is well known that the Terman's method is not accurate in the low N_{ss} region by various reasons discussed in detail by Nicollian and Brews.³⁸ As for the conductance method, on the other hand, we believe that its applicability to GaAs MIS capacitors has not been well established, because the behavior of the time constant dispersion is very different from that of the so-called statistical model³⁸ for Si MOS capacitors. Namely, the conductance peak is asymmetric and more stretched out where the "tunneling model" is more appropriate as we pointed out long time ago⁴³ and later extended by Mui *et al.*⁴⁴ Thus, application of the conductance method to the present samples is beyond the scope of the article.

Coming back to the Terman's method, the most important error source is known to be the error in the value of the doping concentration. According to the textbook by Nicollian and Brews,³⁸ the Terman's method can be valid down to 1 × 10¹¹ cm⁻² eV⁻¹ for 10¹⁷ cm⁻³ doping, if the doping is accurately measured for the sample by the high-low capacitance ratio method.³⁸ In fact, Passlack made a detailed comparison between the Terman's method and the high-low

frequency capacitance method,³⁸ and the result showed good agreement of both methods down to low $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ range. Since we tried to determine the doping level accurately by high-low capacitance ratio and deep depletion sweeps for each sample as already mentioned, we can safely conclude here that our present high- k GaAs MIS structures formed on the SiN_x/Si ICL double layer have minimum N_{ss} values in the range of low $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. This result clearly indicates the benefit of the use of the chemically stable SiN_x/Si ICL where existence of pseudomorphic Si ICL is maintained after processing.

However, a more serious problem in our MIS structures as well as in the Gd_{0.3}Ga_{0.1}O_{0.6}/Ga₂O₃/GaAs structure is the sharp increase of N_{ss} toward the conduction band edge at a rate much faster rate than in Si MOS capacitors. This point should be definitely further improved for MOSFET applications.

Finally, although no C - V measurements have been done for Si ICL-based high- k MIS structures fabricated on (111) B surfaces, or other non-(001) surfaces, it is likely that the present Si ICL-based passivation structure may produce equally good or even better MIS structures on these surfaces, judging from the results of basic XPS analysis on band bending and chemical stability of SiN_x/Si ICL double layer presented here.

IV. CONCLUSION

Attempts were made in this article to realize chemically stable Si ICL passivation structures on (001) and (111) B surfaces which allow *ex situ* deposition of HfO₂ high- k dielectric films without losing the benefit of Si ICL. The SiN_x/Si ICL double-layer structure was investigated for this purpose, and detailed RHEED and XPS studies were performed at each step of structure formation, finally followed by C - V characterization of interface.

First, Si ICL surface passivation structures grown by MBE on (001) and (111) B GaAs surfaces with various initial surface reconstructions were investigated in detail by RHEED and XPS investigations at each step of the interface formation process. Large shifts of the surface Fermi level position toward unpinning were observed after Si ICL growth on appropriately prepared Ga-terminated (001) and (111) B surfaces. On the other hand, on the standard As-terminated (001)-(2 \times 4) surface, no such unpinning was observed. It was found that Si layers grow epitaxially with Si-Ga bonds at the Si/GaAs interface and Si-As termination on top, suggesting surfactant roles played by As atoms.

Then, XPS analysis of an ultrathin SiN_x buffer film formed by partial nitridation of Si ICL was carried out and the result indicated that the structure is chemically stable against air exposure in the sense that it prevents the host GaAs surface from subcutaneous oxidation, although SiN_x film itself partially turns into SiO_xN_y.

Finally, high- k MIS capacitors were formed by *ex situ* deposition of HfO₂ on the SiN_x/Si ICL/GaAs structure after

transferring the sample through air. The C - V analysis indicated that the MOS interface is completely pinning-free with a minimum interface state density in the range of low $10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$.

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