Speed-Power Performances of Quantum Wire Switches Controlled by Nanometer-Scale Schottky Wrap Gates for GaAs based Hexagonal BDD Quantum LSIs

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Abstract. This paper investigates the basic speed-power performance of Schottky wrap gate (WPG) controlled GaAs quantum wire (QWR) switches for hexagonal BDD quantum circuits. The estimated power-delay products (PDPs) of the switches were less than 10^{-20} Js at low temperatures, being smaller than those of the latest Si CMOSFETs. Direct microwave measurements and equivalent circuit analysis confirmed capability of GHz clock operation.

1. Introduction

Nanometer-scale quantum devices will play important roles in the advanced information technology (IT) of the future ubiquitous network society. This is because of their small sizes and of smallest power-delay product (PDP) values near the quantum limit, both of which may lead to high-density, high-speed and ultra low-power quantum (Q-) LSIs beyond the scaling limit of the Si CMOS technology. However, quantum devices show weak current drivability and poor threshold control, making them unsuitable to the conventional logic gate architecture. To overcome this difficulty, we have recently proposed a novel hexagonal binary decision diagram (BDD) quantum logic circuit approach [1], and demonstrated small scale circuits up to 2-bit quantum adders [2].

This paper investigates the basic speed power performance of Schottky wrap gate (WPG) controlled GaAs quantum wire (QWR) switches for hexagonal BDD Q-LSIs.

2. Basic Concept and Device Structure

2.1. Hexagonal BDD quantum logic circuit approach

As shown in **Fig. 1(a)**, the hexagonal BDD quantum logic circuit consists of node devices and root and terminal electrodes formed on a hexagonal closely packed planar QWR network. Each node device has one entry- and two exit-branches as shown in **Fig. 1(b)**, and selects the exit path for the incoming information messenger according to the gate input. The value of a logic function is determined whether the information messenger coming from the root terminal reaches terminal 1 or terminal 0 after traveling through an array of node devices. Any combinational logic function can be realized as a hexagonal BDD graph without nanowire crossover. If the messenger is a single or a few electrons, an ultra small PDP near the quantum limit can be realized.

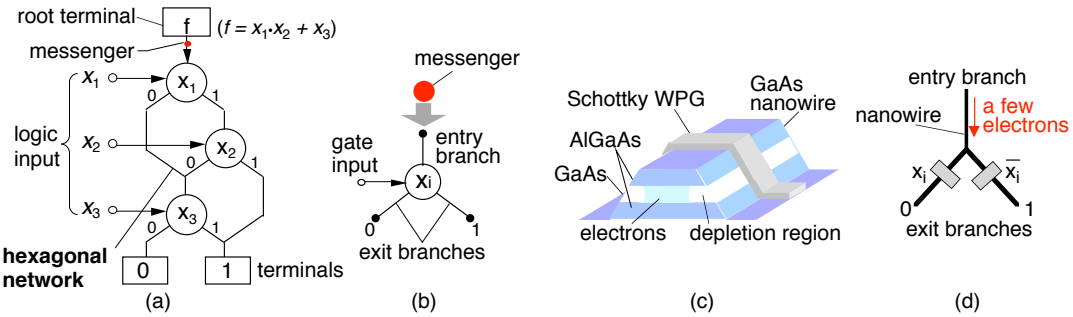

Figure 1. (a) Hexagonal BDD circuit, (b) function of node device, (c) WPG-controlled QWR switch and (d) node device used in this study.

2.2. Device structure and fabrication process

In this study, we realized QWR switches by controlling an etched AlGaAs/GaAs nanowire with a nanometer-scale Schottky wrap gate (WPG) [3] as shown in **Fig. 1(c)**. The gate has a simple structure suitable for planar integration and can provide tight potential control. A hexagonal BDD node device can be constructed by a pair of WPG QWR switches, as shown in **Fig. 1(d)**. Here path switching between zero-th and first steps of quantized conductance is made by applying gate voltages to WPGs on two exit-branches in a complementary fashion. For device fabrication, Y-branch structures were formed on an AlGaAs/GaAs heterostructure wafer by electron beam lithography and wet chemical etching. After ohmic contact formation for terminals, nanometer-scale Al Schottky WPGs were formed by EB lithography and lift-off process.

3. Experimental Results and Discussion

3.1. Quantum transport and path switching characteristics

WPG QWR switches showed excellent gate control characteristics from low temperatures up to room temperature. They exhibited clear conductance quantization at low temperatures up to 70 K, as shown in **Fig. 2** for a QWR switch with the wire width, W, of 580 nm and the gate length, L_G, of 400 nm. BDD node devices having them exhibited clear path switching operation between zero-th and first quantized conductance steps in quantum regime as shown in **Fig. 3**. At room temperature, they also showed clear path switching operation. This is because each switch operates as a classical high electron mobility transistor (HEMT) switch, controlling flow of many electrons.

3.2. Power-delay product

The value of PDP can be estimated roughly by $C_G \Delta V_G^2$, where C_G is the gate capacitance and ΔV_G is the gate voltage swing for switching. Obviously, the voltage slope of the first conductance step, $\gamma = dG/dV_G$, plays an important role in determining ΔV_G. The measured

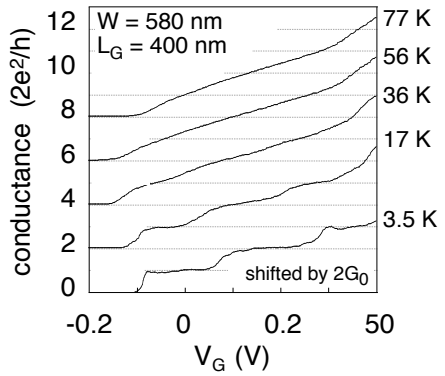

Figure 2. Conductance quantization.

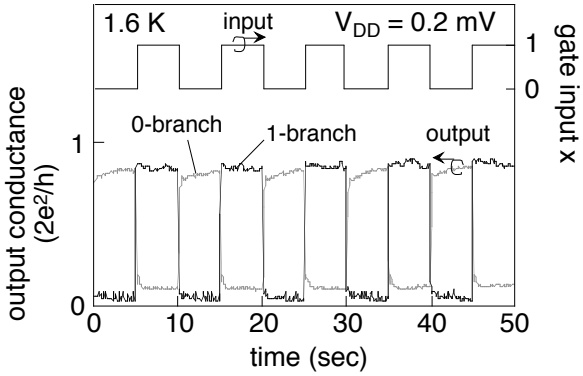

Figure 3. Path switching.

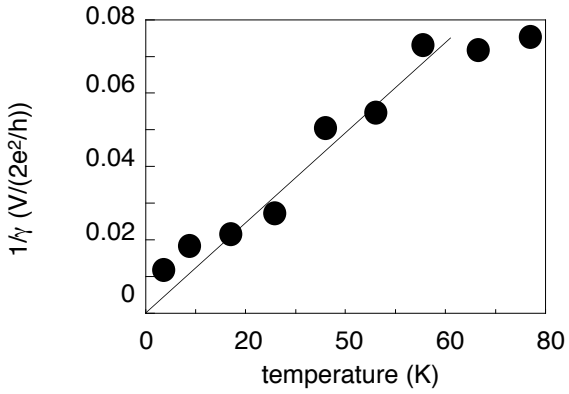

Figure 4. $1/\gamma$ vs. T.

values of $1/\gamma$ from **Fig. 2** are plotted as a function of temperature in **Fig. 4**. A linear relation was obtained up to 60 K in agreement with a theory [4] which predicts

$$\gamma = \frac{G_0}{4k_B T}\frac{d\mu}{dV_G} \tag{1}$$

where μ is a chemical potential in the QWR. From the plot, $d\mu/dV_G = 0.27$ was obtained. This value is about 10 times larger than that of the standard split gate structure [5]. Thus, the WPG can switch with 100 times smaller power consumption.

The value of the gate capacitance C_G of the QWR switch can be estimated by

$$C_G = \frac{q\Delta n_{1D} \cdot L_G}{\Delta V_G} \tag{2}$$

where n_{1D} is the electron one-dimensional density in the QWR switch. Its value was evaluated from gate-dependent Shubnikov-de-Haas (SdH) oscillation measurement [6]. As a result, $C_G = 0.6$ fF and $C_G = 13$ fF were obtained for switches with $L_G = 65$ nm and $L_G = 630$ nm, respectively. The corresponding values of PDP at 1.6 K were found to be 10^{-21} J and 10^{-20} J, respectively. As expected, a smaller PDP value was realized by reducing L_G. These PDP values are three or four orders of magnitude smaller than that of the latest Si MOSFET with $L_G = 20$ nm at room temperature [7].

3.2. Switching speed of WPG QWR switches

Direct switching speed measurements of a single WPG QWR at low temperatures could be done only up to 10 MHz due to instrumental limitation and high-impedance nature of the device. Up 10 MHz, fabricated devices worked correctly without problems.

However, an estimate of the switching speed by C_G/G_0 indicates feasibility of GHz

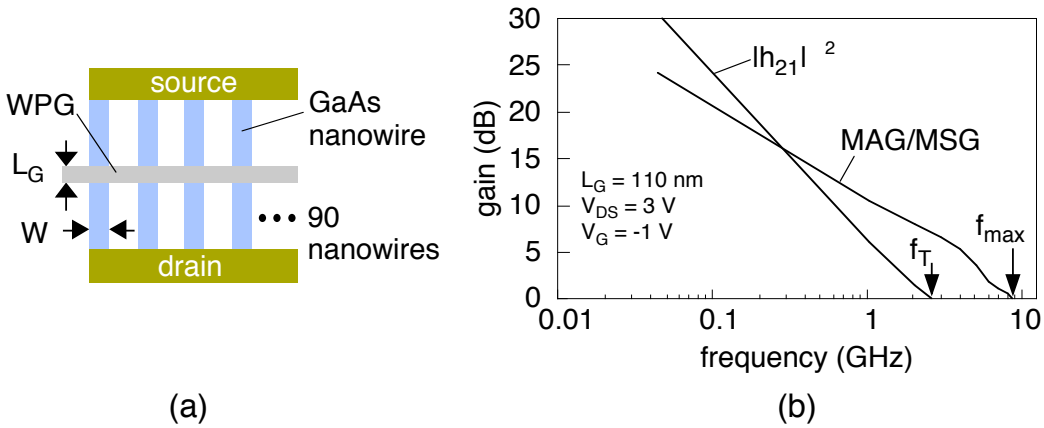

Figure 5. (a) Structure of device for RF measurements and (b) gain plots.

switching. To confirm this, special devices having 90 nanowires in parallel as shown in **Fig. 5(a)** were fabricated, since quantum devices are high impedance devices and do not fit to 50 Ω-measurement systems. Microwave measurements were then performed directly using an Agilent vector network analyzer 8510C. This could only be done at room temperature due to difficulty of RF-probing at low temperatures. **Figure 5(b)** shows the measured current gain, $|h_{21}|^2$, and MAG/MSG of the device with L_G = 110 nm, giving a cut-off frequency, f_T, of 2.5 GHz and the maximum oscillation frequency, f_{max}, of 9 GHz. The device with L_G = 630 nm gave f_T = 1 GHz and f_{max} = 5 GHz. The results directly confirms feasibility of GHz clock operation of the hexagonal BDD circuits. They also indicate that switching speed becomes faster as the gate length is reduced.

Evaluation of the device parameters were made by using a standard equivalent circuit model for a HEMT shown in **Fig. 6(a)**. The parameter values extracted by fitting the model to measured S-parameters are shown for a device with L_G = 65 nm on the right of **Fig. 6(a)**. The value of gate-source capacitance, C_{gs}, of a single WPG QWR was 0.33 fF in reasonably good agreement with the above value by SdH measurements. The value of R_i was found to be in good agreement with the expected value of gate-to-source series resistance of the wire. It was also found necessary to include parasitic capacitances, C_1 and C_2, to obtain good fitting, as shown in **Fig. 6(b)**. We tentatively assume that these parasitic capacitances are due to surface states. Thus, faster switching speeds can be realized by reducing WPG sizes and providing good surface passivation.

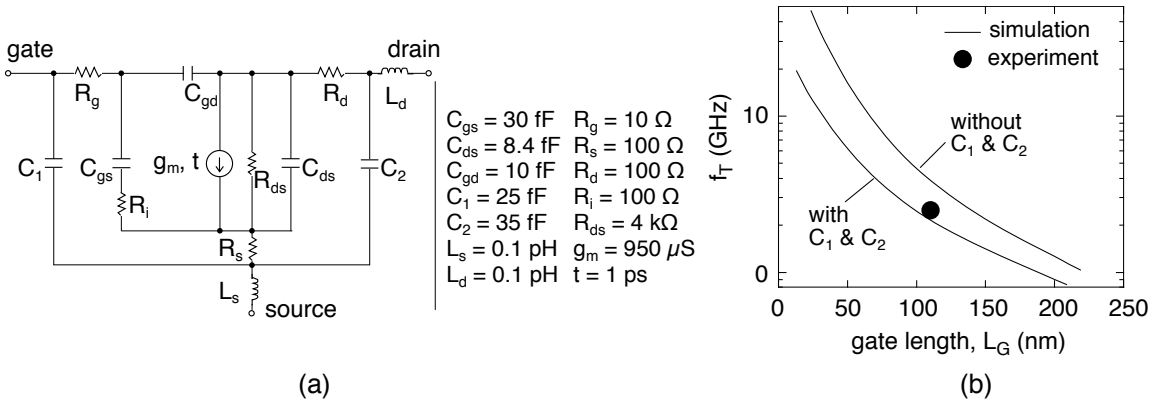

Figure 6. (a) HEMT model for GaAs QWR switch and (b) f_T vs. L_G for two cases.

4. Conclusion

PDP values of the WPG controlled GaAs QWR switches for hexagonal BDD quantum circuits are less than 10^{-20} Js at 1.6 K, being much superior to latest Si CMOSFETs. Direct microwave measurements confirmed feasibility of GHz clock operation.

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References

[1] Kasai S and Hasegawa H 2002 IEEE Electron Device Lett. 23 446
[2] Kasai S, Yumoto M and Hasegawa H 2003 Solid State Electronics 47 199-204
[3] Kasai S 1997 Jpn. J. Appl. Phys. 36 1678
[4] Bagwell P F and Orlando T P 1989 Phys. Rev. B 40 1456
[5] Wees B J van 1991 Phys. Rev. B 43 12431
[6] Yumoto M, Kasai S and Hasegawa H 2002 Appl. Surf. Sci. 190 242-246
[7] Chau R 2001 Nanoelectronics Workshop (Kyoto)