Multiple path switching device utilizing size-controlled nano-Schottky wrap gates for MDD-based logic circuits

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Abstract

A novel simple and compact multiple-path-switching device for multiple-valued decision diagram (MDD) is proposed and investigated theoretically in order to realize high-performance nanowire-network-based logic circuits with advanced functionality. The device is designed on multi-semiconductor-nanowire branches having a couple of size-controlled nanometer-scale Schottky wrap gates (WPGs). The device selects an exit branch for messenger electrons according to gate voltage as a multiple-valued input variable. The path-switching function is realized by multiple assign of gate threshold voltages and applying complementary gate voltages to the two WPGs. Theoretical investigation based on three-dimensional potential simulation confirms that clear current path switching takes place in the proposed device.

Keywords: Multiple-path switching, Nanodevice, Nanowire, Schottky wrap gate (WPG), Threshold voltage shift, Multiple-valued decision diagram (MDD).

1. INTORDUCTION

Nanostructures including nanowires, nanotubes and their network structures are expected to play important roles in the next-generation nanoelectronics, because of their small size, high-density integration capability, etc. Recently, their formation, processing and device technologies have been developed intensively [1,2]. However they have never been used in modern CMOS LSIs because the logic gate-based circuits require sever size and position control with extremely high uniformity in materials and devices. To overcome this problem, a novel logic circuit utilizing hexagonal nanowire network structures, called a hexagonal BDD quantum circuit was proposed [3,4], and its feasibility has been confirmed by demonstrating various circuitries experimentally [4-6]. In this circuit approach, a binary decision diagram (BDD) is utilized for its logic architecture instead of the conventional CMOS logic gates. This enables us to integrate quantum wire devices and/or single electron devices, and to operate the circuit either in quantum transport domain in low temperatures or classical transport domain at room temperature. For giving further advanced functionality to this approach, multiple-valued logic (MVL) is very attractive since it can execute arithmetic and logic functions faster and can be realized on compact area with less interconnection than that of the binary logic. An extension of BDD techniques for multiple valued functions, multiple-valued decision diagram (MDD) has been investigated from 1990s [7-9]. As in the hexagonal BDD circuits, similarity in the physical structure of nanowire networks and the logical structure of a logic function represented by the MDD provides an opportunity to implement the logic function on the nanowire networks directly in material and physical levels. In addition, multiple-branch nanowire network structures can be easily produced by modern bottom-up-type nanotechnology. Then, combination of the MDD and nanowire networks has possibility to open up a new logic LSI technology. An elemental device for hardware implementation is a multiple-path-switching device which function is to switch multiple paths according to multiple valued input. However, simple and compact semiconductor-based device for the MDD has not been realized yet. The purpose of this paper it to propose a novel multiple path switching device for realization of MDD-based logic circuits, implementing it by semiconductor-based nanowires with size-controlled nanometer-scale Schottky wrap gates (WPGs), and to demonstrate its operation based on three-dimensional (3D) potential simulation.

2. CONCEPT AND THEORY

The MDD is a represent scheme of a multiple-valued logic function by a directed acyclic graph. Finite-multiple-valued function f: $R^n \rightarrow R$, where R={0, 1,..., r-1} and n is number of variables, is considered in this study. Each node has an entry and multiple exit branches as shown in **Fig. 1(a)**. When an input signal of $x_i = j$ (j=0,1, ..., r-1) is given to the node, it selects the exit branch labeled j. Then, an information messenger entering from the entry branch goes out from the j-branch. We call it a MDD node device. Each exit branch represents 0 or 1. Graphically represented multiple-valued logic functions using Shannon expansion is implemented as a circuit by integrating the devices as shown in **Fig. 1(b)**. The circuit has a root, a set of terminals and node devices. For logic evaluation, electron messenger is sent from a root to terminals after setting multiple-valued input to each node. If the messenger is detected in terminal labeled "j", then the logic value is "j". As seen in the example, the graph has a complex network structure. If we can realize the node device by controlling nanowire networks, it becomes possible to implement the logical graph structure directly on the 2D or 3D nanowire network structures that can have complex network configurations. Approach to planar implementation of the MDD was also discussed previously[9].

A basic concept of a MDD node device proposed in this paper is shown in **Fig. 1(c)**. In this device, every branch is formed with a semiconductor nanowire channel. All exit branches have two gates labeled A and B, which control carrier conduction in the branch by the filed effect. Standard gate structures are Schottky gates or metal-oxide-semiconductor (MOS) gates. A key for implementing multiple-path-switching function is to assign different threshold voltage to each branch and gate. In the case that the number of exit branches is r,

$$\begin{cases} V_{thA0} > V_{thA1} > \cdots > V_{thAj} > \cdots > V_{thAr-1} \\ V_{thB0} < V_{thB1} < \cdots < V_{thBj} < \cdots < V_{thBr-1} \end{cases} \quad (1)$$

where $V_{\mathrm{thA}j}$ denotes a threshold voltage of the gate A in the j-branch (j=0,1,...,r-1). $V_{\mathrm{thB}j}$ is in a similar way. Assuming n-type depletion-mode-channels for all branches, transfer characteristics in **Figs. 2(a)** and **2(b)** for the gate A and B, respectively, are realized. For the path switching operation, gate voltages for the gate A and B, V_{GA} and V_{GB}, respectively, are given in complementary fashion,

$$V_{GB} = -V_{GA} + \alpha \quad (2)$$

where α is constant. Then, the conductance in the j-branch for the gate A, $G_{\mathrm{A}j}$, monotonically increases as increase of V_{GA}, although, the conductance for gate B, $G_{\mathrm{B}j}$, monotonically

decreases as increase of V_{GA}. It should be noted that both G_{Aj} and G_{Bj} should be non zero only when $V_{thAj} < V_{GA} < \alpha - V_{thBj}$. Thus, in the proposed device, threshold voltages also satisfies following conditions,

$$V_{thAj} < \alpha - V_{thBj} \quad . \tag{3}$$

Current in each exit branch is given by harmonic average of conductance in **Figs. 2(a)** and **2(b)**, as a series circuit configuration. Then, the current in the j-branch, $I_j(V_{GA})$, is given by

$$I_j(V_{GA}) = \frac{G_{Aj}(V_{GA})G_{Bj}(V_{GA})}{G_{Aj}(V_{GA}) + G_{Bj}(V_{GA})} V_{DD} \tag{4}$$

where V_{DD} is applied voltage to the entry branch. It is found that I_j arises only when $V_{thAj} < V_{GA} < \alpha - V_{thBj}$ and it vanishes for other V_{GA} condition. Resultant exit branch currents are schematically shown in **Fig. 2(c)**. Each branch should show a single peak current as a function of V_{GA}. Fundamentally, based on this path switching mechanism, any number of exit branches can be switched only a couple of gates and any number of multiple values are possible.

In this study, semiconductor-based nanowire networks controlled by nanometer-size Schottky wrap gates (WPGs) are applied to implement the proposed MDD node device. The WPG is a fine Schottky gate wrapped around a nanowire as shown in **Fig. 3** [10]. Appling suitable voltage to the WPG, it squeezes the nanowire channel electrostatically and controls conductance in the nanowire. Tight gate control can be obtained in the WPG structure because of its three dimensional gate configuration. In this approach, V_{th} is changed by controlling gate length in nanometer scale. Short gate length results in large V_{th}, which is so called short channel effect [11]. In order to realize the conditions given by **Eq. (1)**, WPG gate lengths are designed to satisfy $L_{GA0} > L_{GA1} > L_{GA2} > ... > L_{GAr-1}$ and $L_{GB0} < L_{GB1} < L_{GB2} < ... < L_{GBr-1}$, as schematically shown in **Fig. 1(b)**. To realize MDD-based logic circuits integrating node devices, nanowire network structures controlled by WPGs are suitable. This approach focuses on the topological similarity between the logical structure of a graphically represented logic function by the decision diagram technique and the physical structure of the nanowire network. The logic function is directly implemented on the hardware in material level [4].

3. SIMULATION STUDY

We investigated the operation of a proposed device theoretically using a 3D potential

simulation in which a 3D Poisson's equation was solved numerically by a finite difference method. For simplicity, three-valued MDD devices having three exit branches was considered. A base structure was an $Al_{0.3}Ga_{0.7}As/GaAs$ modulation doped heterostructure with two-dimensional electron gas (2DEG) at the interface. Nanowires were formed by etching the structure. The nanowire width was 400 nm. WPG length was changed from 50 nm to 500 nm. Conductance in each branch was evaluated as follow. In first, local conductance under a WPG for the gate A in the *j*-branch was calculated by a standard formula for the field-effect transistor (FET) in linear region, $G_{Aj}(V_{GA}) = e\,\mu\,n_{1D}(V_{GA})L_{GAj}^{-1}$, where e is an electron charge, μ is a mobility of electrons, n_{1D} is a electron line density and L_{GA} is the WPG length. The conductance under the gate B, $G_{Bj}(V_{GB})$, is given in a similar way. $n_{1D}(V_G)$ for each gate having different gate length was calculated using the 3D potential simulation. Then, current in the exit branch was computed using **Eq. (4)**. Temperature of 300 K was assumed for all calculations.

4. RESULT AND DISCUSSION

In first, we evaluated gate-length-dependence of threshold voltage in the nanowire controlled by a single WPG. **Figure 4(a)** shows calculated conductance as a function WPG gate voltage for various gate lengths. The calculation included the effect of parasitic series resistance of 10 kΩ. It could be seen that V_{th} clearly decreased when L_G decreased. **Figure 4(b)** plots evaluated V_{th} as a function of L_G. V_{th} shift occurred when L_G was less than 500 nm. The shift was remarkable when L_G was less than 200 nm. Quite large difference of 200 mV was obtained even with slight L_G change from 70 nm to 50 nm. These values might on materials and structures. Anyway, such gate lengths can be realized easily by the modern semiconductor process technology. We also experimentally confirmed such V_{th} shift in fabricated devices [12].

Based on the results above, the operation of the node device having three exit branches was investigated. WPG gate lengths of the device were $L_{GA0} = L_{GB2} = 200$ nm, $L_{GA1} = L_{GB1} = 100$ nm and $L_{GA2} = L_{GB0} = 70$ nm. **Figure 5** shows calculated conductance in each branch for the gate A and B, respectively. Complementary gate voltage given by $V_{GB} = -V_{GA} - 1.2$ was applied to the gate B. The gate length design above resulted in nearly equal V_{th} shifts of 200 mV. From **Eq. (4)**, it was understood that an overlap region of solid and dotted curves in a branch resulted in the exit branch current. Cross points of these currents indicated by arrows

in **Fig. 5**, gave an input gate voltage value for selecting the *j*-branch. It is possible to adjust input voltage value for selecting a branch, logic swing and margin on demand by suitable design of WPG lengths.

Figure 6 shows obtained path switching characteristics. Clear path switching could be realized in the designed device. Each exit branch current had a bell like shape. Peak heights were nearly same for all exit branch currents. As described above, peak positions were given by the cross point of currents controlled by each gate. Peak interval was 200 mV. This value corresponded to V_{th} shift shown in **Fig. 5**. Full width at half maximum (FWHM), giving the switching margin, was 230 mV for all current peaks. At the peak position in the selected branch, small current tails from the other branches was seen, however it was 1/10 of the current from the selected branch. From **Fig. 5** and **Fig. 6**, it seemed that the FWHM depended on difference in V_{th} and gate controllability, dG_{Aj}/dV_{GA} and dG_{Bj}/dV_{GB}, for gate A and B. Tails of current peaks were dominated by subthreshold characteristics. Higher gate controllability and smaller subthreshold slope provide a sharper peak with small tails. These are important for increasing the number of input variables. Because a WPG structure gives tight gate control characteristic, WPG-controlled nanowire is suitable for implementing the proposed MDD device based on V_{th} control.

5. CONCLUSION

A novel simple and compact multiple-path-switching device for multiple-valued decision diagram (MDD) was proposed and investigated theoretically. The device was designed on multi-semiconductor-nanowire branches having a couple of size-controlled nanometer-scale Schottky wrap gates (WPGs). Multiple-path switching function was realized by multiple assign of gate threshold voltages and applying complementary gate voltages to the two WPGs as an input signal. Theoretical investigation based on three-dimensional potential simulation confirmed that clear current path switching took place in the proposed device.

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FIGURE CPATIONS

Fig. 1. (a) MDD node device, (b) diagram of three-valued-variable comparator and (c) physical design of the proposed device.

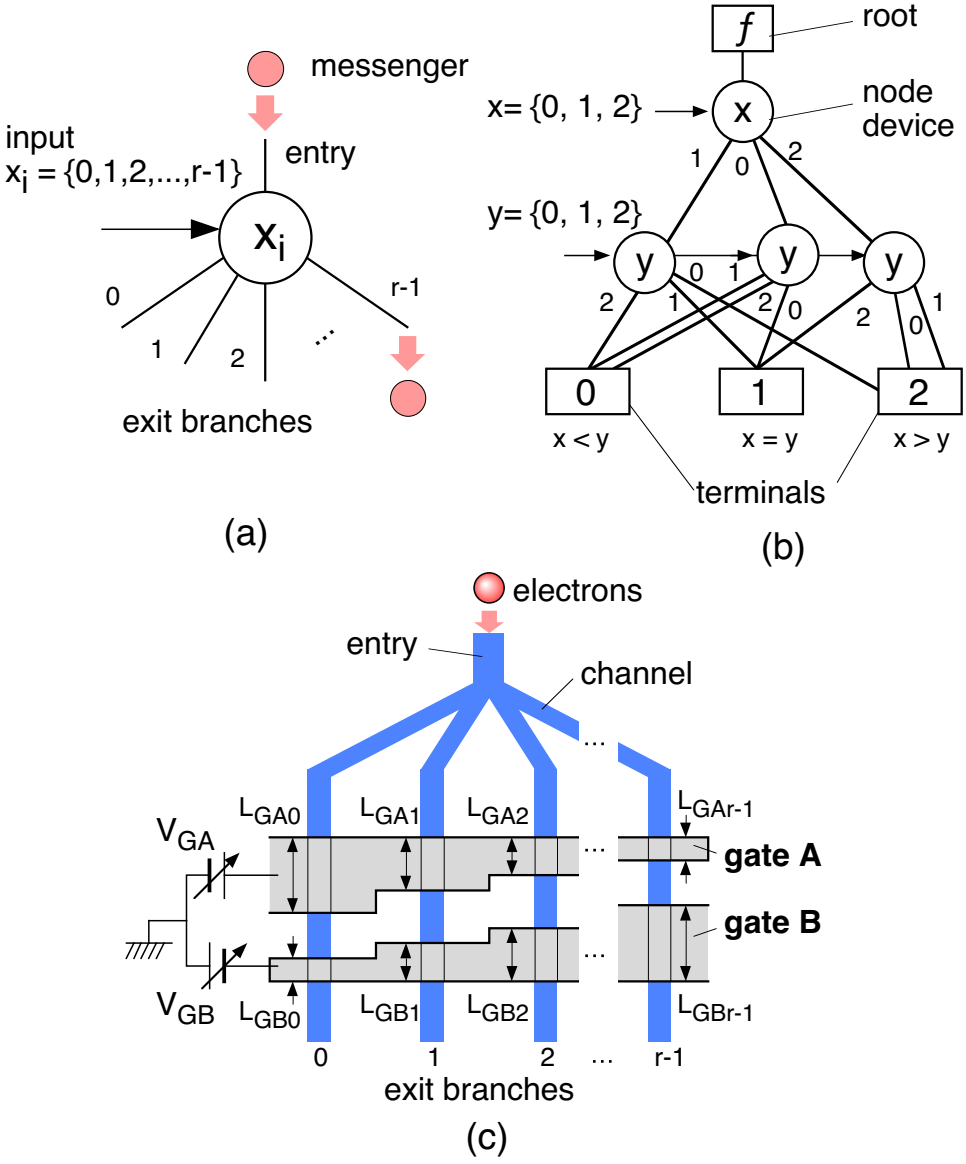
Fig. 2. Transfer characteristics (a) for gate A and (b) for gate B. (c) Ideal path switching characteristics in the proposed device.

Fig. 3. Concept of WPG-controlled nanowire structure.

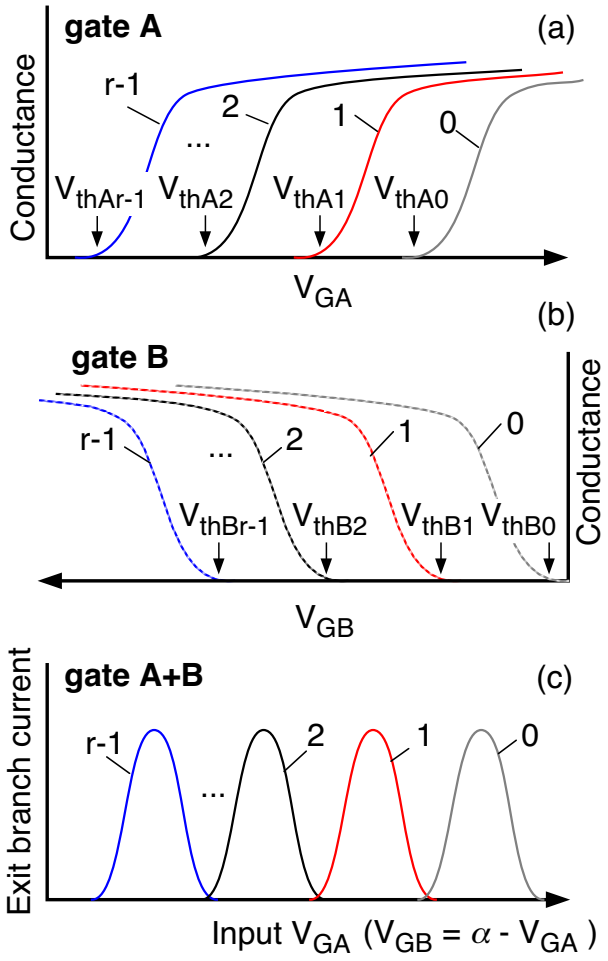
Fig. 4. (a) Nanowire branch conductance as a function of gate voltage for various WPG lengths and (b) threshold voltage, V_{th}, as a function of gate length, L_G.

Fig. 5. Conductance as a function of gate voltage in exit branches for each gate. Solid and dotted lines are for gate A and B, respectively.

Fig. 6. Path switching characteristics.



Kasai et al., Fig. 1



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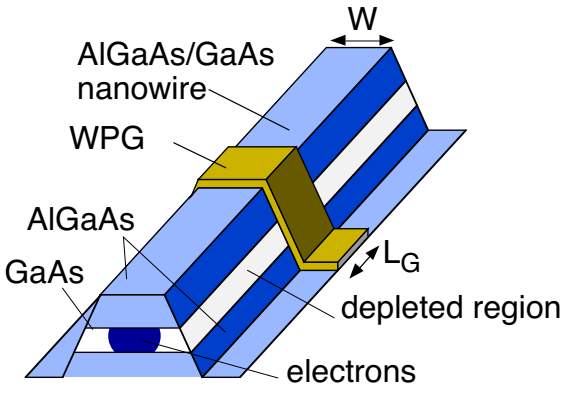

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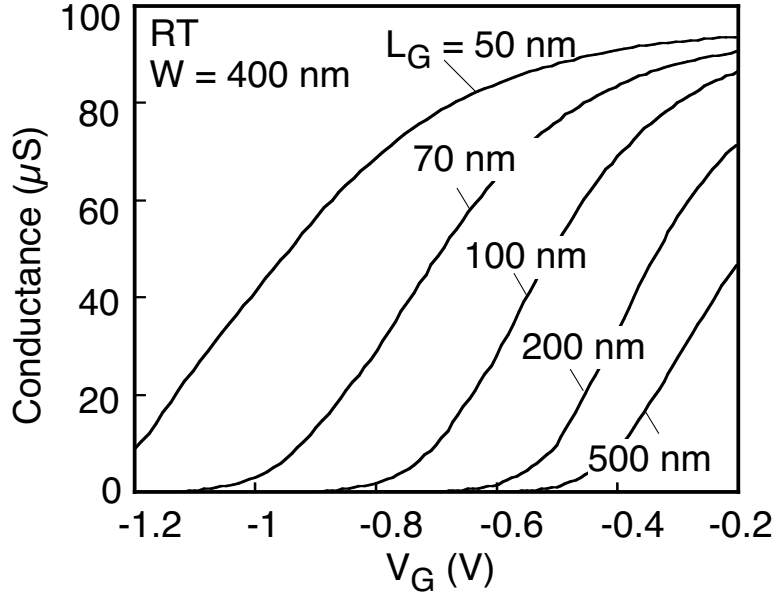
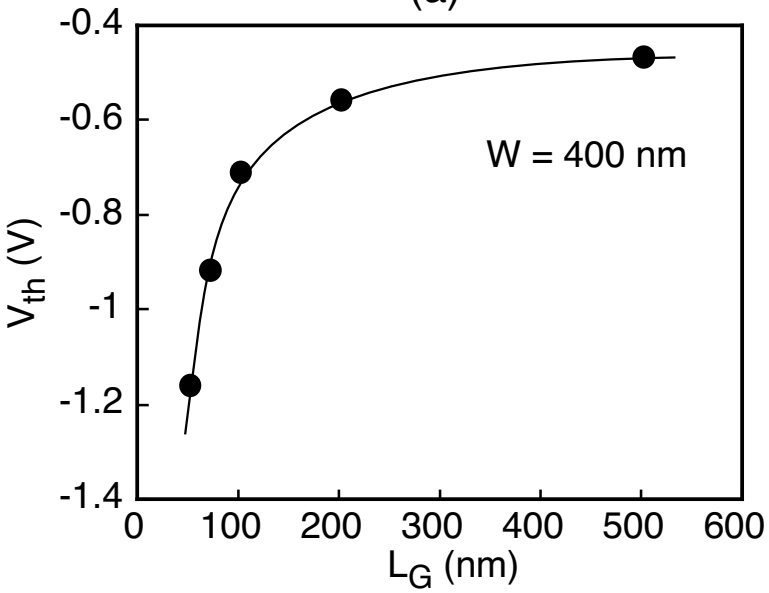


(a)



(b)

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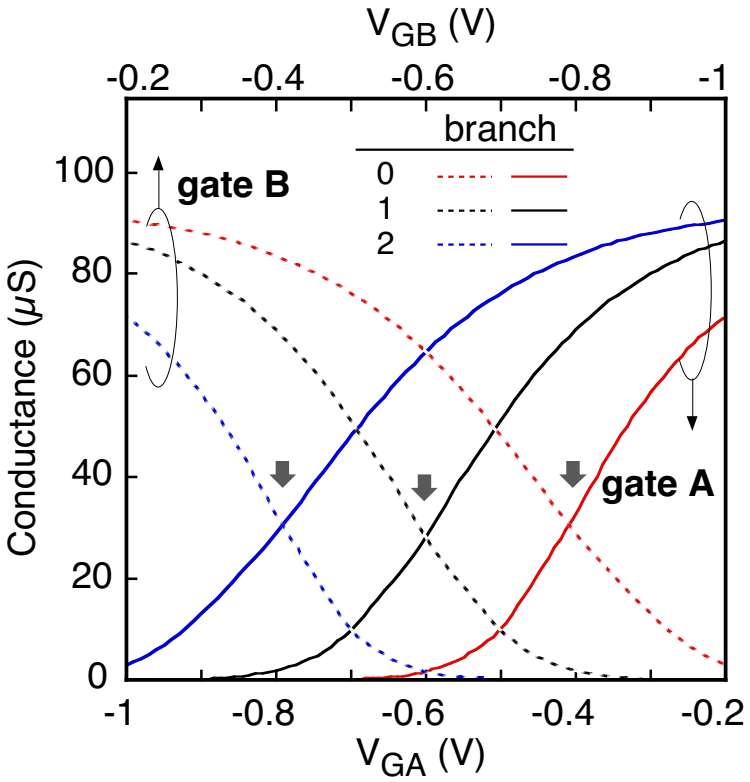
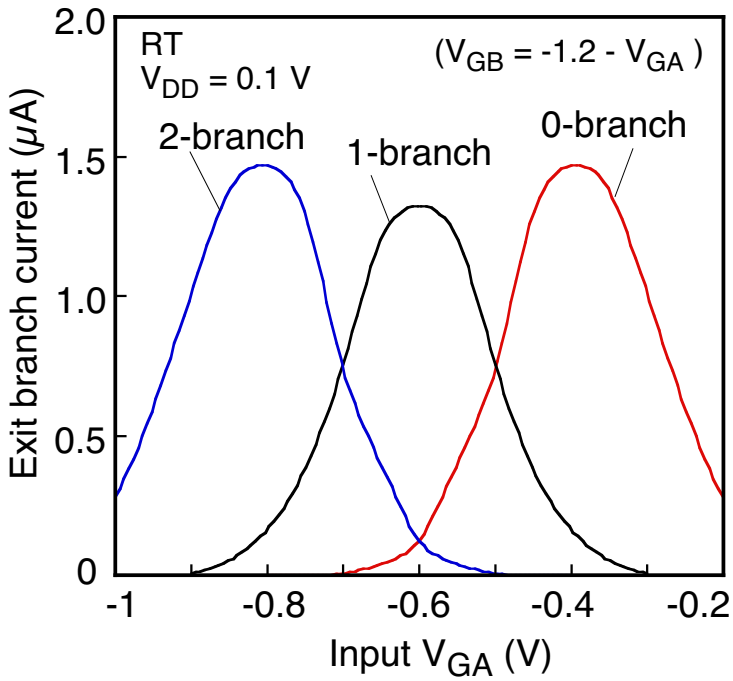


Kasai et al., Fig. 5



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