GaAs-Based Single Electron Transistors and Logic Inverters Utilizing Schottky Wrap-Gate Controlled Quantum Wires and Dots

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GaAs-based single electron transistors (SETs) and their logic inverters were successfully designed and fabricated using a Schottky wrap-gate (WPG) quantum wire and dot formation technology. Three-gate WPG SETs, which have two tunnel barrier gates and center gate for a quantum dot-potential control, showed voltage gains larger than unity due to tight dot-potential control of the center WPG. The conductance peak position of the SET could be systematically controlled by changing the tunnel-barrier-control WPG voltages. A resistive-load single electron inverter utilizing 3-gate WPG SET as a driver and a WPG quantum wire transistor as an active load was fabricated and it showed a proper inverter operation at 1.6 K and realized a logic transfer gain of larger than unity (1.3) for the first time in III-V semiconductor-based SET inverters. A III-V semiconductor-based complimentary inverter utilizing two 3-gate WPG SETs was also successfully fabricated for the first time and the inverter operation was also confirmed at 1.7 K.

KEYWORDS: single electron transistor (SET), single electron logic inverter, Schottky wrap gate (WPG), GaAs, transfer gain, quantum dot, quantum wire

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1. Introduction

Ultimate information processing technology by manipulating single electrons in III-V compound semiconductor quantum structures is extremely attractive for next-generation electronics in wireless and optoelectronic environments. Such a technology has the potential to realize high-speed and high-volume information processing with ultrahigh density integration, ultralow power consumption and rich functionality. Significant and pioneer works on various single electron devices have been made by using III-V compound semiconductors[1,2]. However, from engineering viewpoints, logic gate and memory circuit applications of III-V semiconductor-based single electron devices are premature compared with those of Si-based single electron devices[3,4] which are supported by strong confinement potentials utilizing SiO_2/Si interfaces and an advanced LSI fabrication technology. For realization of the III-V compound semiconductor-based single electron circuits, it is important to develop a single electron transistor (SET) that has a structure suitable for high-density planar integration by means of a simple fabrication process, and that realizes sufficient performance including a voltage gain larger than unity, a high conductance peak, and its position control. To satisfy these requirements, the Schottky wrap gate (WPG) structure applied to III-V semiconductor heterostructures[5] is very attractive, because it has advantages of a stronger confinement potential for electrons than the previous split-gate structure[1], high gate controllability realizing a voltage gain larger than unity[6], a simple lateral structure, a simple fabrication process and flexibility of device design.

The purpose of this study is to fabricate and characterize GaAs-based single electron logic inverters with a proper inverter operation and a sufficient transfer gain using GaAs-based WPG SETs. A preliminary report on the operation has already been reported elsewhere[7], and a detailed description on device and circuit design, simulation, fabrication and characterization is given here.

2. Basic Design Consideration of Schottky Wrap Gate-Based Single Electron Transistors and Their Circuits

The basic concept of the WPG structure is schematically shown in Fig.1(a). This structure has an AlGaAs/GaAs etched nanowire with a width of 180 - 600 nm and a Schottky gate is wrapped around it. This produces a strong confinement potential on the quasi-one-dimensional electron layer underneath the AlGaAs/GaAs heterointerface by depleting electrons directly from both sides as well as from the top of the structure[8]. The control of the potential by the WPG is tighter than that of the conventional split gate structures. A device having a single WPG as shown in Fig.1(a) operates as a quantum wire

transistor (QWTr). A device shown in Fig.1(b) having two short WPGs works as an SET, since complete electron depletion underneath WPGs forms double tunneling barriers with a quantum dot in between. By arranging WPGs and nanowires, the other various single electron devices and single electron logic gates can be simply designed. For the circuit application, a 3-gate WPG SET which has a dot-potential-control WPG between the tunnel-barrier-control WPGs as shown in Fig.1(c) appears to be suitable. The WPG located just above the quantum dot can control the charge in the dot very tightly, similar to field effect transistors (FETs), and a high voltage gain larger than unity has been previously realized using this structure[6)]. Additionally, independent control of tunnel barriers and dot potential provides the possibility of independent voltage control of the conductance peak position and peak height; such a possibility has not been previously explored.

Two possible designs of the single electron logic inverters utilizing the 3-gate Schottky WPG SETs are shown in Figs.1(d) and 1(e). They are a resistive load inverter and a complementary inverter, respectively. The latter was proposed by Tucker[9)], and is important for further reduction of power consumption. The resistive load inverter has a driver 3-gate WPG SET and a WPG QWTr as an active load. In this configuration, the input is applied to the dot-potential-control WPG of the 3-gate WPG SET. The complementary inverter consists of two 3-gate WPG SETs. In order to realize complimentary operation of the two SETs, the conductance peak positions must be adjusted. For this, voltage control by means of the tunnel-barrier-control WPGs was attempted, with success.

3. Fabrication Process

The fabrication process of WPG devices was very simple, as explained in the following. First, the GaAs nanowire with the channel width of 180 - 600 nanometers was formed by an electron beam (EB) lithography and wet chemical etching on an AlGaAs/GaAs heterostructure, using a standard sulfuric acid-based etchant. Next, source and drain ohmic contacts were formed by conventional Ge/Au/Ni deposition, a lift-off process and alloying. Then, nanometer-length Cr/Au Schottky wrap gates were formed on the GaAs nanowire by an EB-lithography-based standard lift-off process. The process included no special technique, thus this type of WPG device and circuit fabrication is suitable for high-density planar integration.

4. Results and Discussion

4.1 Characteristics of 3-gate WPG single electron transistor

To design and realize inverter circuits, an understanding of the basic characteristics of

the 3-gate WPG SETs is extremely important. Figure 2 shows an example of an scanning electron microscope (SEM) plan-view image of a fabricated 3-gate WPG SET. The trapezoidal cross section of the GaAs nanowires with very smooth side walls could be obtained when the wire direction was set to be in the $<\bar{1}10>$ direction. Typically, the nanowire width was 200 - 500 nm and the WPG gate length was 50 nm. The fabricated WPG devices showed conventional FET-like characteristics with excellent gate control from room temperature down to low temperatures.

The device showed clear conductance oscillations with a small number of peaks up to 20 - 30 K which can be explained by single electron lateral resonant tunneling through a single dot energy level with a large electron addition energy, as reported elsewhere[10)].

The Coulomb diamond plot of the 3-gate WPG SET is shown in Fig.3(a). The voltage gain, G_{SET}, which is important for inverters, was estimated from the plot by using the relation of $G_{SET} = \Delta V_{DS}/\Delta V_{CG}$, where V_{DS} is the source-drain voltage and V_{CG} is the dot-potential-control WPG voltage. The maximum gain value achieved in this study was 1.3. This is the highest value reported for III-V compound semiconductor-based SETs, and is acceptable for logic gate applications. On the other hand, the 2-gate WPG SETs shown in Fig.1(b) showed low voltage gain values of 0.2 - 0.3 from $\Delta V_{DS}/\Delta V_{BG}$, where V_{BG} is the tunnel-barrier-control WPG voltage. The observed high gain of the 3-gate WPG SET is due to the tight charge control and a large gate capacitance of the dot-potential-control WPG, as discussed previously[7)].

In order to obtain further information on favorable device size parameters for the construction of inverters, a theoretical estimation of the SET voltage gain for devices with different WPG sizes was made, using the simulation program developed previously[6)]. The results are summarized in Table I. Here, the theoretical voltage gain was calculated by

$$G_{SET} = C_G/C_D, \qquad (1)$$

where C_G and C_D are the gate and drain capacitance, respectively, whose values were estimated from the three-dimensional potential simulation. The result is in good agreement with the gain of the actual device in Fig.3(a). It was also found that higher voltage gains larger than unity can be obtained when the length, L_{CG}, of the dot-potential control WPG is long and the interval between WPGs, d, is narrow. On the other hand, the gain is not so sensitive to the width, W, of the nanowire.

Next, an attempt to control the conductance peak position by changing the gate voltage was made. The observed conductance oscillation characteristics of a fabricated 3-gate WPG SET are summarized in Fig.3(b) for different values of the gate voltage, V_{BG}, on the tunnel-barrier-control WPGs. For a fixed V_{BG}, clear conductance oscillations could be seen as

a function of V_{CG}. It was also found that by changing V_{BG}, the conductance peaks could be shifted systematically, as shown in Fig.3(c). This property is extremely useful for the realization of single electron complementary logic gates. The peak shapes and intervals remained almost the same with the change of V_{BG}. This is rather surprising at first, but can be understood as follows. After the regions under the barrier gate are depleted, the shape of the potential distribution near the barriers and the dot is kept almost the same, and moves up and down with the movement of the Fermi level in the dot. However, the Fermi level in the dot remains the same, if the following condition is satisfied.

$$C_{CG}V_{CG} + C_{BG}V_{BG} = n\,q + \text{const.}, \qquad (2)$$

where n is the number of electrons in the dot and q is the electron charge. The observed linear relationship in Fig.3(c) supports the validity of this interpretation.

4.2 Single electron inverter circuits

The resistive load single electron logic inverters were successfully designed and fabricated by simple arrangement of WPGs and GaAs nanowires, as shown in Fig.4(a). They had a 3-gate WPG SET as a driver SET and a WPG QWTr as an active load. The minimum WPG gate length was 50 nm. The circuit was realized by a simple fabrication process which was exactly the same as that for discrete SETs. A T-shaped connection between the nanowires was formed by wet chemical etching. Figure 4(b) shows the transfer characteristic of the fabricated resistive load inverter with a 3-gate WPG SET. By optimizing the WPG voltages, the transfer gain of 1.3 was obtained, where the voltage gain of the discrete SET with the same structure from the Coulomb diamond was 1.3. This is the first demonstration of a sufficiently large gain in III-V compound semiconductor-based single electron logic gates. Previous III-V semiconductor SET logic inverters showed gains of about 1/1000[11)]. The resistive load inverter with a 2-gate WPG SET as a driver SET was also fabricated and its transfer gain was 0.21. This value was also close to the voltage gain of the driver SET. The obtained high transfer gain of the inverter with the 3-gate WPG SET is concluded to be due to the high voltage gain of the driver SET itself.

An attempt was also made to realize a complementary logic inverter. An SEM micrograph of the fabricated circuit is shown in Fig.5(a). This inverter had two 3-gate WPG SETs. The input port was connected to the dot-potential-control WPGs of both SETs. The tunnel-barrier-control WPG voltages of each SET were changed independently in order to adjust the peak positions. Figure 5(b) shows the transfer characteristic of the fabricated WPG complementary inventer. A proper inverter operation could be seen upon adjusting V_{BG}. However, the measured transfer gain was 0.27. This small value of the transfer gain appears

to be due to small voltage gains of the driver SETs, since the L_{CG} was too short as seen in Fig.5(a). This most probably led to a smaller voltage gain as indicated by the simulation in Table I. Thus, it is expected that setting a suitable length of L_{CG} and the optimization of gate- and supply-voltages will enable the realization of a higher transfer gain of the complementary inverter.

On the other hand, for high-density integration of the logic gates for advanced system applications, the peak position adjustment without offset bias on the tunnel-barrier-control WPGs is required. In the 3-gate WPG SET, it can be realized by changing the threshold voltage with different nanowire widths, by changing the gate capacitance with different center WPG lengths, and by the choice of appropriate Schottky gate metals. These points will be investigated in the near future.

5. Conclusions

GaAs-based SETs and their logic inverters were successfully designed and fabricated by means of the Schottky WPG quantum wire and dot formation technology.

Three-gate WPG SETs showed voltage gains larger than unity due to tight dot-potential control of the center WPG. The conductance peak position of the SET was systematically controlled by changing the tunnel-barrier-control WPG voltages.

A resistive-load single electron inverter utilizing a 3-gate WPG SET as a driver and a WPG quantum wire transistor as an active load showed a proper inverter operation, and a logic transfer gain of 1.3 was obtained at 1.6 K which is the highest value reported in III-V semiconductor-based SET inverters. A complementary inverter utilizing two 3-gate WPG SETs was also successfully fabricated using the voltage tunability of the peak positions and the proper inverter operation was obtained at 1.7 K.

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Figure captions

Fig.1 Schematic views of (a) a basic WPG structure, (b) a 2-gate WPG SET, (c) a 3-gate WPG SET, (d) a resistive load inverter and (e) a complementary inverter.

Fig.2 SEM micrograph of the 3-gate WPG SET.

Fig.3 (a) Coulomb diamond plot, (b) conductance oscillation characteristics, and (c) conductance peak positions of the 3-gate WPG SET.

Fig.4 (a) SEM micrograph and (b) transfer characteristics of the WPG resistive load logic inverter.

Fig.5 (a) SEM micrograph and (b) transfer characteristics of the WPG complementary logic inverter.

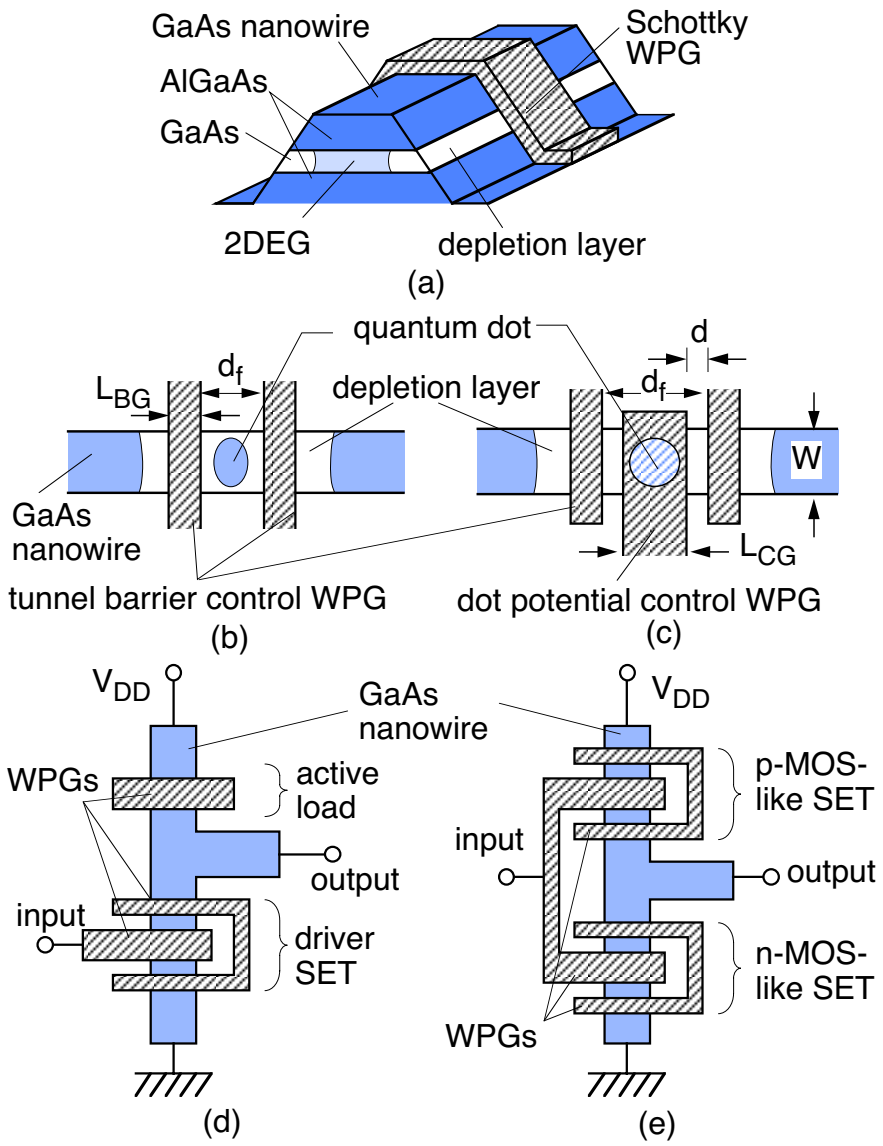


Figure 1, S. Kasai et al.

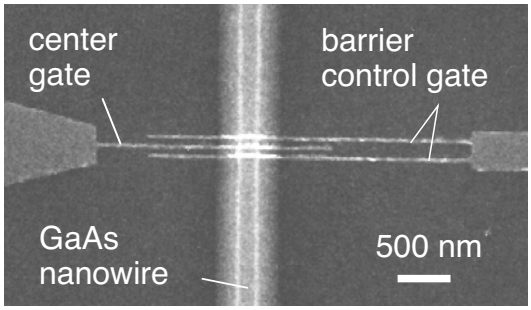
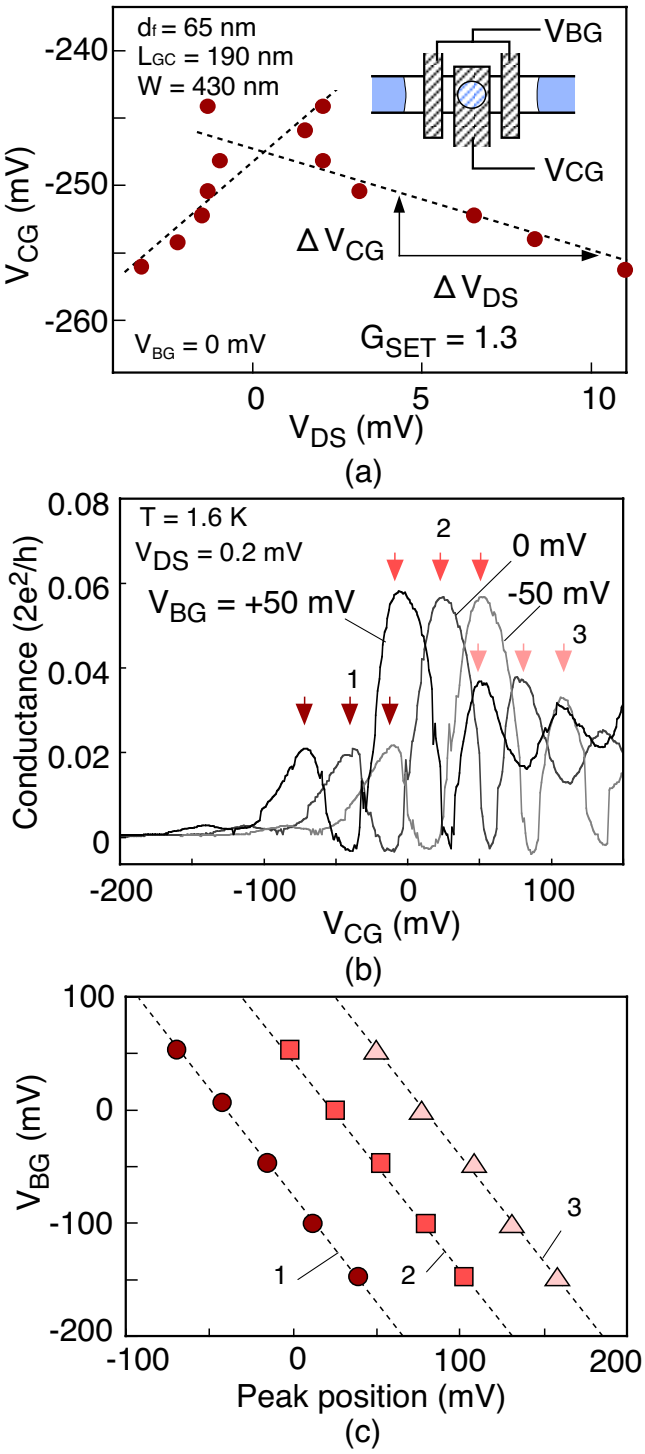


Figure 2, S. Kasai et al.



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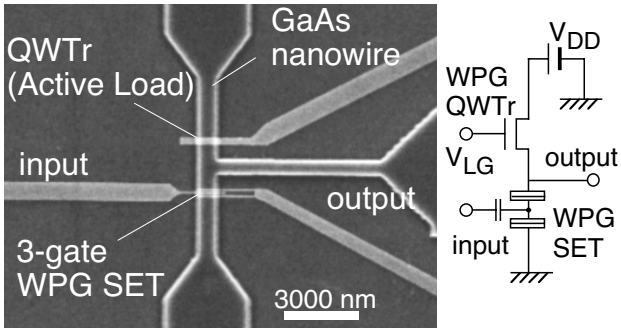
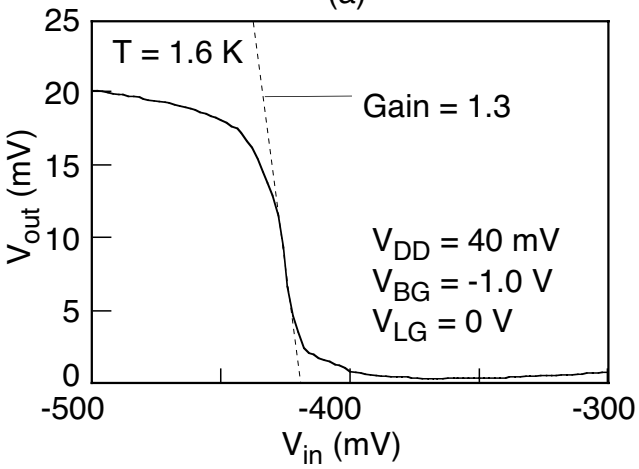


(a)



(b)

Figure 4, S. Kasai et al.

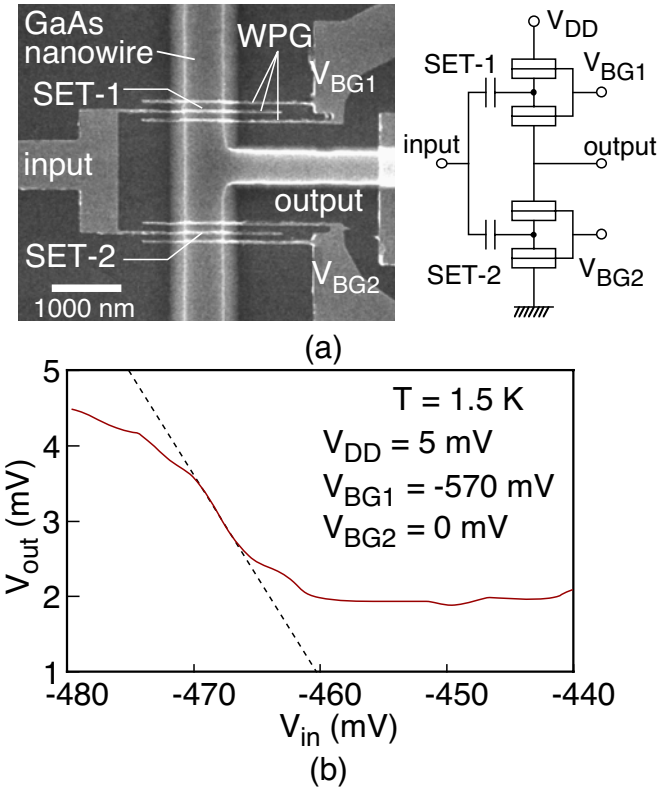
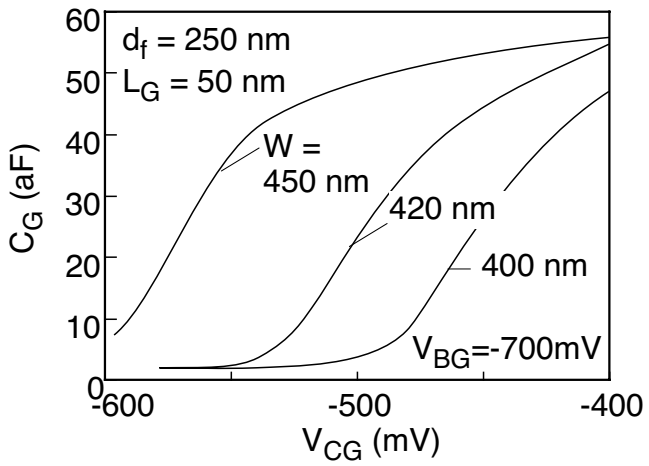
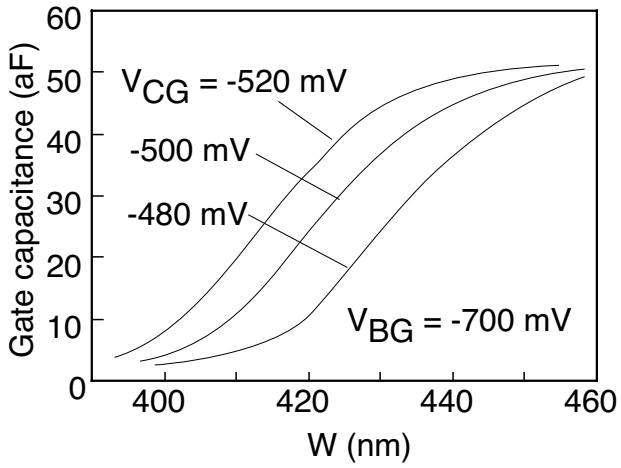


Figure 5, S. Kasai et al.

Table I. 3-gate WPG SET voltage gain (theory).

L_{CG} (nm)	d (nm)	W			
		400 nm	420 nm	430nm	450 nm
50	100	0.52	0.52	-	0.52
50	50	0.66	-	-	0.60
150	50	1.65	-	-	1.58
190	65	-	-	1.50	-


60
50
40
30
20
10
0
C_G (aF)
d_f = 250 nm
L_G = 50 nm
W =
450 nm
420 nm
400 nm
V_{BG}=-700mV
-600
-500
-400
V_{CG} (mV)


60
50
40
30
20
10
0
Gate capacitance (aF)
V_{CG} = -520 mV
-500 mV
-480 mV
V_{BG} = -700 mV
400
420
440
460
W (nm)