Fabrication and Characterization of A Novel Lateral Surface Superlattice Structure Utilizing Schottky Barrier Height Control by Doped Silicon Interface Control Layers

Seiya Kasai and Hideki Hasegawa

Research Center for Interface Quantum Electronics and
Graduate School of Electronics and Information Engineering,
Hokkaido University, Sapporo 060, Japan

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A novel lateral surface superlattice (LSSL) device structure based on Schottky barrier height (SBH) difference produced by periodic insertion of Si interface control layer (Si ICL) stripes is proposed, fabricated and characterized.

Two-dimensional computer simulation was performed first to gain

information on basic design considerations. An electron beam induced current (EBIC) study on the fabricated device directly confirmed SBH modulation by Si ICL stripes. The devices showed periodic oscillations of drainconductance and transconductance at low temperatures up to 10K whose behavior was distinctly different from that of previous split-gate devices. The mechanism of these oscillations was explained by a sequential resonant tunneling model. According to a quantitative analysis of the data, SBH difference of 70-150meV was produced at the metal-semiconductor interface and it produced quantized levels with the separation of 2-3meV at heterointerface.

KEYWORDS: lateral surface superlattice, Si interface control layer, Schottky barrier, electron beam induced current, conductance oscillation.

1. Introduction

Recently, a number of quantum devices are realized on compound semiconductors by utilizing the so-called split-gate structure. One of them is the so- called lateral surface superlattice (LSSL) which is practically interesting because it has a planar geometry and is expected to be capable of producing useful negative differential resistance (NDR) characteristics at extremely high frequencies extending into THz region.[1,2] The basic operation is based on the negative mass effect by mini-band formation in the periodical potential. A number of attempts have already been made to realizing split-gate type LSSLs.[3-5]

In the split-gate structure, modulation of the confinement potential for the two dimensional electron gas (2DEG) at the heterointerface is achieved through the surface potential difference on its top surface. Namely, the surface potential underneath a Schottky metal is usually higher for electrons than on the free surface, and this difference is utilized. However, it is well known that a large amount of surface states

exists on the free surfaces of GaAs and related materials. These states not only reduce the potential difference through Fermi level pinning but also tend to make the device design and performance complex, unstable and irreproducible.

An alternative approach is either to modulate the surface-to-2DEG distance [6] or to modulate the Schottky barrier height (SBH). Unfortunately, the former requires large thickness variations to achieve significant potential modulations, and the latter is known to be difficult due to so-called Fermi level pinning phenomenon. In this regard, however, our group has reported recently that the SBH of compound semiconductor Schottky barriers can be changed over a wide range of a few hundred meV by inserting silicon interface control layer (Si ICL) with suitable thickness and doping. [7-9]

The purpose of this paper is to propose, and fabricate and characterize a novel LSSL structure which utilizes the technique of SBH control by doped Si ICLs. In the novel structure, the periodic modulation of the potentials is created at the surface by lateral arrangement of

Schottky barriers having different SBH values and it gives rise to potential modulation at the heterointerface. The surface is totally covered by metal and operates as the gate. As compared with the split-gate structure it can produce larger variation of potential at the heterointerface. It also enables one to avoid the complexity and uncertainty of the air-exposed free surface of the semiconductor.

In this paper, the structure and basic design of the novel LSSL are presented and discussed first. Next, the fabrication process is introduced. Then the results of the characterization of the novel structure by electron beam induced current (EBIC) measurements and current-voltage measurements at low temperature are presented and finally the current transport mechanism for observed oscillations of transconductance and drainconductance is discussed.

2. Novel LSSL Structure and Its Basic Design

2.1 Structure of novel LSSL

The structure of the novel LSSL devices is shown in Fig.1. As shown in Fig.1(a), its plan view has an standard field-effect transistor (FET) structure with a gate length, L_g, and a gate width, W_g, except for the grating gate region whose cross-sectional view is shown in Fig.1(b). This is the essential part of the device, and here potential modulation is produced by SBH control by doped Si ICL stripes which are periodically inserted with a period of a at the top metal-semiconductor (M-S) interface of a conventional AlGaAs/GaAs modulation doped structure with a surface to 2DEG distance, D, and the doping of the carrier supply layer, N_D.

Figure 2 shows the basic concept of the SBH control by doped Si ICL layers for metal/n-GaAs system which was previously reported by our group.[7-8] It is well known that the Fermi level at the M-S interface of GaAs is firmly pinned, making the SBH of n-GaAs always remain in the range of 800~900meV independent of the metal workfunction as shown in Fig.2(a). However, by inserting a Si ICL with the thickness

t_{ICL} doped with high concentration of donors or acceptors at the M-S interface, strong doping dipoles are created at the interface and SBH values are modified, although the Fermi level at metal/Si ICL interface is firmly pinned. The band diagram for the case of SBH reduction on n-type GaAs by Si ICL doped with donors is shown in Fig.2(b). The Si ICL needs to be very thin, being a few nm, so that it retains psedomorphic matching with GaAs and that no Fermi level pinning takes place at the Si ICL/GaAs interface. It should be highly doped in the range of $10^{20}cm^{-3}$ to produce strong dipoles within a thin thickness. According to previous experiments, the SBH of Al/Si ICL/n-GaAs Schottky barriers could be changed systematically over 200meV with As dopeing.[7,8)]

Therefore, inserting doped Si ICL stripes with SBH=f_{Bn1} periodically at n-GaAs Schottky interface with SBH=f_{Bn2} without Si ICL, periodic square-wave modulation of potential between f_{Bn1} and f_{Bn2} should be created at the top surface of the structure, which then modulate potential at the AlGaAs/GaAs heterointerface as shown in Fig.1 (b).

2.2 Basic design considerations

In order to have ideas about the relationships among the surface potential difference, Df_{Bn}, at the top M-S interface, the modulation shape and amplitude of potential at the heterointerface and the quantum states resulting from potential modulation, we performed two-dimensional potential calculation for the present LSSL structure. The Poisson's equation was solved numerically using a finite difference method. Use of the successive over relaxation (SOR) method realized quick convergence of the solution.

Figure 3(a) shows an example of calculated potential at heterointerface for the present LSSL having two different SBH values of 800meV and 600meV with respect to GaAs cap layer. As for dimension and doping, a=200nm, D=55nm and $N_D=1x10^{18}cm^{-3}$ were used. Although the surface potential at M-S interface varies in a square-wave fashion, the result of calculation in Fig.3(a) shows that the shape of the

potential at heterointerface quickly becomes sinusoidal due to long range isotropic nature of the Coulomb force. It is also seen that both of the full amplitude of the sinusoidal potential modulation V_0 and Fermi level position E_F with respect to the edge of GaAs conduction band, E_C, vary very much with the gate bias. In order to clarify possible differences in potential distribution with the split-gate device, a similar calculation was made for the latter with the same dimensions and doping. The result is shown in Fig.3(b). Here, a SBH of 800meV at M-S interface and presence of uniform surface states density of $1.2 \times 10^{12} cm^{-2} eV^{-1}$ at the free semiconductor surface were assumed. The Fermi level position at the free surface was determined self-consistently in this calculation. As seen in Fig.3(b), the potential shapes are sinusoidal as in Fig.3(a), but, only the amplitude is changed largely by gate bias, and the Fermi level position varies much less in the case of the split-gate structure.

Figure 4(a) summarizes the calculated energy positions of the potential maximum E_{Cmax} and minimum E_{Cmin} at heterointerface for the same LSSL device shown in Fig.3(a). The result is given in terms of

GaAs conduction band edge position with respect to the Fermi level E_F as a function of gate bias. As seen in Fig.4(a), Fermi level moves quickly with gate bias and the amplitude of the potential modulation V_0 ($=E_{Cmax} - E_{Cmin}$) becomes larger with decrease of gate bias.

It is also desirable to have a rough idea about the quantized states formed by potential modulation. Since the effect of level broadening by mini-band formation is expected to be small for the period of a few hundred nm, we estimated the energy separation ΔE, of subbands applying harmonic potential approximation to the sinusoidal potential. The calculated relationship between the potential difference $\Delta f_{Bn}=f_{Bn2}-f_{Bn1}$ at M-S interface and the level spacing ΔE is shown in Fig.4(b) for the same device shown in Fig.3(a) except for changing f_{Bn1} keeping f_{Bn2} constant. The effect of changing a from 200nm to 300nm is also shown. We see that using quantized levels with spacings of a few meV should be realized with Δf_B of a few hundred meV. Rigorously speaking, the spacing of the levels decreases towards higher energies because of the sinusoidal shape, but its effect was found to be very small by a rigorous

numerical analysis.

3. Fabrication of Novel LSSL

The fabrication process of the LSSL device consisted of five major steps. They are;

(1) MBE growth of $Al_{0.3}Ga_{0.7}As$/GaAs heterostructure wafer,

(2) MBE growth of Si ICL and formation of Al Schottky barrier,

(3) formation of an H shaped mesa island by chemical etching,

(4) formation of source and drain ohmic contacts and

(5) formation of the grating gate.

Figure 5 shows the sequence for formation of the grating gate which is the essential part of the present LSSL. First, the basic starting structure for fabrication of the LSSL shown in Fig.5(a) was grown by the above steps (1) and (2), using an ultra high vacuum (UHV)-based system including a molecular beam epitaxy (MBE) chamber and a metal deposition chamber connected with an UHV transfer chamber. The n^+-

AlGaAs layer had a thickness of 50nm and Si doping of $1x10^{18}cm^{-3}$. The doped Si ICL grown by MBE at the substrate temperature of 250¡C had a thickness of t_{ICL}=2nm and an estimated As doping of $3x10^{20}cm^{-3}$. As doping was done by irradiation of As flux during growth of the Si ICL. The film of Al metal layer had a thickness of 40nm deposited in UHV on the Si ICL.

After formation of the starting structure described above, the sample was taken out to the air and the steps (3) and (4) were carried out. Ni/Ge/Au ohmic electrodes were formed as the source and drain. Then, in the final step (5) of grating gate formation, the Al film and Si ICL was periodically removed by using electron beam lithography and wet chemical etching as shown in Fig.5(b). Then, the second Al metal was deposited over the whole wafer as shown in Fig.5(c) and finally the gate electrode pattern was defined by photolithography and wet etching.

We fabricated and characterized four samples, A, B, C and D, having nominally the same structure and dimensions. The period a of the grating gate was chosen to be a=200nm. Macroscopic gate dimensions

were L_g=14μm and W_g=54μm, respectively. Out of four samples, the sample A was used for SEM/EBIC study in a destructive fashion and the samples B, C and D for electrical characterization.

4. Characterization of Novel LSSL

4.1 SEM/EBIC study

The plan-view SEM images of the grating gate are shown in Fig.6. Figure 6(a) shows electron-beam resist pattern before etching of the first Al layer, and the plan-view after deposition of the second Al layer is shown in Fig.6(b). The entire surface is covered by Al in Fig.6(b), but the periodicity of 200nm can still be recognized. Here, bright and dark regions corresponded to the region of Al Schottky contact with Si ICL and the region of direct Al Schottky contact without Si ICL, respectively.

Figure 7 (a) and (b) show the cross-sectional SEM and EBIC images taken on the cleaved surface of under the grating gate region of sample A.

The corresponding schematic illustration of the EBIC image is also shown. In the EBIC measurement, an electron beam is irradiated on the cleaved surface of sample A, and the generated carriers were detected as a current in an external circuit.[10] This measurement was found to be extremely powerful for investigation of the potential in nanometer-scale structures.[11] In our EBIC system, the lateral resolution was estimated to be about 50nm at the electron beam energy of 10kV. Thus, if there is any potential modulation in the present sample, it should be detectable.[9]

As shown in Fig.7(b), the EBIC image exhibited a clear periodic pattern. The periodic pattern had the same period with the fabricated grating structure, whereas no such pattern was observed in the SEM image in Fig.7(a). The periodic signal pattern are located at the M-S interface region, and it was confirmed that the dark and bright regions in the image corresponded to the M-S interfaces with and without As doped Si ICL, respectively. Since brighter regions correspond to regions with higher electric fields, the observed EBIC image indicates that the M-S interface region without doped Si ICL should posses higher fields than

those with Si ICL. Thus, the EBIC study directly confirmed that periodic variation of electrostatic potential in nanometer scale could be produced at the M-S interface by doped Si ICL stripes whose thickness is only 2nm.

4.2 Drainconductance oscillation

The fabricated LSSL devices showed reasonably good field-effect performance on a macroscopic scale as seen in drain current - drain voltage (I_{DS}-V_{DS}) characteristics of sample B shown in Fig.8(a). Here, V_G denotes the gate-to-source voltage. However, periodic occurrence of dips are also recognized in the I_{DS}-V_{DS} characteristic in Fig.8(a). The presence of dips are more clearly revealed in terms of the drainconductance g_D (=¶I_{DS}/¶V_{DS}) as shown in Fig.8(b) where oscillatory behavior of drainconductance is observed with the increase of V_{DS}. The period is of the order of a few hundred meV, but its values changes strong with V_G. Similar drainconductance oscillation was also

observed in samples C and D.

4.3 Transconductance oscillation

Measurement of the transconductance was made under extremely small drain voltage V_{DS}, so that the effect of electric field in the direction of electron transport becomes negligible. Figure 9(a) and (b) show the measured gate-voltage dependence of transconductance g_m (=$\P I_{DS}/\P V_G$) near the threshold voltage (V_{th}) of the channel pinch off for samples C and D. The observed characteristics are complex, but, again periodic occurrence of dips pattern can be clearly observed as indicated by dashed lines in Fig.9. The periods of the dips were determined by Fourier transformation and found to be independent of the drain voltage V_{DS} in both samples. The periodicity was about 2meV and 4meV for sample C and D, respectively.

4.4 Temperature dependence of transconductance

Figure 10(a), (b) and (c) show the observed temperature dependence of the transconductance of sample D. In this measurement, relatively large values of V_{DS} were used, and this resulted in more complex pattern than that for low V_{DS}. As seen in Fig.10(a), at 2.5K, the transconductance oscillation structure was clearly observed. At 10K, the shape of the oscillation pattern remained more or less the same, but the oscillation amplitude became smaller. On the other hand, the oscillation completely vanished at 77K. This temperature dependence suggests that the observed transconductance oscillation due to quantum effects.

5. Discussion

The fabricated novel LSSL devices showed consistently oscillatory behavior in their drainconductance and transconductance at low temperatures up to 10K. The origin of the observed two kinds of oscillatory behavior can be explained in terms of the sequential resonant

tunneling model shown in Fig.11, as suggested previously for split-gate LSSL devices.[4] Namely, the periodic variation of the potential results in the formation of multiple quantized levels shown in Fig.11 with possible formation of narrow mini-bands. Since the period of the potential in the present device is longer than the Fermi wave length and the scattering length, most of the current flows either by inelastic tunnelling or thermal excitation process. However, we assume that part of electrons do not loose phase information and are transported through the sequential resonant tunneling process.

Then, the transconductance oscillation can be explained as follows according to Fig.11(a). As the V_{DS} was sufficiently low in the I_{DS}-V_G measurement, the position of each quantized level in neighboring wells aligns horizontally as shown in Fig.11(a). The Fermi level (E_F) also aligns horizontally and its position is controlled by V_G. Sweeping V_G, the sequential tunneling takes place only when E_F agrees with one of the quantized levels with possible small broadenings. If such a condition is not met, the resonant tunneling process is prohibited, and the current

produces a dip. Then the conductance changes periodically by sweeping V_G, resulting in the transconductance oscillation.

On the other hand, the drainconductance oscillation can be explained by Fig.11(b). Since measurements were performed under high V_{DS} condition, it is now possible that one quantized level in one well aligns with other quantized level in the neighboring wells in a staggered fashion as shown in Fig.11(b). The sequential resonant tunneling takes place with energy loss and it occurs when the amount of the loss is equal to integral multiple of the energy separation of the quantized levels. Thus, drainconductance oscillation can be observed by sweeping source drain voltage.

On the basis of the above qualitative explanation, one could make a more quantitative discussion. A remarkable feature of the observed transconductance oscillation in Fig.9(a) and (b), is occurrence of regular periodic oscillation with a small gate voltage period of a few mV. In contrast to this, previous split-gate LSSL devices showed more nonuniform and larger periods of gate voltages of about 8-15mV for the

same value of a=200nm.[3] This difference can be understood in terms of the difference in the E_F-V_G relation discussed earlier in Section 2.2. As compared with split-gate device, the present device changes E_F-E_{Cmin} more rapidly with V_G, and the relation becomes remarkably linear near pinch-off as seen in Fig.4(a). Thus, regular occurrence of dip in Fig.9(a) and (b) can be understood in terms of linear sweep of Fermi level though equally spaced quantized levels. Then, using the relation of

, (1)

where $ÆV_{Gdip}$ is the gate voltage period of g_m dip, and the values of $(¶E_F/¶V_G)_{near\ pinch\ off}$ Å 0.7, one can obtain the estimated values of ÆE as shown in Table I from the observed values of $ÆV_{Gdip}$.

On the other hand, in the case of drainconductance oscillation, ÆE should satisfy the following relation, on the basis of the model in Fig.11 (b).

$$ÆE \sim qÆV_{DSdip} \text{ á } a / L_g = qÆV_{DSdip} / \text{finger}, \quad (2)$$

where $ÆV_{DSdip}$ is the period of the drainconductance oscillation. Here, it is assumed that the electric field under the gate is uniform. Since the drainconductance oscillation was observed in the saturation region, there is a possibility that *Æ*E may be overestimated due to electric field concentration near drain region. However, as the estimation of *Æ*E from the drainconductance was done in this study by using the I-V curves near the drain current pinch-off, where the channel under the gate is almost uniformly near pinch-off and such concentration of electric filed near the drain does not seem to be large. According to Fig.8(a), the observed periodicity $ÆV_{DSdip}$ of the oscillation decreased rapidly with the increase of the gate voltage. Such a large change of periodicity with gate bias has not been observed in the previously split-gate type devices.[4,5] This difference can also be explained by the difference in the gate control characteristic. Namely, as seen in Fig.3 and Fig.4(a), the potential

amplitude is more sensitively changed in the present device than the split-gate device. The amplitude of the potential modulation, V_0, at the heterointerface changes more rapidly with increase of V_G in the present device. Reduction of V_0 with V_G reduces ÆE and then, reduces V_{DSdip} according to Eq.(2).

To make comparison with the value of ÆE from transconductance oscillation, ÆE was estimated from the drainconductance oscillation near pinch-off, using Eq.(2). The result is given in Table I. The difference of the SBHs (Æf$_B$) estimated from the values of ÆE using Fig.4(b) is also included in Table I. As seen in Table I, agreement between two values of ÆE is good, showing the consistency of the interpretation given here. On the other hand, further work is necessary to understand the detailed complex patterns and the amplitudes of transconductance oscillation. Such a work may reveal detailed features of quantum transport including density of states in mini-bands. The remarkable linear E_F-V_G relationship in the present device suggests that it may be used as a spectrometer for quantum transport in LSSL devices. Such application is

difficult for the split-gate structure because the highly nonlinear and complex relationship between ÆE, the Fermi level position and V_G.[12)]

As regards the SBH control capability achieved by Si ICL stripes in the present study, the value of Æf_B is estimated to be Æf_B=70~150meV as shown in the Table I. These values are well consistent with the clear contrast of the EBIC image shown in Fig.7(b). The estimated value of Æf_B is somewhat smaller than the expected value of Æf_B=200meV, but not unlikely because it can be very much affected by the details of Si ICL processing and metal deposition.

6. Conclusion

A novel LSSL device structure based on Schottky barrier height (SBH) control with Si interface control layers (Si ICL) was proposed and fabricated. The main conclusions are listed below:

(1) Basic design considerations were given by 2D computer simulation of potential.

(2) The appearance of periodic EBIC signal directly confirmed SBH modulation by Si ICL stripes.

(3) Marked periodic oscillations of drainconductance and the transconductance were observed at low temperatures up to 10K. Their detailed behavior was distinctly different from that of previous split-gate devices.

(4) The mechanism of these oscillations can be explained by the sequential resonant tunneling model. A quantitative analysis of the data indicated that SBH difference of 70-150meV was produced, which produced quantized levels with the separation of 2-3meV at heterointerface.

Acknowledgement

The authors would like to express their sincere thanks to Dr. T. Hashizume for helping us with EBIC measurements. The present research is financially supported in part by a Grant-in-Aid for Scientific Research

(General Research B, No.07455017) from the Ministry of Education, Science and Culture.

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Figure captions

Figure 1. The structure of the novel LSSL. (a) the plan-view. (b) the cross-sectional view of the grating gate.

Figure 2. The band diagrams of metal/n-GaAs system (a) without Si ICL and (b) with doped Si ICL.

Figure 3. Calculated potentials at heterointerface (a) for the novel LSSL and (b) for a conventional periodic split-gate LSSL.

Figure 4. (a) The calculated potential at heterointerface of the novel LSSL as a function of V_G. (b) The calculated *Æ*E as a function of SBH difference, *Æ*f_B, for different periodicity of the grating gate.

Figure 5. The fabrication process of the LSSL device.

Figure 6. SEM images of (a) the resist pattern of the grating gate and (b) after the final metalization.

Figure 7. The cross sectional (a) SEM and (b) EBIC images of sample A.

Figure 8. (a) I_{DS}-V_{DS} characteristics and (b) drainconductance of sample B.

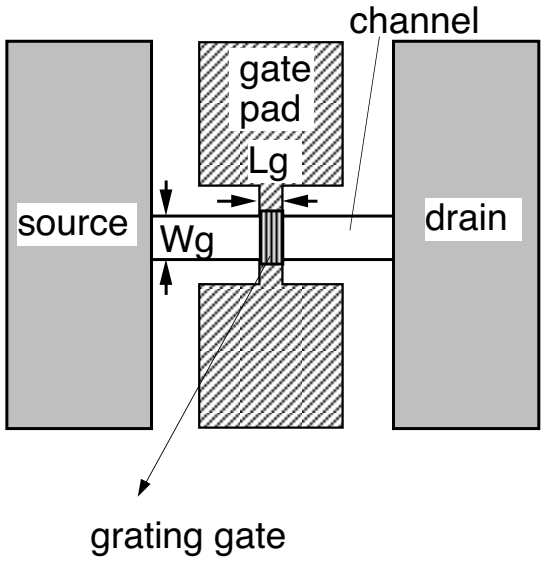
Figure 9. The transconductance characteristics for (a) sample C and (b)

sample D.

Figure 10. The temperature dependence of the transconductance oscillation of sample D.

Figure 11. Sequential resonant tunneling model for the observed oscillations of (a) transconductance and (b) drainconductance.

Table I. Estimated *Æ*E from the transconductance and drainconductance oscillations, and estimated *Æ*f_B.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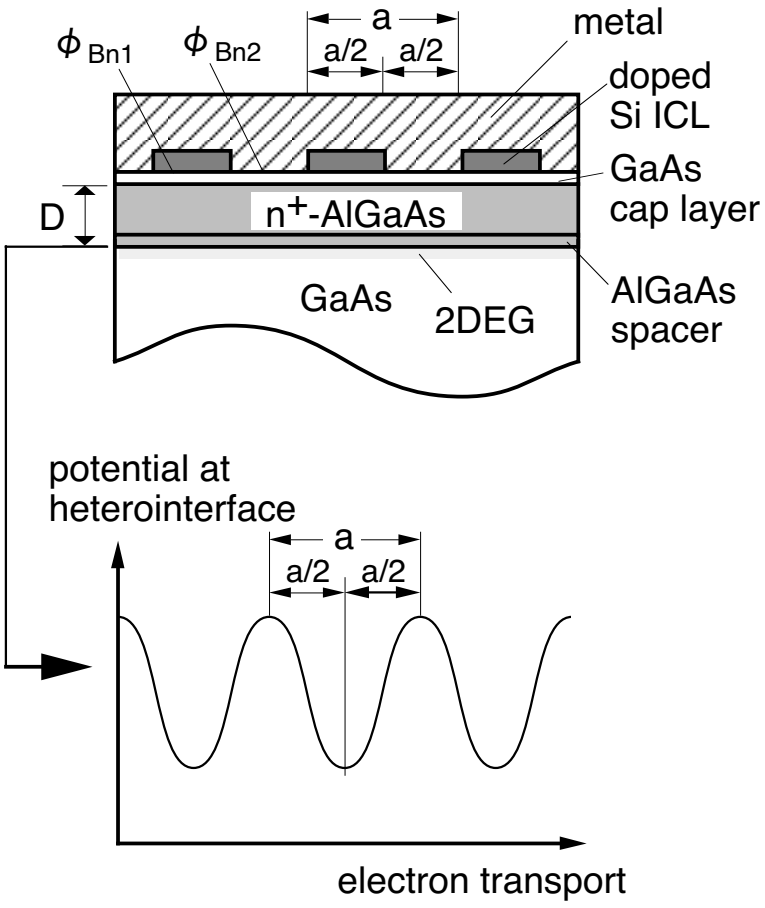
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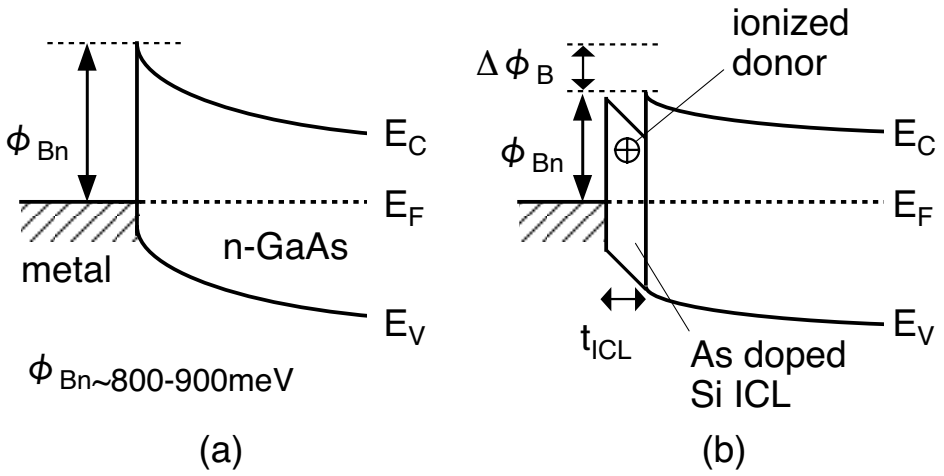
(b)

Figure 1.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t_{ICL}
As doped
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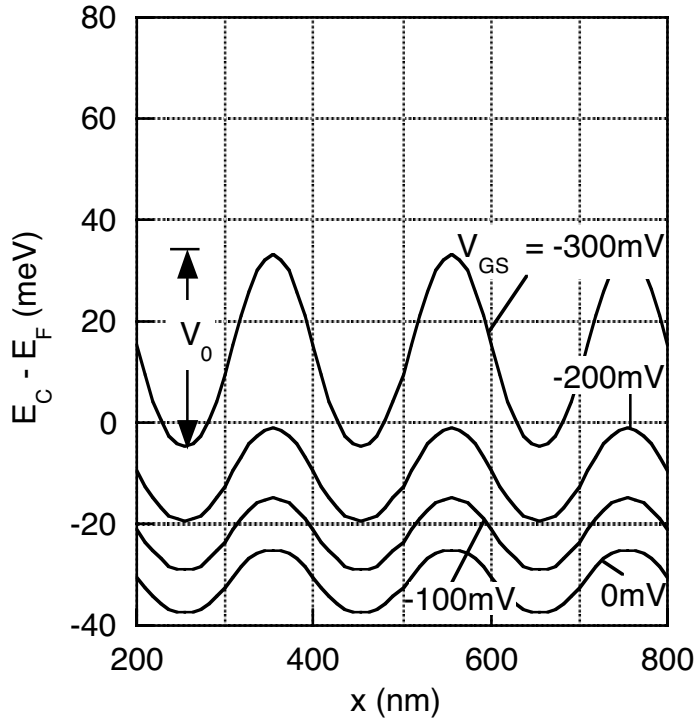
(b)

Figure 2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V_GS = -300mV
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-100mV
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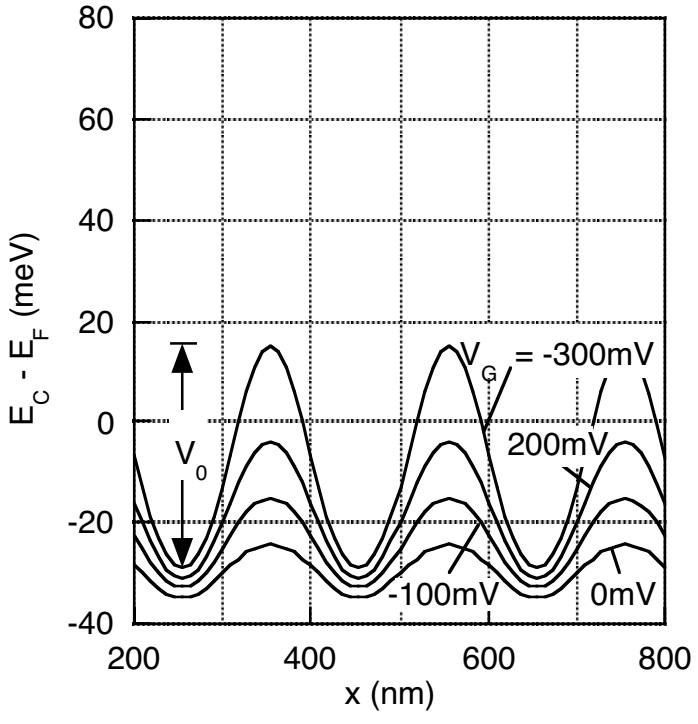
(a)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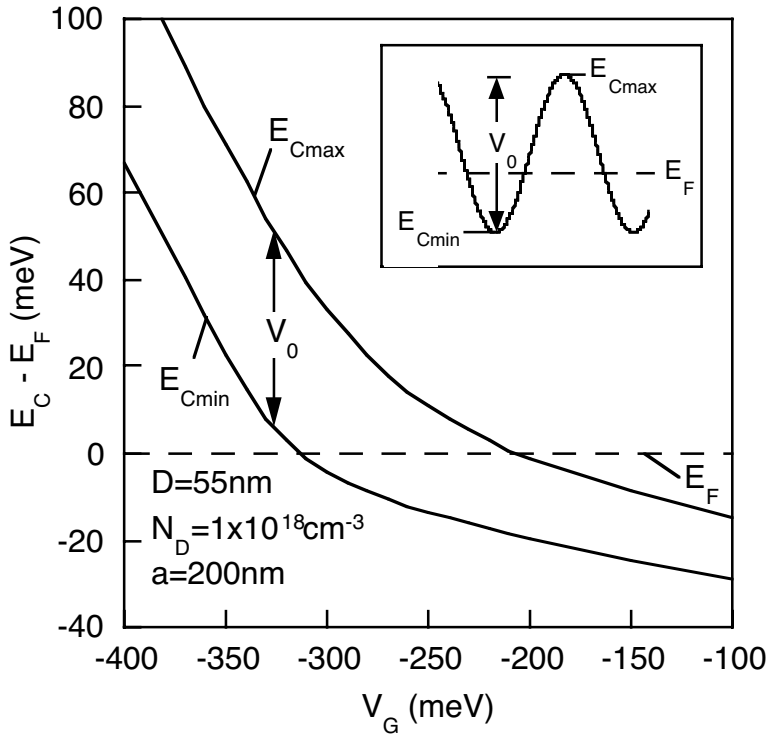
200mV
-100mV
0mV

(b)

Figure 3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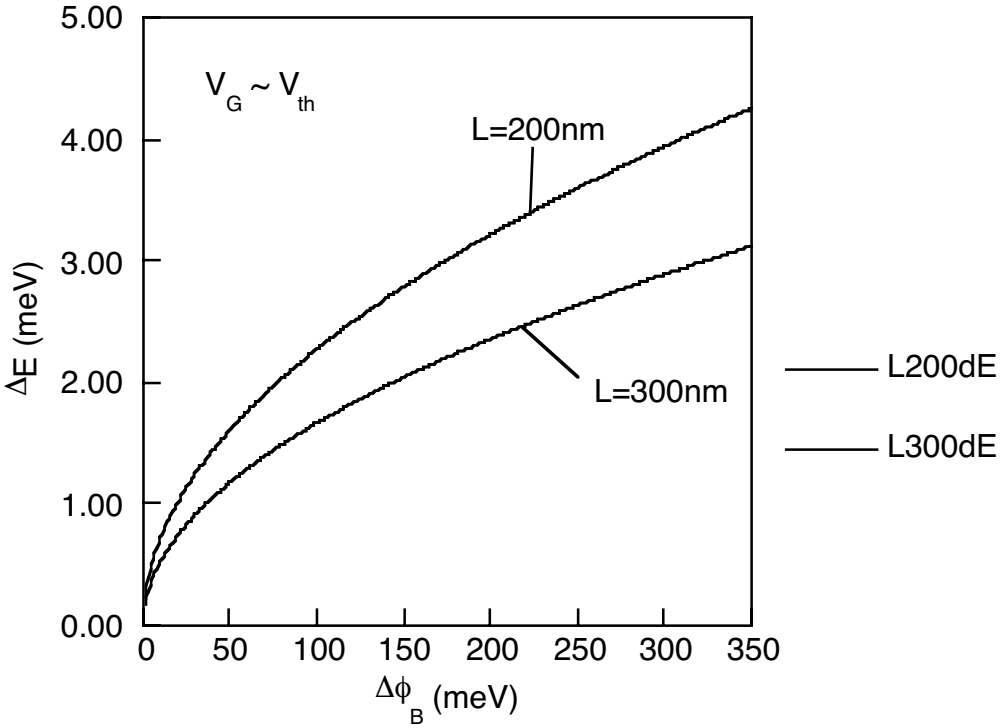
V_G (meV)
E_Cmax
E_Cmin
V_0
E_F
D=55nm
N_D=1x10^18cm^-3
a=200nm

(a)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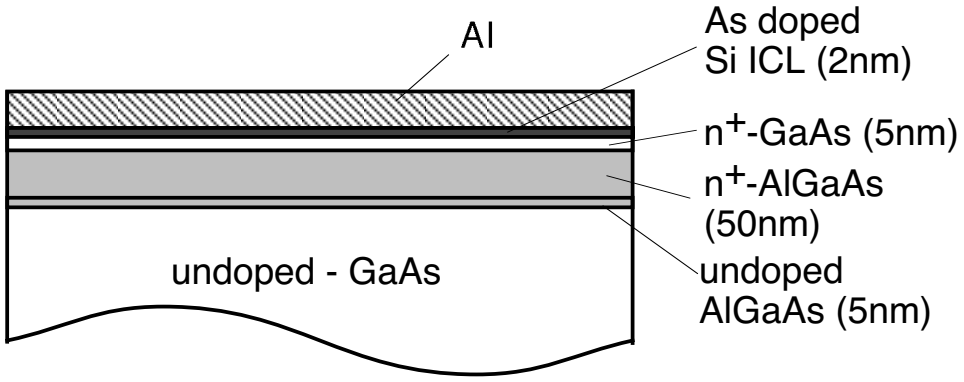
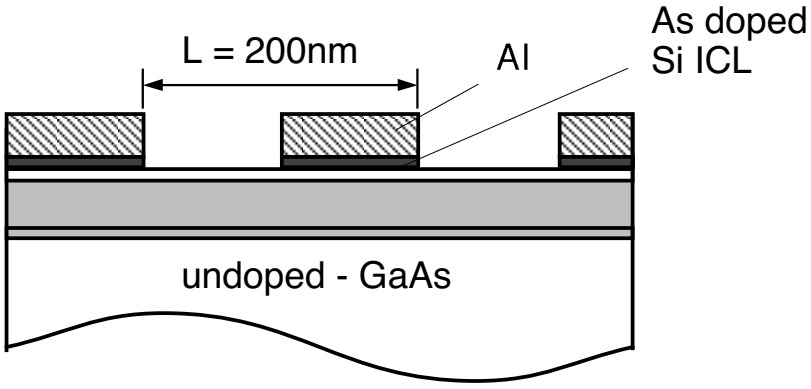
ΔE (meV)
Δφ_B (meV)
V_G ~ V_th
L=200nm
L=300nm
L200dE
L300dE

(b)

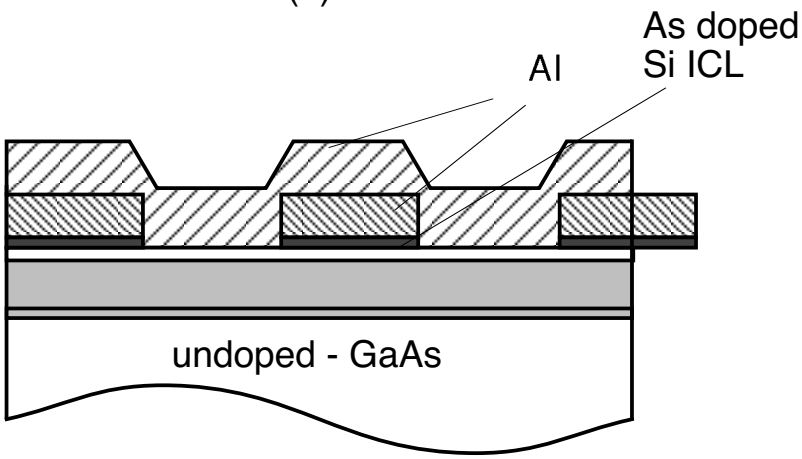
Figure 4


Al
As doped
Si ICL (2nm)
n+-GaAs (5nm)
n+-AlGaAs
(50nm)
undoped - GaAs
undoped
AlGaAs (5nm)

(a)

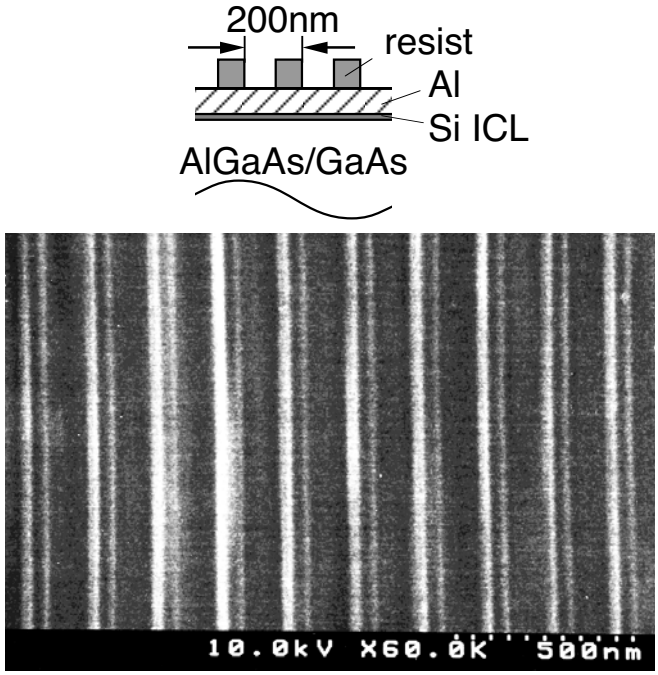

L = 200nm
Al
As doped
Si ICL
undoped - GaAs

(b)

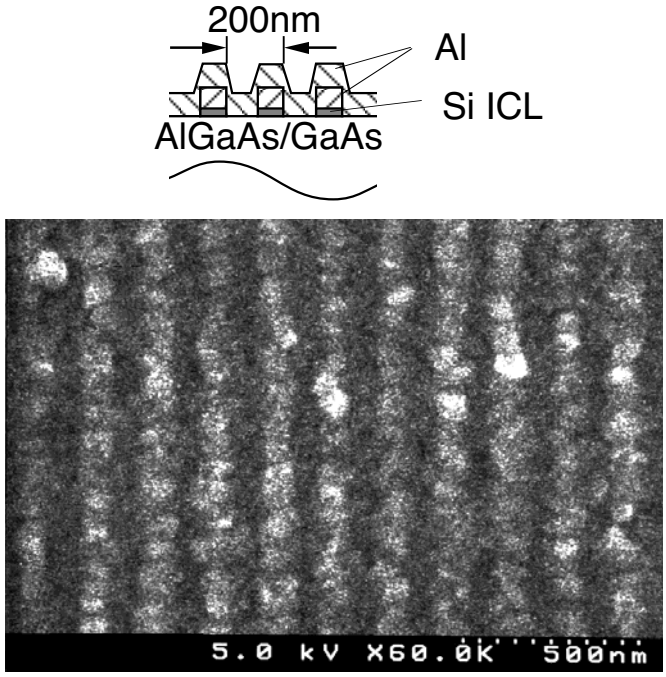

Al
As doped
Si ICL
undoped - GaAs

(c)

Figure 5

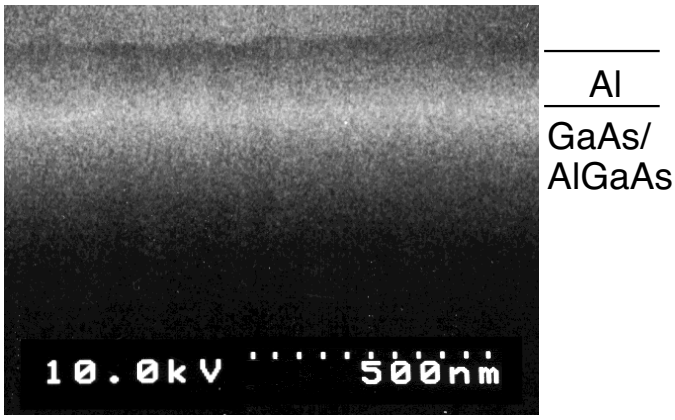

200nm
resist
Al
Si ICL
AlGaAs/GaAs
10.0kV X60.0K 500nm

(a)

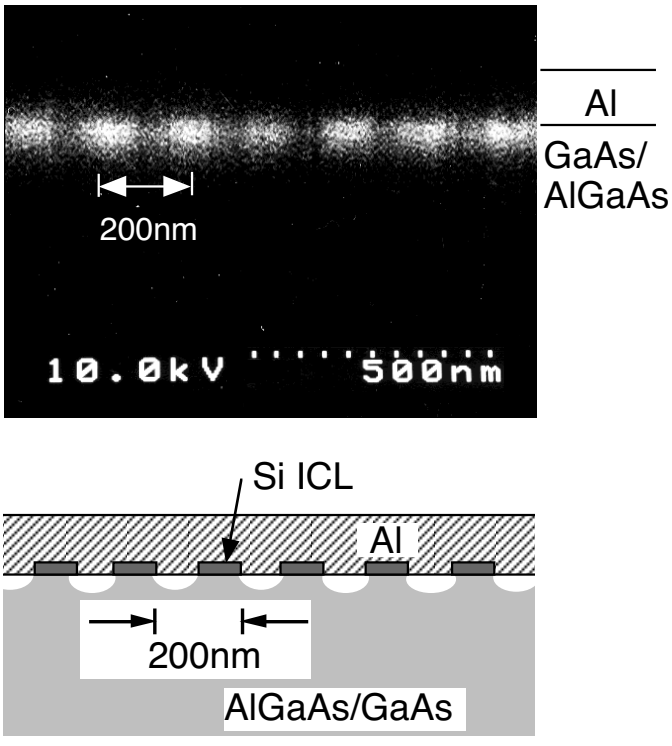

200nm
Al
Si ICL
AlGaAs/GaAs
5.0 kV X60.0K 500nm

(b)

Figure 6

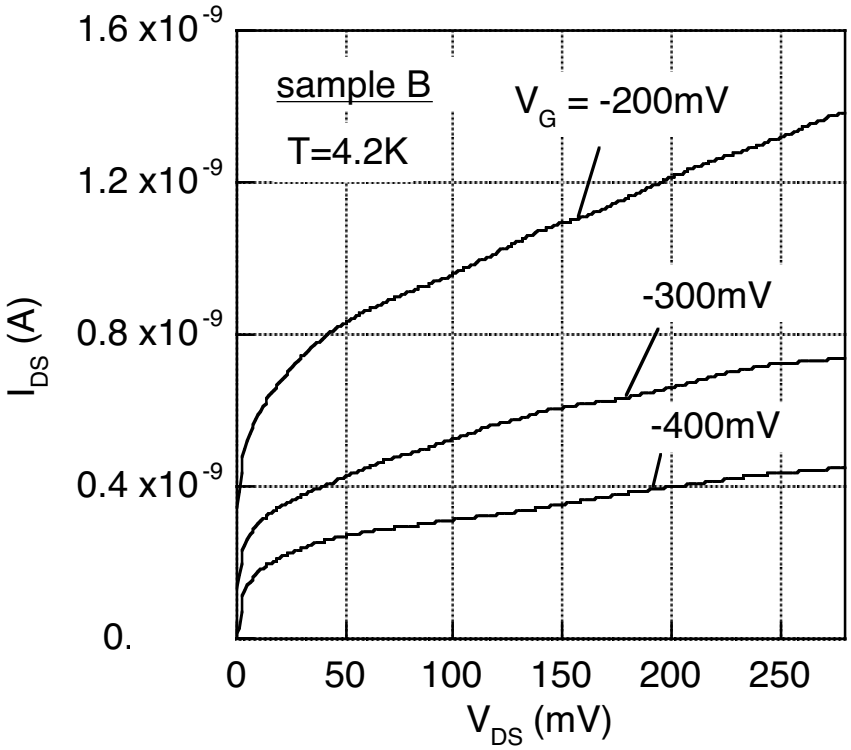

Al
GaAs/
AlGaAs
10.0kV
500nm

(a)

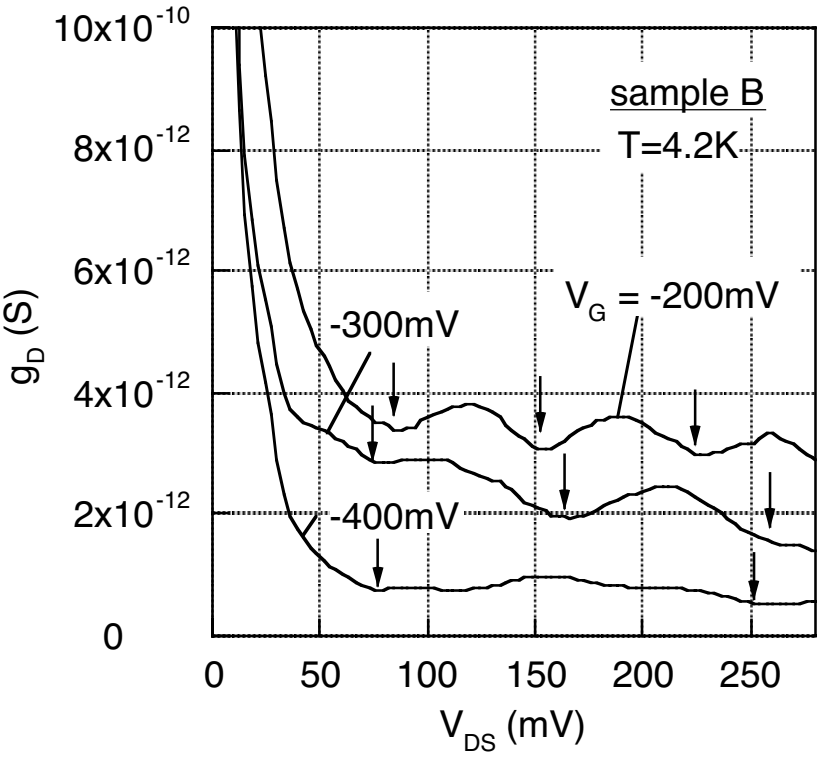

Al
GaAs/
AlGaAs
200nm
10.0kV
500nm
Si ICL
Al
200nm
AlGaAs/GaAs

(b)

Figure 7

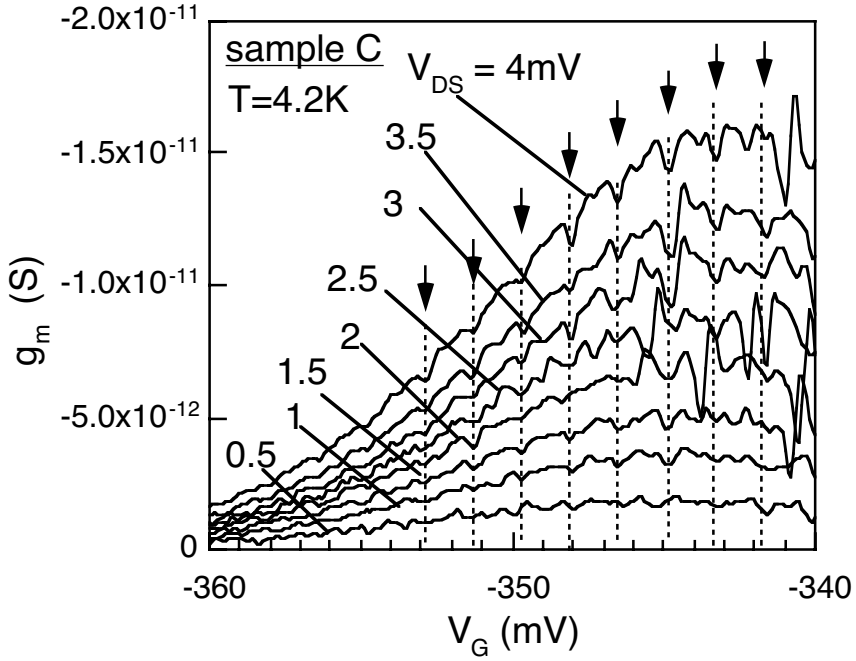

1.6 x10-9
1.2 x10-9
0.8 x10-9
0.4 x10-9
0.
IDS (A)
sample B
T=4.2K
VG = -200mV
-300mV
-400mV
0
50
100
150
200
250
VDS (mV)

(a)

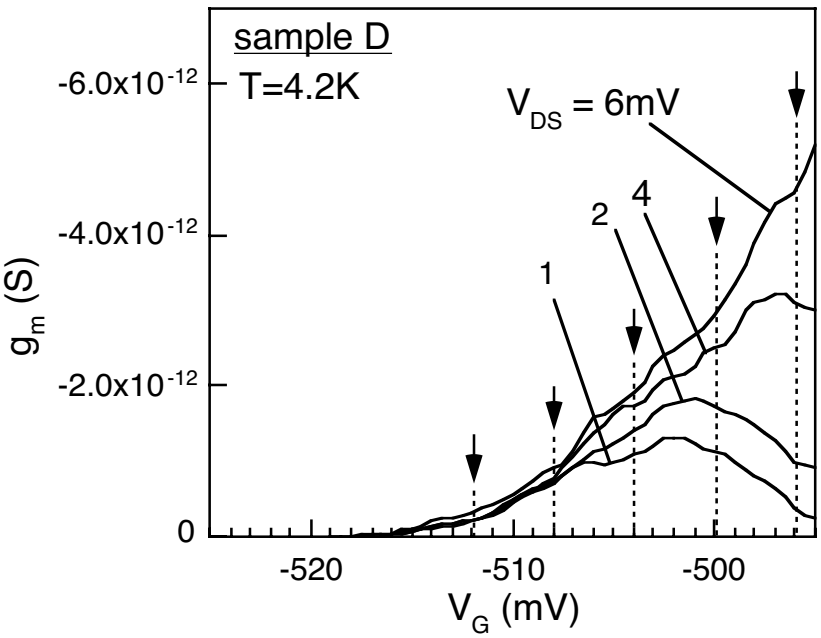

10x10-10
8x10-12
6x10-12
4x10-12
2x10-12
0
gD (S)
sample B
T=4.2K
VG = -200mV
-300mV
-400mV
0
50
100
150
200
250
VDS (mV)

(b)

Figure 8

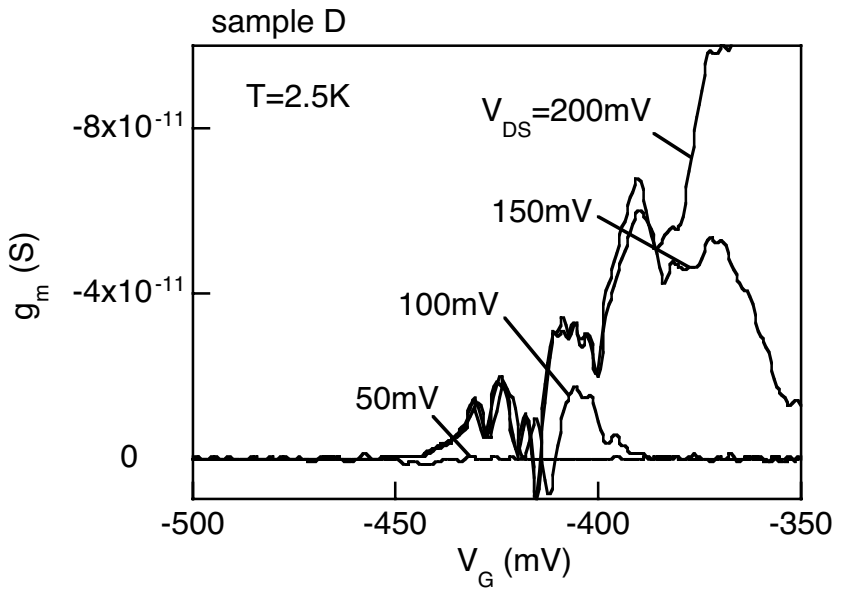

sample C
T=4.2K
V_{DS} = 4mV
3.5
3
2.5
2
1.5
1
0.5
-2.0x10^{-11}
-1.5x10^{-11}
-1.0x10^{-11}
-5.0x10^{-12}
0
g_m (S)
-360
-350
-340
V_G (mV)

(a)

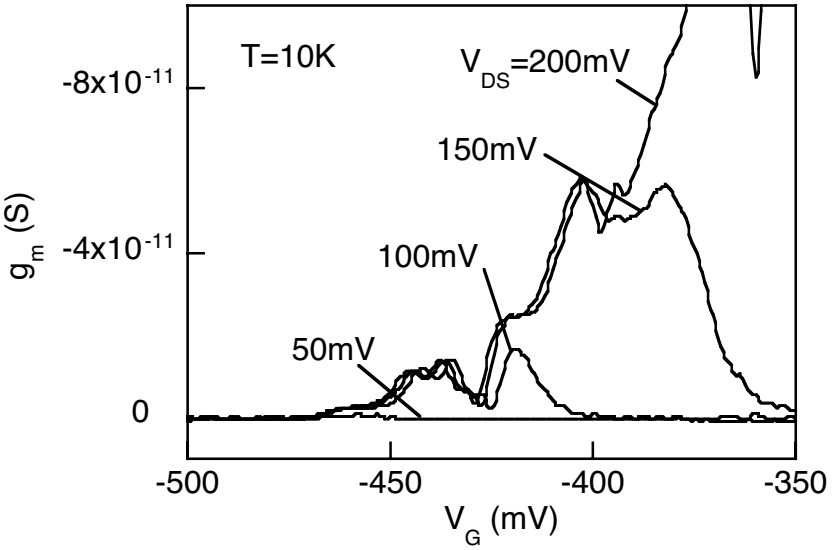

sample D
T=4.2K
V_{DS} = 6mV
4
2
1
-6.0x10^{-12}
-4.0x10^{-12}
-2.0x10^{-12}
0
g_m (S)
-520
-510
-500
V_G (mV)

(b)

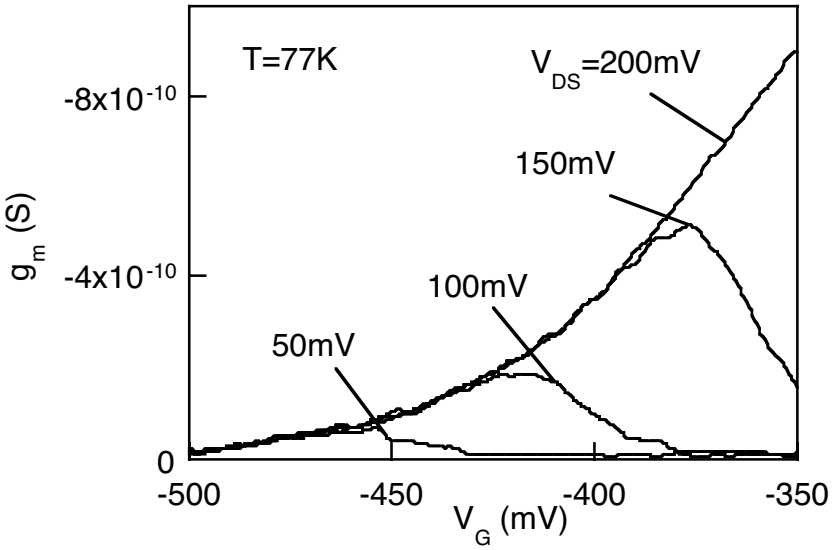
Figure 9



(a)

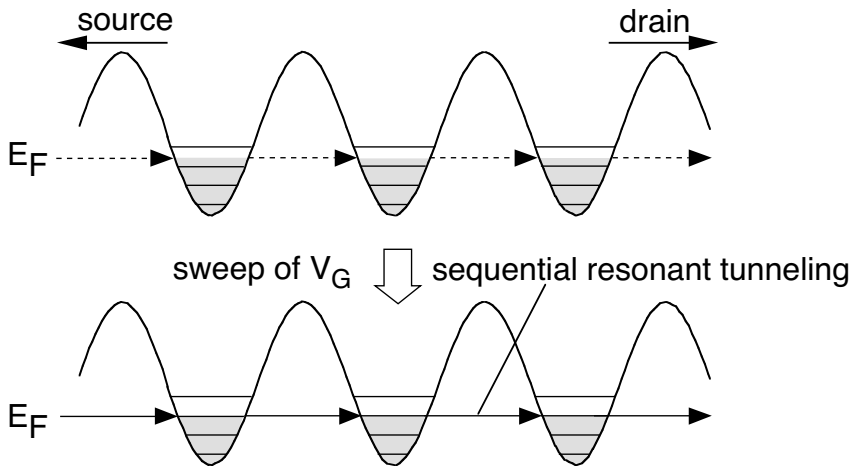


(b)

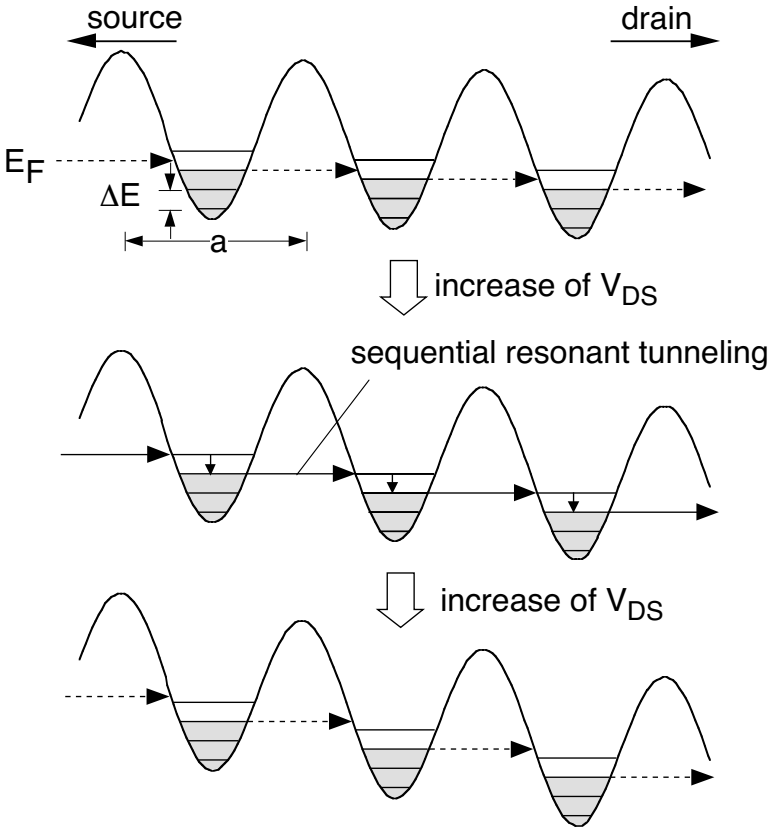


(c)

Figure 10


source
drain
E_F
sweep of V_G
sequential resonant tunneling
E_F

(a)


source
drain
E_F
ΔE
a
increase of V_{DS}
sequential resonant tunneling
increase of V_{DS}

(b)

Figure 11

Table I. Estimated ΔE from the transconductance and drainconductance oscillatioons and estimated Δ_B

	g_m oscillation		g_d oscillation		estimated Δ_B
	ΔV_G	ΔE	ΔV_{DS}	ΔV_{DS} / finger	
sample B	———	———	175meV	2.5meV	120meV
sample C	2meV	1.4meV	140meV	2meV	80meV
sample D	4meV	2.8meV	200meV	2.8meV	150meV