BDD-based 2-bit Arithmetic Logic Unit on GaAs-based Regular Nanowire Network with Hexagonal Topology

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Abstract

A 2-bit arithmetic logic unit (ALU) was successfully fabricated on a GaAs-based regular nanowire network with hexagonal topology. This fundamental building block of central processing units can be implemented on a regular nanowire network structure with simple circuit architecture based on graphical representation of logic functions using a binary decision diagram and topology control of the graph. The 4-instruction ALU was designed by integrating subgraphs representing each instruction, and the circuitry was implemented by transferring the logical graph structure to a GaAs-based

nanowire network formed by electron beam lithography and wet chemical etching. A path switching function was implemented in nodes by Schottky wrap gate-control of nanowires. The fabricated circuit integrating 32 node devices exhibits correct output waveforms at room temperature allowing for threshold voltage variation.

Keywords: Arithmetic logic unit (ALU), nanowire network, binary decision diagram (BDD), Schottky wrap gate (WPG), GaAs

1. Introduction

Nanowires and nanowire network structures are expected to play important roles in next-generation large-scale integrated circuit (LSI) technology. In current semiconductor-based LSI technology, devices and circuits are artificially designed in fine detail and they are produced from only perfectly controlled top-down nanotechnologies. They do not consist of nanostructures spontaneously produced by bottom-up technologies, even those with high regularity, high symmetry, and high-density. As a possible approach to nanowire-based circuits, a hexagonal binary-decision-diagram (BDD) logic circuit was proposed and has been developed recently [1-3]. In this circuit, a logic function is represented graphically using a directed graph instead of conventional logic gates [4, 5]. The graph is directly implemented on a regular nanowire network having hexagonal topology [2, 3]. This circuit architecture enables us to use regular nanowire network structures. It can also simplify circuit design, layout, device structure, and the fabrication process. The basic feasibility of this approach has been clarified by successful demonstration of small logic functions [3, 6], a 2-bit full adder [7], and implementation of a signal processing system using the hexagonal BDD by circuit simulation [8]. It is also noted that the BDD enables us to use quantum nanodevices, such as rapid single flux quantum [9, 10], quantum wire [11], and single electron devices [3, 12], even though these devices are quite difficult to implement conventional logic gate architecture due to small transfer gain and small current drivability. Furthermore, the addition of reconfigurable capability to this circuit

architecture has been investigated recently [13].

The purpose of this paper is to clarify the capability of the hexagonal BDD circuit to implement a fundamental building block of a central processing unit by demonstrating an arithmetic and logic unit (ALU). The ALU, an integration of a set of subsystems, was designed with a simple and regular logical structure. It was implemented as hardware using a GaAs-based hexagonal nanowire network together with Schottky wrap gates (WPGs).

2. Logical Architecture and Physical Implementation

To utilize nanowire network structures for electronic logic circuits, a BDD was chosen as logic architecture instead of the conventional logic gate. The BDD is a graphical way to represent a logic function and has a simple structure. A binary decision tree representing *f* is shown in figure 1(a). As an example, we take a Boolean function *f* = $x_1 x_2 + x_3$. This tree has a data structure completely matching the truth table of *f*. It consists of a root, terminals- 0 and 1, and a number of path-switching nodes labeled x_i. Two exit branches in each node are labeled "0" and "1", and the path is switched according to an input binary variable. The value of the function can be determined for a given input variable assignment by following a path down the tree to a terminal. The binary decision tree is transformed into a binary decision diagram with hexagonal topology, as shown in figure 1(b), by reducing and ordering techniques [1] together with topology control. The hexagonal topology of the graph network comes from the closely

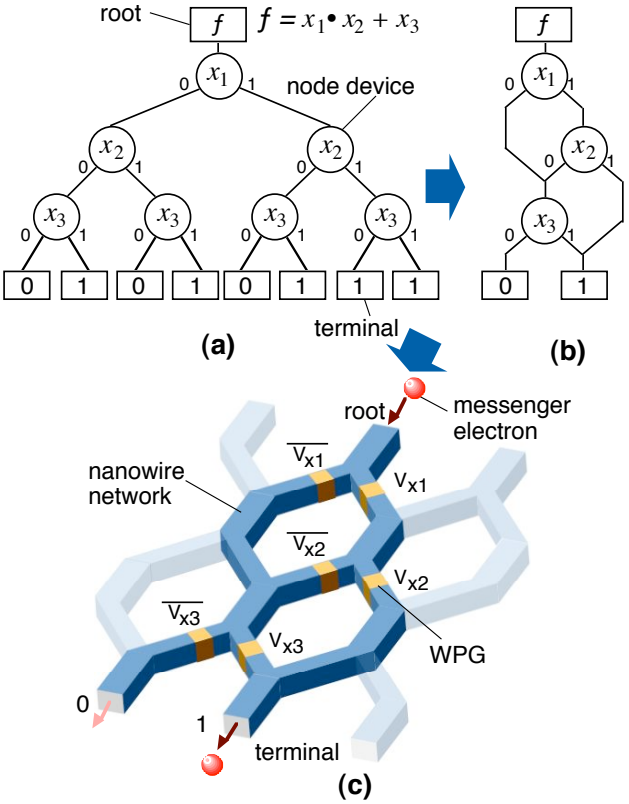

Fig. 1. Basic concept of hexagonal BDD circuits. (a) Binary decision tree of Boolean function $f = x_1x_2 + x_3$, (b) logical structure of BDD with hexagonal topology, and (c) physical implementation.

packed integration of node devices having a threefold symmetric configuration. Any combinational logic function can be represented in this way. Physical implementation of the BDD logic architecture is schematically shown in figure 1(c). The logical structure in figure 1(b) is directly transferred to a semiconductor-based nanowire network having the same topology. The node device is implemented by attaching a nanometer-size gate to each exit nanowire branch, which controls nanowire conduction by the field effect. Path switching is performed by giving complementary gate voltages, Vx_i and $\overline{V}x_i$, simultaneously and turning the conductions of exit branches on/off in a complementary fashion. The value of the logic function is evaluated by sending electrons from the root

to the terminals. If electrons, i.e., current, are detected in terminal-1, the logic is true. If not, it is false. The logic function can be evaluated only using terminal-1, so terminal-0 can be omitted.

There are three reasons that this circuit approach is applicable to regular nanowire networks: the regular graph structure without additional branch crossover, passive operation, and the simplified structure and fabrication process. If a large-scale high-density regular network with hexagonal topology can be formed, it can be used as a host structure of the circuit. Any combinational logic circuit can be fabricated only by removing unnecessary branches and by attaching gates. This provides an opportunity to use regular network structures spontaneously formed by bottom-up nanotechnologies.

3. ALU Design

A diagram of a hexagonal BDD-based 4-instruction 2-bit ALU is shown in figure 2(a). The circuit design and structure are further simplified by bit-slice design [14] and contain redundancy. The design procedure is as follows. After the design of an instruction set, BDD subsystems (i.e., subgraphs) implementing each instruction are designed with a hexagonal layout. At this stage, a merging rule is applied to reduce the isomorphic nodes, retaining no additional nanowire crossover. The order of variables is the same in all subgraphs. Then node devices receiving the same logic input are aligned in the same horizontal line. Next, the subgraphs are integrated using a multiplexer tree for each bit of the output. Finally, the lateral order of the subgraphs is arranged to

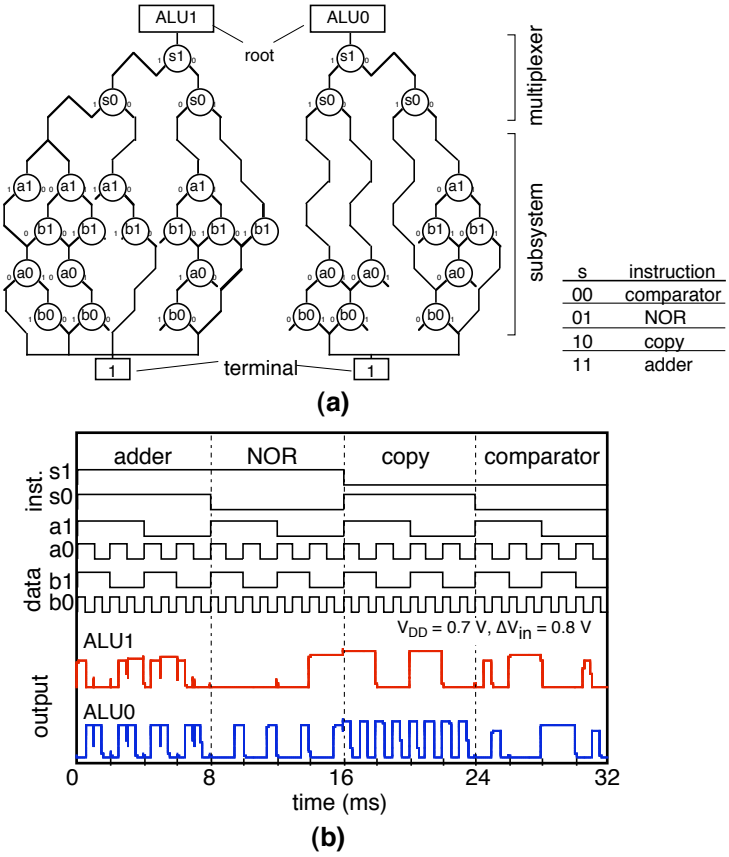

Fig. 2. (a) Diagram of BDD-based 4-instruction 2-bit ALU on hexagonal network and (b) input-output waveforms from circuit simulation.

decrease the total area. The present design approach keeps the logic function for each instruction clearly visible and makes the design and node device layout simple. The shared BDD technique [15] will also reduce the graph size and area. Various techniques and tools for synthesizing BDD and reduction of logical graph size are available [1], and these would be useful for the present circuit design.

The ALU shown in figure 2(a) implements instructions including adder, NOR, copy, and comparator. A 4-input multiplexer combined them for each bit of the output. The output value of the ALU can be evaluated directly from this diagram. Smaller

device counts than that of CMOS logic gate architecture can be obtained in many cases because the BDD represents logic functions compactly [16]. The node device count in the present ALU is 32 with 45 gates, although the transistor count in a straightforward CMOS design with the same composition is 136. A small device count helps to reduce the area and to compensate introduced redundancies for simplifying the design. Typical activity factors of switching in a static CMOS logic gate and the BDD circuit are 0.1 [17] and 0.2 [7], respectively. On the other hand, the device count is under 50 %. Thus, reduction of active power consumption is also expected.

The operation of the ALU was verified by circuit simulation using a conventional circuit simulator. Each node device was represented using two FETs, and the device parameters were extracted from DC and RF measurements [18]. Simulated waveforms are shown in figure 2(b). The circuit operated asynchronously. The obtained result clarified the correct outputs of the ALU, confirming that the design was correct. Synchronous circuit design is important for current large-scale integrated logic circuits. Conventional design inserting flip-flop (FF) circuits might be possible since they can be implemented on the same nanowire network with WPGs [19]. Another possible design is to use clocked electron transfer utilizing a charge-coupled device. It only needs additional gates operating as a turnstile synchronized with the clock. This design is simple and seems suitable for the present BDD. Single- or a-few-electron transfer has been demonstrated experimentally [20 - 22] and this type of the synchronous single electron BDD circuit was successfully implemented by circuit simulation [23].

3. Fabrication

In this study, a GaAs-based nanowire network was used as a host network structure. Nanowire networks and circuits were fabricated using a standard III-V semiconductor device fabrication process without special techniques. First, a regular nanowire network with hexagonal topology was formed on a conventional AlGaAs/GaAs modulation-doped heterostructure grown on (001) GaAs substrates by electron beam (EB) lithography and wet chemical etching with H_2SO_4 solution. The $<\bar{1}10>$, <100>, and $<0\bar{1}0>$ directions were chosen for nanowire branches. Etching depth was 150 nm, reaching a buffer layer under the 2DEG channel. Due to the low-index crystal-faceting nature of wet chemical etching, smooth and uniform networks could be formed reproducibly in a wide area. The fabricated nanowire width was typically 500 nm. The mobility and carrier density of the 2-dimensional electron gas (2DEG) were 5.0 x 10^3 $cm^2V^{-1}s^{-1}$ and 1 x 10^{12} cm^{-2} at 297 K and 1.1 x 10^5 $cm^2V^{-1}s^{-1}$ and 1 x 10^{12} cm^{-2} at 77 K, respectively. The mean free path was 90 nm at 297 K and 1,800 nm at 77 K. Next, Ohmic contacts for the roots and terminals were made by Ge/Au/Ni/Au deposition and subsequent alloying. Schottky wrap gate (WPG) was used, in which a metal gate wraps around the nanowire for tight gate control. It was formed by EB lithography, Pd/Pt deposition, and lift-off. Typical gate length was 500 nm. Interconnect metal lines with 100 nm-width or less were formed at the same level as WPGs without insulators. They did not work as gates because the threshold voltage of the narrow metal lines was very negative due to the short channel effect [24].

4. Experimental Results and Discussion

An example of the fabricated node device is shown in figure 3(a). The direction of the entry branch was $<\bar{1}10>$. A smooth nanowire junction was formed by wet chemical etching. The WPG-controlled nanowires for the exit branches exhibited FET-like *I-V* characteristics, as shown in figure 3(b). These characteristics were uniform and symmetrical. The maximum transconductance, g_m, of 161 mS/mm was obtained at V_{DS}

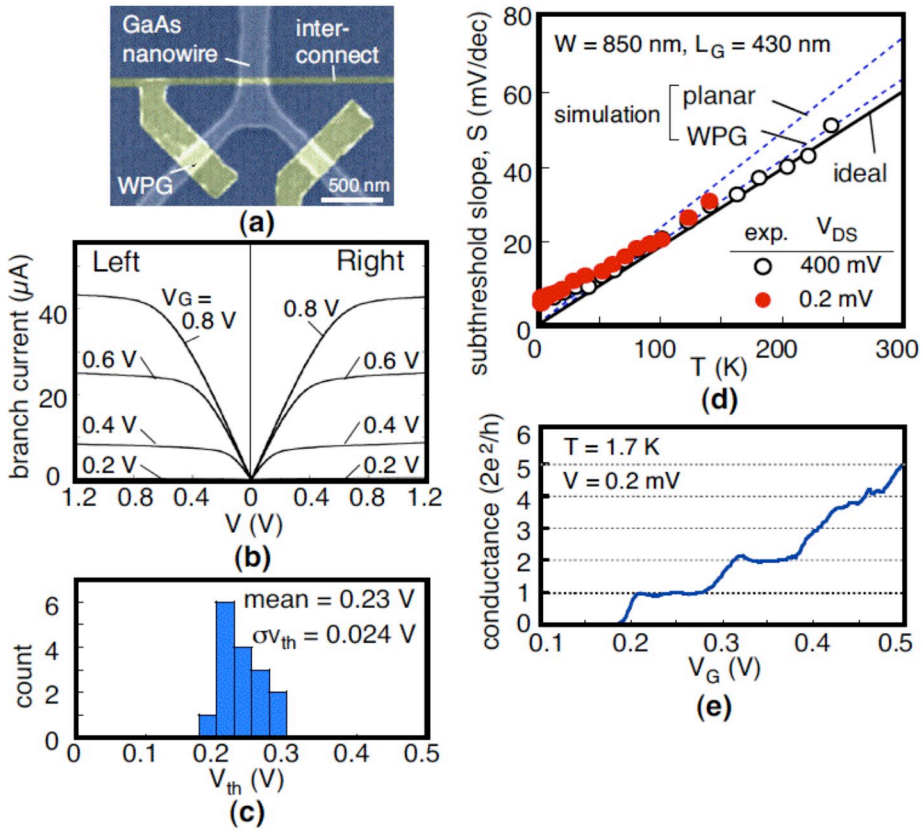

Fig. 3. (a) Example of fabricated node device, (b) typical *I-V* characteristics of both branches of node device, (c) histogram of measured threshold voltage, (d) experimental and theoretical subthreshold slope of WPG as a function of temperature, and (e) transfer curve of WPG-controlled nanowire at 1.7 K.

= 0.2 V in devices with W = 570 nm and L_G = 550 nm. The fabricated devices always operated in the enhancement mode. A histogram of measured threshold voltage, V_{th}, for 16 devices on 8 different wafers is shown in figure 3(c). Average V_{th} was 0.23 V. V_{th} varied from 0.18 to 0.28 V with a standard deviation, σ_{Vth}, of 0.024 V. The observed V_{th} variation was acceptable for the present circuit operation. The circuit was expected to operate correctly by applying enough large input voltage swing to compensate the V_{th} variation.

The measured subthreshold slope in the WPG-controlled nanowire as a function of temperature is shown in figure 3(d). The date was taken at drain voltage 0.2 mV and 0.4 V. The measured values follow an ideal curve given by $kT\ ln(10)/e$ in a wide temperature range. Slight deviation in low temperatures is probably due to the tunneling effect around the top of the potential barrier [25]. We evaluated the subthreshold slope for the WPG and planar gate structures using numerical three-dimensional (3D) potential simulation. The results are also plotted in figure 3(d) by broken lines. The theory reproduced the experimental data well. The simulation clarified that the nearly ideal subthreshold characteristics of the WPG was due to the tight potential control resulting from the 3D gate configuration. The WPG-controlled nanowire is preferable not only in a simple fabrication process but also in low active switching power.

The WPG squeezes the nanowire electrostatically, and a one-dimensional channel can be formed [11, 24]. The typical transfer curve of the WPG-controlled nanowire at 1.7 K is shown in figure 3(e). Clear conductance quantization was observed, confirming the one-dimensional quantum transport. Conductance quantization was

found to appear even at 100 K if the geometrical nanowire width was decreased [26]. Of the devices, over 80% successfully showed conductance quantization at 30 K when $W \leq$ 200 nm [26]. The WPG enables operation of the present circuit with a possibly ultra-small input voltage swing using the quantized conductance.

A SEM image of a fabricated 4-instruction 2-bit ALU is shown in figure 4. The circuit integrated 32 node devices. It was fabricated using a 3M nodes/cm^2 fabrication process. The size of each hexagon was 6 x 6 μm^2, and the total circuit area was 70 x 45 μm^2. L_G and W were 550 nm and 570 nm, respectively. The fabrication process was completely the same as that for discrete node devices. A higher density fabrication process for 45M nodes/cm^2 has already been developed [27] that reduces the area to 7% of present circuits. The area of the BDD ALU depends on the density of the nanowire network. In case of the present material system and the device structure, a critical factor in the scale down is the nanowire width, because it is limited around 40 nm due to side

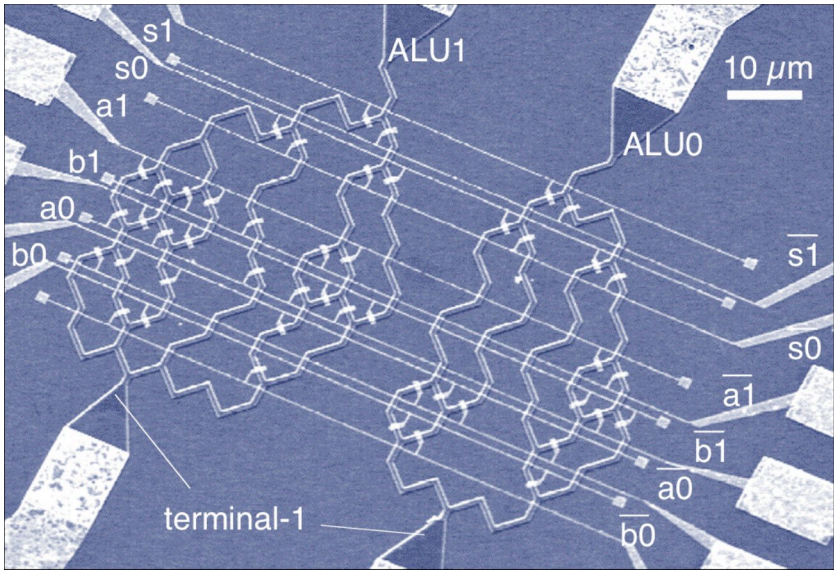

Fig. 4. SEM image of fabricated 4-instruction 2-bit ALU on hexagonal nanowire network.

depletion [26]. Then a possible node density is 1G nodes/cm^2 where the ALU area is 400 times smaller than that in figure 4. Narrow and conductive semiconductor nanowires and networks produced by other sophisticated nanotechnology [28-30] have possibility to provide further high-density BDD circuits.

Measured input-output waveforms at room temperature are shown in figure 5(a). In these measurements, a supply voltage, V_{DD}, of -0.7 V was applied to the roots to send electrons from the roots to the terminals. Output voltages were measured in terminals through 1 MΩ resistors. A DC offset voltage, V_{offset}, of -0.2 V was applied to all the WPGs expect s_1 to obtain output waveforms with uniform height. An input voltage swing, ΔV_{in}, of 0.8 V was used. The output waveforms were found to reproduce the

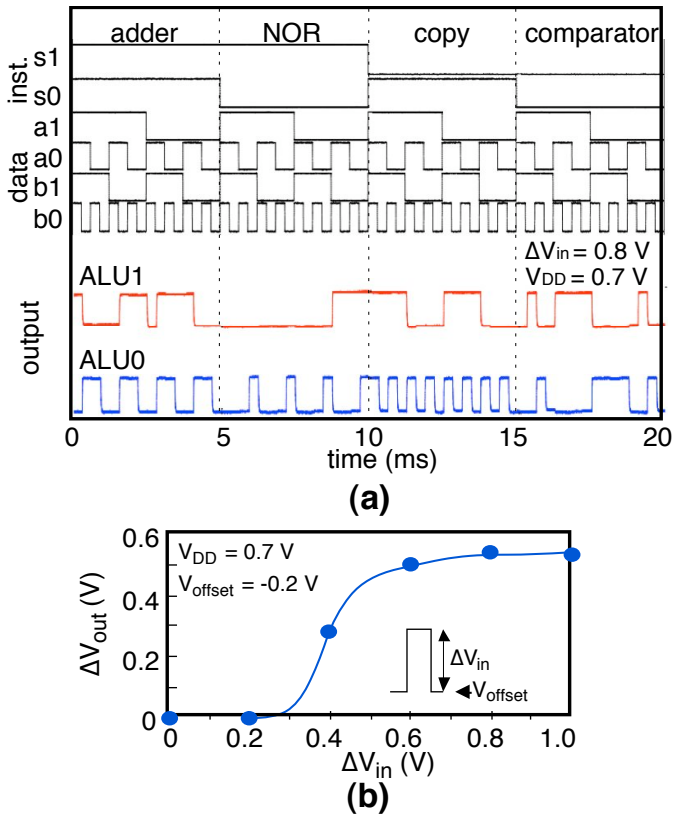

Fig. 5. (a) Measured input-output waveforms and (b) input voltage swing dependence of output of fabricated ALU circuit.

simulated result in figure 2(b). Thus, correct operation of the fabricated ALU was successfully demonstrated experimentally. This result clarifies the feasibility of the present circuit approach for achieving a functional logic circuit at ALU level that utilizes a semiconductor nanowire network structure in a simple manner.

To investigate the effect of V_{th} variation in the fabricated ALU circuit, the input-voltage-swing dependence of the output voltage in the fabricated circuit was characterized. This circuit was expected to operate even with V_{th} variation, if the input voltage swing was large enough to cancel the variation. Measured output voltage amplitude, ΔV_{out}, is shown in figure 5(b). V_{offset} was -0.2 V for all inputs, and V_{DD} was 0.7 V. ΔV_{in} was also the same for all inputs. Input voltage at WPG switch on, V_{on}, was evaluated by ΔV_{in} - V_{offset}. The circuit could operate and could give output signals when $\Delta V_{in} \geq 0.4$ V. The output saturated around 0.57 V when $\Delta V_{in} \geq 0.6$ V. From these results, the WPG having the smallest V_{th} was found to turn on at $V_{on} = 0.2$ V. This value was reasonably consistent with the average V_{th} of 0.23 V in figure 3(c) for node devices having similar dimensions. Also found was that V_{th} variation was small and large input voltage swing was not necessary in the fabricated circuit. Saturation of the output in figure 5(b) indicated that all WPGs turned on sufficiently. From the total nanowire resistance [31] between the root and the terminal and the inserted resistor of 1 MΩ, the output voltage was expected to saturate at 0.6 V. This value reasonably explained the observed saturated output voltage of 0.57 V. The result indicated that the channel resistance under the WPG was small enough in comparison with the nanowire when $V_{on} \geq 0.6$ V. For a practical system utilizing the BDD circuits, sequential and active circuits

such as FF and readout transistors should be also implemented on the same network and these are severely influenced by the V_{th} variation at low supply voltage. As a possible approach, a multiple supply voltage design has been investigated for integrated systems [7, 8]. Sufficient voltage is independently applied to sequential and active circuits to compensate the variation without increasing the supply voltage for the BDD circuits. In addition, for very weak signal readout in fluctuation, a bio-inspired approach that utilizes stochastic resonance (SR) in nanowire devices has been started to investigate [32, 33]. The SR is a phenomenon in which the response of a system is enhanced by noise and thermal fluctuation, and is known to facilitate the detection of a small number of photons in biological systems [34].

Execution time of the ALU circuit for asynchronous operation was estimated from a simple *RC* chain. In a general case, *C* is determined by WPG gate capacitance, C_G. From the discussion of the data in figure 5(b), channel resistance under the WPG is small and total resistance is decided by nanowire resistance. The resistance value can be computed from the resistance per unit length, R_{NW}, and the physical path length from a root to a terminal. Then the execution time of the circuit is estimated by the equation

$$\tau_{ALU} = 2R_{NW}L_{node}C_G\left\{\left[\log_2 N_S\right] + N_B\right\}, \qquad (1)$$

where N_S is the number of instructions, N_B is the number of bits of data, and the brackets denote a floor function. The term in the braces denotes the number of nodes between a root to a terminal. *RC* delay in each node is $R_{NW}L_{node}C_G$, where L_{node} is the physical nanowire length in a node. The fabricated ALU had $N_S = 4$, $N_B = 2$, and $L_{node} = 6$ μm. R_{NW} was 3 kΩ/μm [19, 31]. C_G of a 550 nm-gate WPG was estimated to be 3.0 fF

from the result of RF characterization [18]. Using these parameters, τ_{ALU} = 0.43 ns was obtained, corresponding to the intrinsic operation frequency of 2.3 GHz. The power-delay product (PDP) of the ALU was roughly estimated by $(N/N_S)C_G\Delta V_{in}^2$ for active switching. N is the node device count. N/N_S is an average number of node devices per instruction. N = 32 and ΔV_{in} = 0.4 V. The possible PDP of the present ALU with L_G = 550 nm and W = 570 nm was estimated to be 3.8 x 10^{-15} J. This value is comparable to the PDP of the reported full adder using an ultra-low power subthreshold CMOS circuit by 0.35-μm process technology [35], indicating the low-power consumption capability of the BDD ALU. Although there are many complex factors in the scaling recently [36], it is useful to estimate performance of the circuits according to the simple scaling. The commercially available 45-nm CMOS process technology will give one order of magnitude smaller PDP than the above values due to the decrease of C_G [36]. If the same scale down of the gate size is available for the present BDD circuit, the PDP will also decrease and its advantage in the power consumption will be held. The present BDD circuit is expected to demonstrate its ability of the ultra-low power consumption in the quantum transport domain. In the case of sufficiently small V_{th} variation, the input voltage swing can be decreased because the device switches a smaller number of electrons using the abrupt quantized conductance step as shown in figure 3 (e). Possible PDP in the WPG-controlled nanowire FET operating as a quantum wire transistor at 30 K was 3 x 10^{-20} J for the device with L_G = 300 nm [26]. This results in the PDP of 2.4 x 10^{-19} J for the BDD ALU. Assuming the linear dependence of the switching voltage on temperature as the subthreshold slope and the 45 nm design rule, the effective PDP

extrapolated to RT is 3.6 x 10^{-17} J. It is one order smaller than that of the 45 nm subthreshold-CMOS full adder.

Finally, we mention the possibility of the present circuit approach for other nanodevices, such as organic devices and molecular devices as well as quantum devices. Major factors preventing their application to the conventional integrated circuits are low transfer gain and large V_{th} variation. The present circuit operates with passive switching, solving the first problem. This has been confirmed by successful demonstration of BDD circuits integrating single electron devices [3] and quantum wire devices [11]. V_{th} variation can be also compensated in the present circuit by large input voltage swing. From figure 5(b) and discussion of the data, the circuit was found to operate correctly even though each device did not turn on sufficiently and there were only small current flows. The fabricated ALU circuit is expected to operate as a quantum device integrated circuit because WPG-controlled nanowires can operate as quantum wire transistors in low temperatures. Demonstration of the circuit operation in a quantum transport domain should confirm the above possibility, and it remains as future work.

5. Conclusion

A 2-bit arithmetic logic unit (ALU) was achieved on a GaAs-based regular nanowire network with hexagonal topology. This fundamental building block of central processing units can be implemented on a regular nanowire network structure with simple circuit architecture based on graphical representation of logic functions using a

binary decision diagram (BDD) and topology control of the graph. A 4-instruction 2-bit ALU was designed by integrating subgraphs representing each instruction. The circuit was fabricated by transferring the logical graph structure to a GaAs-based nanowire network formed by EB lithography and wet chemical etching together with Schottky wrap gate (WPG) control of nanowires. The fabricated circuit integrating 32 node devices operated correctly at room temperature, allowing for threshold voltage variation. Obtained results indicated that the present circuit approach can possibly utilize various nanodevices that are difficult for current-driven integrated circuits having logic gate architecture to utilize.

Acknowledgements

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Figure captions

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