Threshold-Logic Devices Consisting of Subthreshold CMOS Circuits

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SUMMARY A threshold-logic gate device consisting of subthreshold MOSFET circuits is proposed. The gate device performs threshold-logic operation, using the technique of current-mode addition and subtraction. Sample digital subsystems, i.e., adders and morphological operation cells based on threshold logic, are designed using the gate devices, and their operations are confirmed by computer simulation. The device has a simple structure and operates at low power dissipation, so it is suitable for constructing cell-based, parallel processing LSIs such as cellular-automaton and neural-network LSIs.

key words: subthreshold, MOS, circuit, threshold logic, majority logic, gate, current mode

1. Introduction

Threshold logic is a way of digital processing that is more functional than conventional AND-OR Boolean logic. To construct LSIs based on threshold logic, we propose a gate device for threshold-logic operation that is compatible with silicon technology. This device is a threshold logic gate consisting of subthreshold-operated MOSFET circuits.

Threshold logic implements digital operations in a manner different from that of Boolean logic. Instead of using Boolean logic operators (AND, OR, and their complements), threshold logic represents and manipulates digital functions on the basis of threshold comparison. The logic process of threshold logic is much more sophisticated than that of Boolean logic; consequently, threshold logic is more powerful for implementing a given digital function with a smaller number of logic gates. Besides, threshold logic is very compatible with functional processing architectures such as the cellular automaton, neural network, and holonic processing.

In this paper, we propose a method of constructing gate devices for threshold logic. Section 2 outlines the unit function required for threshold logic and presents a method of implementing the function using the technique of current-mode addition and subtraction. Section 3 presents a gate device that can implement the unit function with CMOS technology. The device consists of a MOSFET circuit operated in the subthreshold region, i.e., the region where the gate-source voltage is smaller than the threshold voltage of MOSFETs and drain-source current is in a range of 1–100 nA. The logic operation of the device is studied by computer simulation. Section 4 describes the design of simple subsystems, adders and morphological operation cells consisting of our gate devices. The simulated operation of these subsystems is also described.

2. Implementing the Function of Threshold Logic

2.1 Unit Function of Threshold Logic

The unit function of threshold logic is determining the output logic value on the basis of threshold comparison. The logic element, a threshold-logic gate, has a number of binary inputs and a binary output. It produces an output of 1 if the sum of inputs is larger than a threshold value, and produces an output of 0 if the sum is smaller than the threshold. The function of a five-input gate is shown in Fig. 1 for various values of threshold \( k \). If the threshold is 3.5 for instance, the output is 0 for inputs 1, 1, 0, 0, 1, and the output is 1 for inputs 1, 1, 0, 1, 1. (For further details on threshold logic, see Ref. [1]) Any digital function can be implemented using a combination of threshold gates and inverters. If a gate has odd number \( n \) of inputs and the threshold is set to \( n/2 \), the gate performs the operation of majority logic because its output is determined with majority vote of 1-0 inputs. Three-input majority gates suffice for the construction of any logic functions.

2.2 Implementing the Unit Function

To implement such threshold logic operation, we developed a gate circuit on the basis of a current-mode addition/subtraction technique. The concept of the circuit is illustrated in Fig. 2. The circuit consists of two subcircuits: a threshold current source \( kI_0 \), and input current sources \( I_i \) with switches controlled by binary input signals \( X_i \) (ith switch is on for \( X_i = 1 \)). The threshold current source drains current \( kI_0 \) (k is the threshold of the gate) from the sum line, and each input current source injects current \( I_0 \) into the sum line. The net current injected to the sum line is \( \sum X_i \cdot kI_0 \). The circuit accepts 1-0 binary inputs \( X_i \) and compares the number of 1-inputs with threshold \( k \) to produce the corresponding output voltage. If the number of 1-inputs is larger than \( k \), the net current for the sum-line is positive and, consequently, the voltage of the sum line will rise to a 1 state; otherwise the net current is negative and the voltage of the

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3. Constructing the Threshold-Logic Gate Circuit

3.1 Gate Circuit

The threshold logic gate (M₁-M₆) we propose is illustrated in Fig. 3, with an example of a three-input configuration (a CMOS inverter M₇-M₈ is also shown). It consists of input transistors M₁-M₃ with a gate width of W, threshold-current transistor M₄ with a gate width of \((n-k)W\) (k: threshold value, n: the number of inputs) and an output inverter M₅-M₆. Bias voltages \(V_{dd}\) and \(V_{gg}\) are set to appropriate values so that, when the input voltage is 0, the current flowing through each of M₁-M₃ will be \(1/k\) of the current through M₄. This can be performed using a power supply circuit shown later in Figs. 5 and 6.

The operation of the gate circuit is as follows. If the number of 1-inputs (or inputs with voltage \(V_{dd}\)) for M₁-M₃ is smaller than threshold k, the net current injected to the sum line is positive. This raises the voltage of the sum line to a high value, so the output of inverter M₅-M₆ falls to 0 (logic 0). In contrast, if the number of 1-inputs is larger than k, the net current for the sum line is negative; consequently, the voltage of the sum line falls to a low value, and the output of the inverter rises to \(V_{dd}\) (logic 1). The gate operates as a majority gate if we set k to 3/2.

Our threshold logic gate uses a current flow for logic operation, thereby producing power dissipation even in a static state; this would be inevitable generally in threshold gate devices and other analog-like logic devices. To reduce power dissipation, we operate the gate circuit in the subthreshold region of MOSFETs.

The subthreshold region is a region where the gate-source voltage of a MOSFET is smaller than the threshold voltage of the MOSFET (see [2] for details of the subthreshold operation of MOSFETs). Figure 4 shows the transfer characteristics of nMOS and pMOS transistors (0.35-μm CMOS devices, W/L = 1.5 μm/0.35 μm).
3.2 Power Supply for the Gates

Two kinds of power supplies for our logic gates are shown in Figs. 5 and 6. Both convert an external source voltage $V_{ss}$ to bias voltages $V_{dd}$ and $V_{gg}$ such that a current $I_0$ in monitoring transistors (M14-M15 in Fig. 5 and M26-M27 in Fig. 6) is equal to a given reference current $I_{ref}$. Voltages $V_{dd}$ and $V_{gg}$ are used as biases for the gates. The gate width of the monitoring transistors (M14, M15, M26, and M27) is set equal to that of the input transistors (M1-M3 in Fig. 3) in the gate. By setting $I_{ref}$ to 1–100 nA, we can ensure the subthreshold operation of each MOSFET in the gate.

The circuit in Fig. 5 operates as follows. Reference current $I_{ref}$ is injected to gate node Q of regulating transistor M16 through current mirror M11-M12, and monitoring current $I_0$ is drained from node Q through current mirror M13-M14. If $I_0 < I_{ref}$, the circuit performs a negative feedback operation to increase $I_0$; that is, $I_0 < I_{ref} \rightarrow$ node voltage Q increases $\rightarrow$ on-resistance in M16 decreases $\rightarrow$ supply voltage $V_{dd}$ increases $\rightarrow$ monitoring current $I_0$ increases $\rightarrow I_0$ is equalized to $I_{ref}$. And if $I_0 > I_{ref}$, the circuit operates in a similar manner to equalize $I_0$ to $I_{ref}$. This circuit is stable and has no possibility of oscillation. However, it needs a large external source voltage $V_{ss}$ because the voltage of node Q has to be larger than $V_{dd}$ by the threshold voltage of M16. The circuit cannot operate if external source voltage $V_{ss}$ is smaller than the sum of $V_{dd}$ and the threshold voltage of M16. For instance, with nMOS and pMOS transistors we used, external source voltage $V_{ss}$ should be larger than 1.3 V as shown Fig. 7. Therefore, this circuit is unsuitable for the use of a manganese dry cell with a nominal voltage of 1.5 V.

This problem can be solved using a pMOS transistor as a regulating transistor. Figure 6 shows the modified circuit with the regulating transistor M28. The operation is similar to that of the circuit in Fig. 5. The modified circuit can operate on condition that external source voltage $V_{ss}$ is larger than the threshold voltage of M28. The lower limit of external source voltage $V_{ss}$ can be reduced to 0.7 V, as shown in Fig. 7. This circuit has the possibility of oscillation, so a compensation capacitance (1 pF) was connected for safety between the gate and the drain of M28. We used this power supply circuit in the following sections.

3.3 Operation of the Gate

We simulated the operation of our gates, taking a 3-input majority gate ($k = 3/2$) shown in Fig. 3. We used the power supply circuit shown in Fig. 5. The transistor size was set to $W/L = 1 \mu m/0.35 \mu m$ for all transistors except for M4 in the threshold-logic subcircuit (Fig. 3) and M28 in the power supply circuit (Fig. 6). The size of M4 was set to $1.5 \mu m/0.35 \mu m$ because the gate width of M4 was given by $(n-k) \times 1 \mu m$, where $n$ is the number of inputs ($n = 3$) and $k$ is the threshold value ($k = 1.5$). The size of power M28 in the power supply circuit was set to $W/L = 80 \mu m/0.35 \mu m$. The external voltage $V_{ss}$ was set to 1.5 V in the power supply circuit. Reference current $I_{ref}$ was set to 10 nA, so the power supply circuit produced bias voltages $V_{dd}$ and $V_{gg}$ such that monitoring current $I_0$ was adjusted to be 10 nA. The values of $V_{dd}$ and $V_{gg}$ were 610 mV and 390 mV.

The result of simulation is shown in Fig. 8. In simulation, we increased the number of 1-inputs (inputs of which voltage is $V_{dd}$) with time. First, the three inputs for the gate was 000, then changed to 001 at time $= 10 \mu s$, to 011 at $20 \mu s$, and to 111 at $30 \mu s$. When two inputs rose to $V_{dd}$ (logic 1), the voltage of the sum line changes from high to low, and the output inverter produces an output $V_{dd}$ (logic 1). The circuit shows a majority logic operation. The current in the gate was maximum and 28 nA for an input of 001. For this input, the power consumption was maximum and...
17 nW. This value is smaller than other threshold-logic devices. For example, on the neuron MOSFET(νMOS) gate—a typical example of existing threshold-logic devices—the power consumption has been reported several hundreds of microwatts [5], [6].

If two or three inputs are 1, the voltage of the sum line should be 0 because current drained from the sum line is larger than injected current. In practice, however, the voltage of sum line was about 200 mV for an input of 011. This is so because the injected current through M1, M2, or M3 and the drained current through M4 in the gate were balanced at this voltage. However, because the voltage of sum line for input 011 is always lower than the inverting threshold voltage of the output inverter, the output inverter produces an output 1 correctly.

4. Adders Consisting of Threshold Logic Gates

Using the gate circuits, we designed a 8-bit ripple carry (RC) adder and a 8-bit carry-look-ahead (CLA) adder and simulated their operations.

Figure 9 (a) shows the full adder consisting of majority gates and inverters. Sum output \( S_i \) should be 1 when the number of 1-inputs in three inputs \( X_i, Y_i, \) and \( C_{i-1} \) is 1 or 3 (odd parity). Carry output \( C_i \) should be 1 when the number of 1-inputs is 2 or 3 (majority decision). These operations can be performed using 3 majority gates and 2 inverters. Figure 9(b) shows the operation of an 8-bit adder. Figure 9(c) shows the circuit of an 8-bit RC adder and Fig. 9(d) shows a carry-look-ahead circuit for the 8-bit CLA adder.

We confirmed the circuit operation by computer simulation and calculated the addition time of the RC and the CLA adders. Monitoring current \( I_0 \) and external voltage \( V_{ss} \) in the power supply circuit were set to 10 nA and 1.5 V. The number of gates that a signal has to passes from the least-significant-bit inputs \( (X_0,Y_0) \) to the most-significant-bit output is 9 in the RC adder and 5 in the CLA adder. The addition time was the time to perform a calculation of 11111111 + 00000001 = 100000000. Figure 10 shows the waveforms for the voltage of each signal bit. The upper figure shows the voltages of input bits; all input bits were initially 0 and, at time = 0, nine bits were raised to 1 (= \( V_{dd} \)) and seven bits were kept 0. The middle figure depicts the voltages of output bits (sum bits and carry bits) of the RC adder. The bottom figure depicts the output bits of the CLA adder. The addition time was determined by the delay of the most significant bit \( S_7 \) of the sum output. The addition time of the RC adder was 5.1 \( \mu \)s (Fig. 10(a)), and that of the CLA adder was 3.4 \( \mu \)s (Fig. 10(b)).

5. Majority-Black Circuit Consisting of Threshold Logic Gates

As a promising application of our threshold logic gate, we designed cellular-automaton cells that perform morphological operations for picture processing. The following shows part of the result, taking the majority-black operation as an example. The majority-black operation is a morphological picture processing for binary images. It is useful for filling
small holes and eliminating small projections in objects and, therefore, can be used for noise elimination (Fig. 11(a)). The majority-black operation is a processing for a $3 \times 3$ pixel window, and its operation is as follows; set the center pixel to black if five or more pixels in the $3 \times 3$ window are black; otherwise set the center pixel to white (Figs. 11(b) and 11(c)). In picture processing, the majority-black operation is performed in all pixels on a picture synchronously with a clock.

The cell function of majority-black operation can be performed using a 9-input majority gate circuit shown in Fig. 12. Each input corresponds to the state of each pixel in the $3 \times 3$ window; we define that the input is 1 (voltage $V_{dd}$) if the pixel is black and the input is 0 if the pixel is white. The output of the circuit corresponds to the subsequent state of the center pixel; the subsequent state is black for a 1-output and white for a 0 output. If the number of 1-inputs for $M_{31}$-$M_{39}$ is higher than the threshold ($=4.5$), the net current injected to the sum line is negative. The output of the inverter rises to $V_{dd}$ (logic 1). If the number of 1-inputs is lower than the threshold, the output falls to 0 (logic 0). The width of $M_{40}$ is set to $4.5 \times 1 \mu m$ because the gate width of $M_{40}$ is given by $(n - k) \times 1 \mu m$, where $n$ is the number of inputs ($n = 9$) and $k$ is the threshold value ($k = 4.5$).

We simulated the operation of the majority-black circuit. The result is shown in Fig. 13. The reference current was set to $I_{ref} = 10 \text{nA}$. The external voltage $V_{ss}$ was set to 1.5 V, and the power supply circuit produced voltages $V_{dd} = 610 \text{mV}$ and $V_{gg} = 390 \text{mV}$. In simulation, we increased the number of 1-inputs with time. First, the nine inputs for the gate was 000000000, then changed to 000000001, 000000011, and 111111111. When five inputs rose to 1, the voltage of sum line fell and the inverter output changed from 0 to 1. The circuit performed a majority black operation successfully. The maximum current and power con-
6. Conclusion

We proposed a threshold-logic gate consisting of subthreshold MOSFETs circuits. The circuit can be constructed with simple circuit configuration and low power dissipation, and can be used for elementary cell circuits for large-scale parallel signal processing such as cellular-automaton and neural-network applications. As example subsystems, we designed adders and majority-black operation cells by using the gates. Using our threshold-logic gate will enable us to construct low-power, functional processing LSIs.

References


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