A 300 nW, 15 ppm/°C, 20 ppm/V CMOS Voltage Reference Circuit Consisting of Subthreshold MOSFETs

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***Abstract*—A low-power CMOS voltage reference was developed using a 0.35 μm standard CMOS process technology. The device consists of MOSFET circuits operated in the subthreshold region and uses no resistors. It generates two voltages having opposite temperature coefficients and adds them to produce an output voltage with a near-zero temperature coefficient. The resulting voltage is equal to the extrapolated threshold voltage of a MOSFET at absolute zero temperature, which was about 745 mV for the MOSFETs we used. The temperature coefficient of the voltage was 7 ppm/°C at best and 15 ppm/°C on average, in a range from −20 to 80°C. The line sensitivity was 20 ppm/V in a supply voltage range of 1.4–3 V, and the power supply rejection ratio (PSRR) was −45 dB at 100 Hz. The power dissipation was 0.3 μW at 80°C. The chip area was 0.05 mm^2. Our device would be suitable for use in subthreshold-operated, power-aware LSIs.**

***Index Terms*—CMOS, voltage reference, ultra-low power, subthreshold, weak inversion, process variation, die-to-die variation, power-aware LSIs.**

I. Introduction

ONE of the promising areas of research in microelectronics is the development of ultra-low power LSIs that operate in the subthreshold region of MOSFETs, i.e., a region at which the gate-source voltage of MOSFETs is lower than the threshold voltage [1], [2]. Such LSIs would be suitable for use in power-aware LSI applications such as portable mobile devices, implantable medical devices, and smart sensor networks [3]. These devices have to operate with ultra-low power, e.g., a few microwatts or less [3]–[5] because they will probably be placed under conditions where they have to get the necessary energy from poor energy sources such as microbatteries and environmental energy sources [6]. As a step toward such LSIs, we first need to develop a voltage reference circuit that can operate with an ultra-low current, several tens of nanoamperes or less. To achieve such low power operation, the circuit has to be operated in the subthreshold region of MOSFET.

A voltage reference is one of the important building blocks for analog, digital, and mixed-signal circuit systems in microelectronics. It generates a constant reference voltage for other various components such as operational amplifiers, comparators, and AD/DA converters. For this purpose, bandgap reference circuits with CMOS-based vertical bipolar transistors are conventionally used in CMOS LSIs [7], [8]. However, they need resistors with a high resistance of several hundred megaohms to achieve low-current, subthreshold operation. Such a high resistance needs a large area to be implemented, and this makes conventional bandgap references unsuitable for use in ultra-low power LSIs. Therefore, modified voltage reference circuits for low-power LSIs have been reported (see [9]–[13]). However, these circuits have various problems. For example, their power dissipations are still large, and their outputs voltages are sensitive to supply voltage and temperature variations; these are quite inconvenient for practical use in ultra-low power LSIs. Moreover, the effect of the process variations on the reference voltage was not discussed in detail.

To solve these problems, we developed a new voltage reference that can operate with sub-microwatt power dissipation and has less temperature sensitivity and a smaller line sensitivity [14] than the reported works [9]–[13]. Our device consists of subthreshold MOSFET circuits and uses no resistors. It generates two voltages having opposite temperature coefficients (TCs), i.e., a MOSFET threshold voltage with a negative TC and a multiple of the thermal voltage with a positive TC, and adds them to produce an output voltage with a zero TC. The output voltage is equal to the threshold voltage of a MOSFET at 0 K and is about 745 mV for MOSFETs we used. The voltage is quite insensitive to temperature and the supply voltage variations, although its value fluctuates with process variation. By utilizing the nature of the reference voltage, which changes with the process conditions of threshold voltage in each LSI chip, the circuit can be used as an elementary circuit block for on-chip process compensation systems. The following sections provide the details on our device. Section II describes the principle of our voltage reference and discusses the effect of process variations. Section III explains the method of designing the circuit with a SPICE simulator. Section IV shows the characteristics of a prototype device we made using a 0.35 μm standard CMOS process technology. A small TC of 7 ppm/°C and a line sensitivity of 20 ppm/V were achieved.

II. Circuit Configuration

The principle of our voltage reference circuit is illustrated in Fig. 1. The circuit consists of a current source subcircuit

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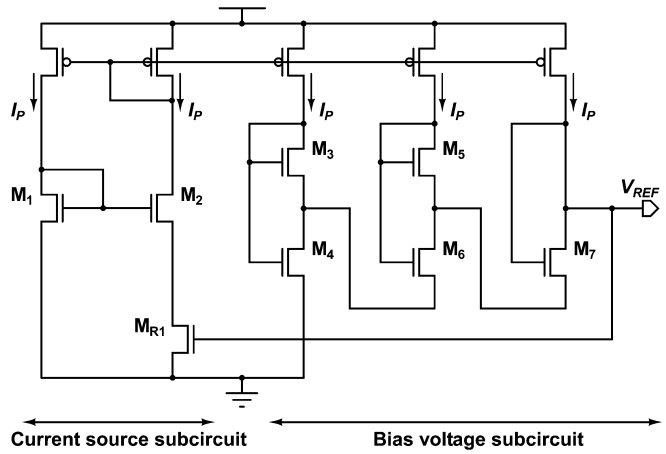

Fig. 1. Schematic of our voltage reference circuit.

and a bias-voltage subcircuit. The current source subcircuit is a modified β multiplier self-biasing circuit that uses a MOS resistor $\mathrm{M_{R1}}$ instead of ordinary resistors. It generates a current, I_P. The bias-voltage subcircuit accepts current I_P through pMOS current mirrors and produces an output voltage (i.e., reference voltage), V_{REF}. The bias-voltage subcircuit consists of a transistor $(\mathrm{M_4})$ and two source-coupled pairs ($\mathrm{M_3}$–$\mathrm{M_6}$ and $\mathrm{M_5}$–$\mathrm{M_7}$). The gate-source voltages of $\mathrm{M_3}$–$\mathrm{M_7}$ in the bias-voltage subcircuit and $\mathrm{M_{R1}}$ in the current source subcircuit form a closed loop [15], [16]. All the MOSFETs except for $\mathrm{M_{R1}}$ are operated in the subthreshold region. The MOS resistor $\mathrm{M_{R1}}$ is operated in a strong-inversion, deep-triode region. The circuit generates two voltages with a negative TC and a positive TC and combines them to produce a constant voltage with a zero TC. The following sections describe the operation in detail.

A. Operation Principle

The subthreshold drain current I_D of a MOSFET is an exponential function of the gate-source voltage V_{GS} and the drain-source voltage V_{DS}, and given by

$$I_D = KI_0 \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{\eta V_T}\right) \times \left(1 - \exp\left(-\frac{V_{\mathrm{DS}}}{V_T}\right)\right), \quad I_0 = \mu C_{\mathrm{OX}}(\eta - 1){V_T}^2, \tag{1}$$

where K is the aspect ratio $(= W/L)$ of the transistor, μ is the carrier mobility, C_{OX} is the gate-oxide capacitance, $V_T (= k_B T/q)$ is the thermal voltage, k_B is the Boltzmann constant, T is the absolute temperature, and q is the elementary charge, V_{TH} is the threshold voltage of a MOSFET, and η is the subthreshold slope factor [1], [17]. For $V_{\mathrm{DS}} > 0.1$ V, current I_D is almost independent of V_{DS} and given by

$$I_D = KI_0 \exp\left(\frac{V_{\mathrm{GS}} - V_{\mathrm{TH}}}{\eta V_T}\right). \tag{2}$$

In the current-source subcircuit, gate-source voltage V_{GS1} in $\mathrm{M_1}$ is equal to the sum of gate-source voltage V_{GS2} in $\mathrm{M_2}$ and drain-source voltage V_{DSR1} in $\mathrm{M_{R1}}$, i.e.,

$$V_{\mathrm{GS1}} = V_{\mathrm{GS2}} + V_{\mathrm{DSR1}}. \tag{3}$$

Because currents I_P in $\mathrm{M_1}$ and in $\mathrm{M_2}$ are equal to each other, (3) can be rewritten as

$$V_{\mathrm{DSR1}} = \eta V_T \ln(K_2/K_1). \tag{4}$$

MOS resistor $\mathrm{M_{R1}}$ is operated in a strong-inversion, deep-triode region, so its resistance $R_{M_{R1}}$ is given by

$$R_{M_{R1}} = \frac{1}{K_{R1}\mu C_{\mathrm{OX}}(V_{\mathrm{REF}} - V_{\mathrm{TH}})}. \tag{5}$$

From (3), (4), and (5), we arrive at the expression

$$I_P = \frac{V_{\mathrm{DSR1}}}{R_{M_{R1}}} = K_{R1}\mu C_{\mathrm{OX}}(V_{\mathrm{REF}} - V_{\mathrm{TH}})\eta V_T \ln(K_2/K_1) \tag{6}$$

for current I_P. In the bias-voltage subcircuit, the gate-source voltages (V_{GS3} through V_{GS7}) of the transistors form a closed loop, and the currents in $\mathrm{M_4}$ and $\mathrm{M_6}$ are $3I_P$ and $2I_P$. Therefore, we find that output voltage V_{REF} of the circuit is given by

$$\begin{aligned} V_{\mathrm{REF}} &= V_{\mathrm{GS4}} - V_{\mathrm{GS3}} + V_{\mathrm{GS6}} - V_{\mathrm{GS5}} + V_{\mathrm{GS7}} \\ &= V_{\mathrm{GS4}} + \eta V_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right) \\ &= V_{\mathrm{TH}} + \eta V_T \ln\left(\frac{3I_P}{K_4 I_0}\right) + \eta V_T \ln\left(\frac{2K_3K_5}{K_6K_7}\right) \end{aligned} \tag{7}$$

where we assumed that the mismatch between the threshold voltages of the transistors can be ignored. Equation (7) shows that V_{REF} can be expressed as a sum of the gate-source voltage V_{GS4} and thermal voltage V_T scaled by the transistor sizes. Because V_{TH} has a negative TC and V_T has a positive TC, output voltage V_{REF} with a zero TC can be obtained by adjusting the size of the transistors.

The temperature dependence of the threshold voltage can be given by

$$V_{\mathrm{TH}} = V_{\mathrm{TH0}} - \kappa T \tag{8}$$

where V_{TH0} is the threshold voltage at 0 K, and κ is the TC of V_{TH} [18]. Equations (6) and (8) show that output voltage V_{REF} can be rewritten as

$$V_{\mathrm{REF}} = V_{\mathrm{TH0}} - \kappa T + \eta V_T \ln\left\{\frac{6\eta K_{R1}K_3K_5(V_{\mathrm{REF}} - V_{\mathrm{TH}})}{K_4K_6K_7(\eta - 1)V_T} \ln\left(\frac{K_2}{K_1}\right)\right\}. \tag{9}$$

The TC of V_{REF} is given by

$$\frac{dV_{\mathrm{REF}}}{dT} = -\kappa + \frac{\eta k_B}{q} \times \ln\left\{\frac{6\eta K_{R1}K_3K_5(V_{\mathrm{REF}} - V_{\mathrm{TH}})}{K_4K_6K_7(\eta - 1)V_T} \ln\left(\frac{K_2}{K_1}\right)\right\} + \eta V_T \left\{\frac{1}{V_{\mathrm{REF}} - V_{\mathrm{TH}}}\left(\frac{dV_{\mathrm{REF}}}{dT} + \kappa\right) - \frac{1}{T}\right\}. \tag{10}$$

On condition that $V_{\rm REF} - V_{\rm TH0} \ll \kappa T$ and $\eta V_T \ll \kappa T$, the TC of $V_{\rm REF}$ can be rewritten as

$$\frac{dV_{\rm REF}}{dT} = -\kappa + \frac{\eta k_B}{q} \ln\left\{\frac{6q\eta\kappa}{k_B(\eta-1)} \frac{K_{R1}K_3K_5}{K_4K_6K_7} \ln\left(\frac{K_2}{K_1}\right)\right\} \tag{11}$$

(see the Appendix for the derivation of (11)). Therefore, a zero TC can be achieved on condition that

$$-\kappa + \frac{\eta k_B}{q} \ln\left\{\frac{6q\eta\kappa}{k_B(\eta-1)} \frac{K_{R1}K_3K_5}{K_4K_6K_7} \ln\left(\frac{K_2}{K_1}\right)\right\} = 0. \tag{12}$$

A zero TC voltage can be obtained by setting the aspect ratios K_i in accordance with (12). From (9) and (12), we find that

$$V_{\rm REF} = V_{\rm TH0}. \tag{13}$$

This shows that the circuit generates a voltage equal to the threshold voltage of MOSFETs at 0 K.

Using (6), (8), and (9), we can express current I_P as

$$I_P = K_{R1}\mu C_{\rm OX}\kappa T\eta V_T \ln\left(\frac{K_2}{K_1}\right). \tag{14}$$

The current is determined only by the aspect ratios (K_1, K_2, and K_{R1}) and the temperature coefficient (κ) of the threshold voltage of MOSFETs, and it is independent of $V_{\rm TH0}$. The dependence of κ on process variation is far smaller than that of $V_{\rm TH0}$ as shown in the next section, so current I_P is less dependent on process variations.

The TC of I_P is given by

$$\frac{1}{I_P}\frac{\partial I_P}{\partial T} = \frac{1}{\mu}\frac{\partial \mu}{\partial T} + \frac{1}{T}\frac{\partial T}{\partial T} + \frac{1}{V_T}\frac{\partial V_T}{\partial T}. \tag{15}$$

The temperature dependence of the mobility can be expressed as

$$\mu = \mu_0 \left(\frac{T}{T_0}\right)^{-m} \tag{16}$$

where μ_0 is the mobility at temperature T_0, and m is the mobility temperature exponent [18]. Equations (15) and (16) show that the TC of the current can be given by

$$\frac{1}{I_P}\frac{\partial I_P}{\partial T} = \frac{2-m}{T}. \tag{17}$$

The value of m is about 1.5 in standard CMOS process technologies, so current I_P has a positive TC and increases with temperature.

B. Dependence of Output Voltage on Temperature and Process Variation

The output voltage $V_{\rm REF}$ of our circuit is equal to the threshold voltage of MOSFETs at 0 K, so its value depends on process variation. However, its TC is quite insensitive to process variation and is very small in a wide temperature range. These are discussed in the following.

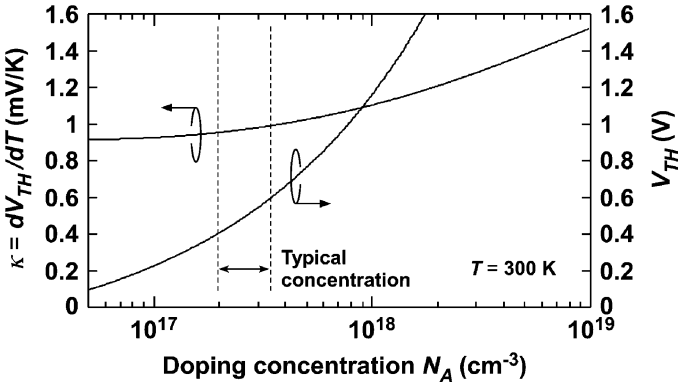

Fig. 2. Threshold voltage ($V_{\rm TH}$) and its TC ($\kappa = dV_{\rm TH}/dT$) as a function of channel doping concentration (N_A), calculated using 0.35 μm standard CMOS parameters at room temperature.

Process variations can be classified into two categories: i.e., within-die (WID) (intra-die) variation and die-to-die (D2D) (inter-die) variation [19]–[21]. The WID variation causes mismatches between transistor parameters within a chip and affects the relative accuracy of the parameters. It can be reduced by using large-sized transistors and various analog layout techniques [21], [22]. In our circuit design, we used a large WL values and a common centroid technique. In contrast, the D2D variation affects the absolute accuracy of transistor parameters and is difficult to reduce with existing techniques. Our circuit generates voltage $V_{\rm REF}$ equal to the threshold voltage of a MOSFET at 0 K, so the D2D variation will directly affect $V_{\rm REF}$. On the other hand, the TC of $V_{\rm REF}$ is quite insensitive to process variations and is very small in a wide temperature range. We show these characteristics with the aid of computer simulation.

The TC of the reference voltage is expressed by (11) and can be set to 0 if (12) is satisfied. Therefore κ (TC of the threshold voltage of MOSFETs) is the key parameter to achieving zero TC operation. The threshold voltage in (8) is theoretically given by

$$V_{\rm TH} = -\frac{E_g}{2q} + \psi_B + \frac{\sqrt{4\varepsilon_{\rm si} q N_A \psi_B}}{C_{\rm OX}},$$
$$\psi_B = V_T \ln\left(\frac{N_A}{n_i}\right), \tag{18}$$

where ψ_B is the difference between Fermi-level potential and intrinsic-level potential, $\varepsilon_{\rm si}$ is the silicon permittivity, N_A is the channel doping concentration, n_i is the intrinsic carrier density, and E_g is the bandgap energy of silicon [17]. Equation (18) shows that the TC, ($\kappa = dV_{\rm TH}/dT$), of the threshold voltage is given by

$$\kappa = -(2\eta - 1)\frac{k_B}{q}\left\{\ln\left(\frac{\sqrt{N_c N_v}}{N_A}\right) + \frac{3}{2}\right\} + \frac{\eta - 1}{q}\frac{dE_g}{dT} \tag{19}$$

where N_c and N_v are the effective densities of states in the conduction and valence bands [17]. From (18) and (19), we find that both $V_{\rm TH}$ and its temperature coefficient κ depend on channel

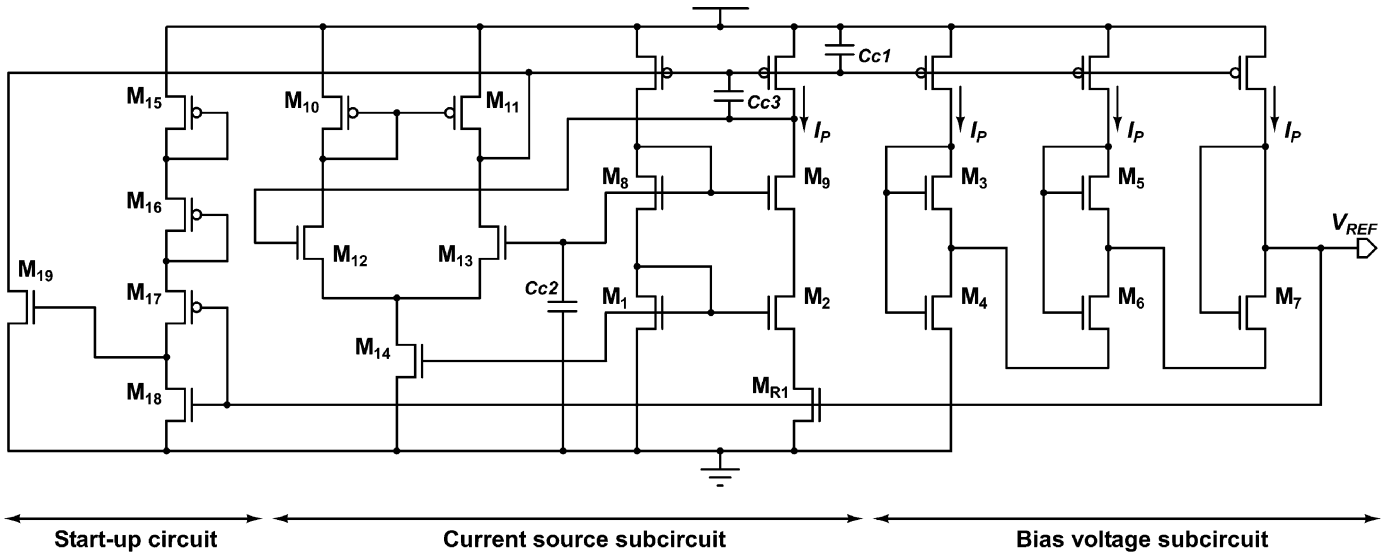

Fig. 3. Entire circuit of our voltage reference. All MOSFETs are operated in subthreshold region, except for MOS resistor $\mathrm{M_{R1}}$, which is operated in strong-inversion, triode region.

doping concentration N_A. This concentration is a process-dependent quantity, so κ can change with process variation. The change is very small, however, because κ is a logarithmic function of N_A. Therefore, the TC of V_{TH} has little dependence on process variation.

To study the effect of process variation on the threshold voltage and its TC, we calculated (18) and (19) numerically using a set of 0.35 μm CMOS parameters at room temperature. Fig. 2 shows the result, a plot of the calculated V_{TH} and κ as a function of N_A. The dashed lines (2.0–3.3 $\times$ 10^{17} cm^{-3}) represent the range of N_A for the CMOS process we used. In this concentration range, threshold voltage V_{TH} changes by $\pm 20\%$ with N_A, while its temperature coefficient κ changes by only $\pm 2\%$. Therefore, the TC of the output voltage hardly depends on process variation.

C. Entire Configuration for Actual Circuit

The entire circuit we designed is illustrated in Fig. 3. Capacitors C_{C1}, C_{C2}, and C_{C3} are used to prevent parasitic oscillation and noise disturbances. A differential amplifier $\mathrm{M_{10}}$–$\mathrm{M_{14}}$ and a current mirror $\mathrm{M_8}$–$\mathrm{M_9}$ are used to increase the power supply rejection ratio (PSRR) to reduce the line sensitivity of the circuit. A start-up circuit $\mathrm{M_{15}}$–$\mathrm{M_{19}}$ is used to avoid the stable state in the zero bias condition. Table I shows the size of transistors $\mathrm{M_1}$–$\mathrm{M_7}$ and $\mathrm{M_{R1}}$.

TABLE I
TRANSISTOR SIZES OF OUR CIRCUIT

Transistor	Value (W/L)
$\mathrm{M_1}$	60 μm / 3 μm = (3 μm / 3 μm) $\times$ 20
$\mathrm{M_2}$	300 μm / 3 μm = (3 μm / 3 μm) $\times$ 100
$\mathrm{M_3}$	252 μm / 3 μm = (3 μm / 3 μm) $\times$ 84
$\mathrm{M_4}$	6 μm / 3 μm = (3 μm / 3 μm) $\times$ 2
$\mathrm{M_5}$	252 μm / 3 μm = (3 μm / 3 μm) $\times$ 84
$\mathrm{M_6}$	6 μm / 3 μm = (3 μm / 3 μm) $\times$ 2
$\mathrm{M_7}$	6 μm / 3 μm = (3 μm / 3 μm) $\times$ 2
$\mathrm{M_{R1}}$	4 μm / 150 μm = (2 μm / 150 μm) $\times$ 2

III. Simulation Results

We confirmed the operation of our circuit with the aid of a SPICE simulation using a set of 0.35 μm standard CMOS parameters and assuming a 1.5 V power supply. To study the dependence of the output voltage on process variations, we performed Monte Carlo simulations assuming both D2D variation (e.g., $\Delta V_{\mathrm{TH}}, \Delta\mu, \Delta T_{\mathrm{OX}}, \Delta L, \Delta W$) and WID variation (e.g., $\sigma_{V_{\mathrm{TH}}}, \sigma_\mu, \sigma_{T_{\mathrm{OX}}}, \sigma_L, \sigma_W$) in transistor parameters. For WID variation, we assumed that every parameter shows a Gaussian distribution that depends on device area (e.g., $\sigma_{V_{\mathrm{TH}}} = A_{V_{\mathrm{TH}}}/\sqrt{LW}$) [19]–[21]. For D2D variation, we assumed a uniform distribution (e.g., $-0.1\ \mathrm{V} < \Delta V_{\mathrm{TH}} < 0.1\ \mathrm{V}$), which shows worst case corners independent of device area [19]–[21]. Let us call a Monte Carlo simulation for a set of parameters a "run".

The results for 300 runs are depicted in Figs. 4 and 5. Fig. 4 shows the dispersion of V_{REF} from the average value ($\overline{V_{\mathrm{REF}}}$) of V_{REF} in the temperature range from -20 to 80°C as a function of D2D threshold-voltage variation ΔV_{TH}. Each open circle shows $\overline{V_{\mathrm{REF}}}$ for a run. As discussed in Section II, V_{REF} varies significantly with each run in a range from 0.7 V to 0.9 V; this reflects the variation in transistor parameters for each run. The value of $\overline{V_{\mathrm{REF}}}$ depends linearly on ΔV_{TH} because the circuit produces the voltage equal to the 0-K threshold voltage of MOSFETs. Fig. 5 shows the distribution of $\overline{V_{\mathrm{REF}}}$. The average of $\overline{V_{\mathrm{REF}}}$ was 840 mV, and the standard deviation was 60 mV. The coefficient of variation σ/μ was 7%, including D2D and WID variations.

IV. Experimental Results

We fabricated a prototype chip, using a 0.35 μm, 2-poly, 4-metal standard CMOS process. Fig. 6 shows a micrograph of

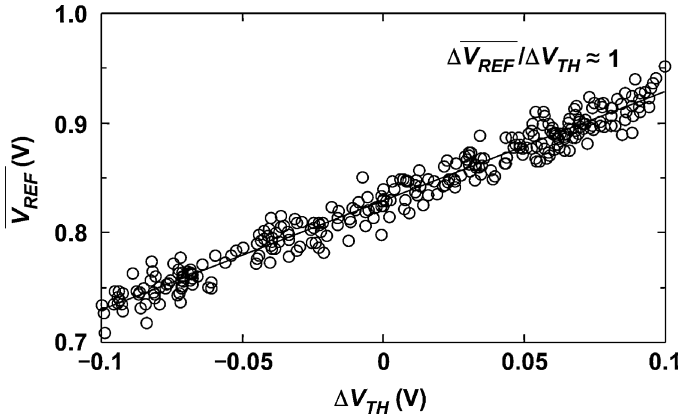

Fig. 4. Average output voltage as a function of D2D variation $\Delta V_{\rm TH}$ of threshold voltage, as obtained from Monte Carlo simulation of 300 runs. Output voltage shows a linear dependence on threshold voltage $(\Delta\overline{V_{\rm REF}}/\Delta V_{\rm TH} \approx 1)$.

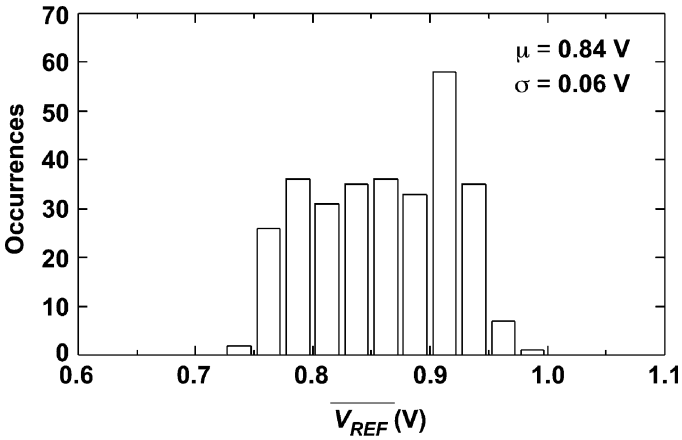

Fig. 5. Distribution of output voltage, as obtained from Monte Carlo simulation of 300 runs.

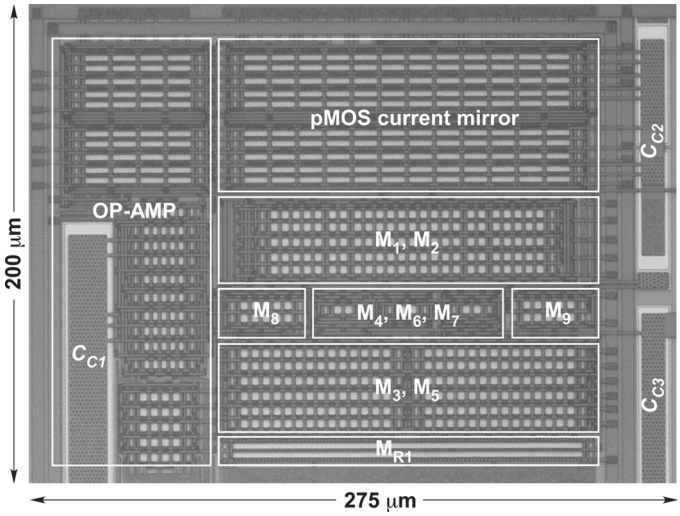

Fig. 6. Micrograph of chip. Chip area is 0.055 mm^2.

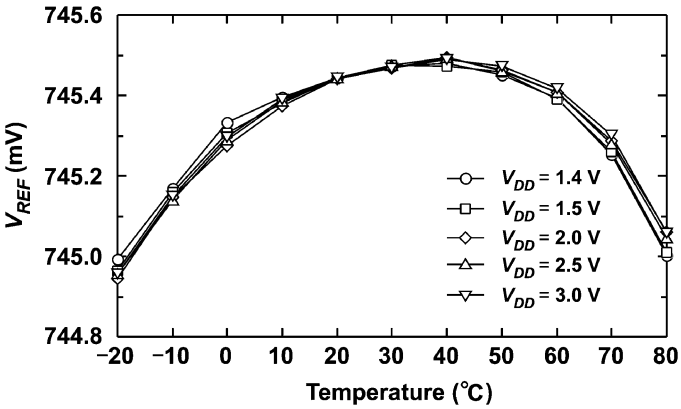

Fig. 7. Measured output voltage $V_{\rm REF}$ as a function of temperature, with various supply voltages. Temperature coefficient was 7 ppm/°C.

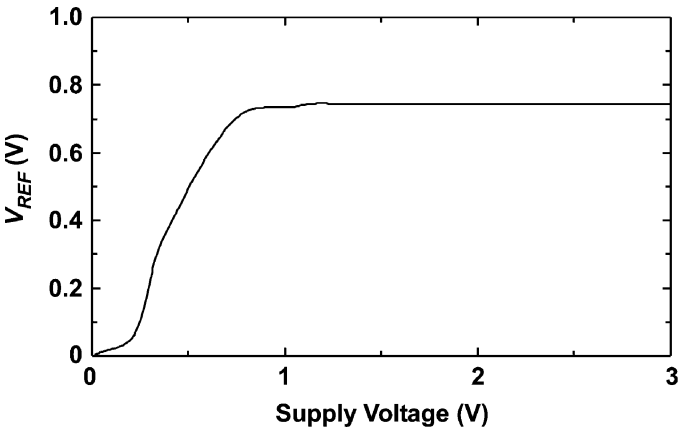

Fig. 8. Measured output voltage $V_{\rm REF}$ at room temperature as a function of power supply. Line sensitivity was 20 ppm/V for supply voltages 1.4–3.0 V.

our chip. The chip area was 0.055 mm^2 (=200 μm × 275 μm). Fig. 7 shows measured output voltage $V_{\rm REF}$ as a function of temperature, with supply voltage $V_{\rm DD}$ as a parameter. Almost constant voltage was able to be achieved. The average of output voltage was 745 mV. The temperature variation was 0.48 mV in a temperature range from −20 to 80°C, so the temperature coefficient was 7 ppm/°C.

Fig. 8 shows output voltage $V_{\rm REF}$ at room temperature as a function of supply voltage. The circuit operated correctly when supply voltage was higher than 1.4 V. The line sensitivity was 20 ppm/V in the power range of 1.4 to 3 V. Fig. 9 shows the power supply rejection ratio (PSRR) at room temperature with a 1 pF filtering capacitor and a 2 V power supply. The PSRR was −45 dB at 100 Hz. Thus, we were able to achieve the voltage reference circuit that was almost independent of temperature and supply voltage.

Fig. 10 shows measured current I_P as a function of temperature, with power supply voltage as a parameter. The current I_P was about 36 nA at room temperature and reached the maximum of 39 nA at 80°C. The power dissipation of the circuit with a 1.5 V power supply was 0.32 μW at room temperature and varied from 0.28 to 0.35 μW at temperatures from −20 to 80°C. The temperature variation of the power dissipation was 0.2%/°C.

To study the D2D variation of our device, we measured 17 samples, each on a different chip, and confirmed their constant-voltage operation. Fig. 11 shows measured output voltage $V_{\rm REF}$ as a function of temperature for a 1.5 V supply voltage. The D2D

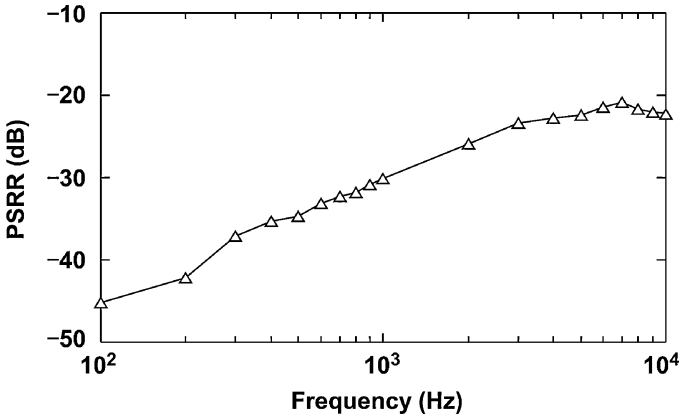

Fig. 9. Measured PSRR at room temperature with 1 pF filtering capacitor and a 2 V supply voltage.

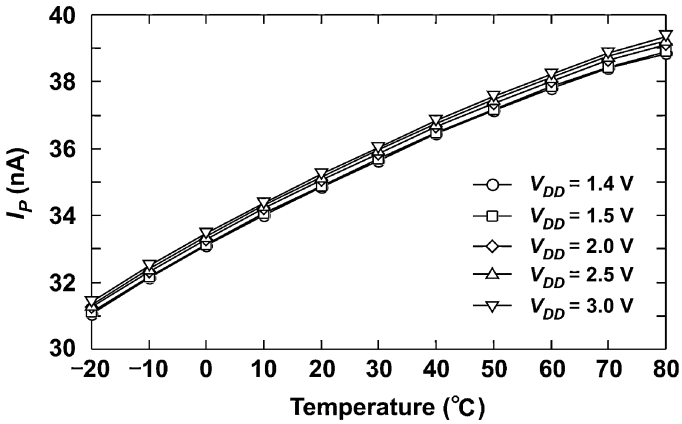

Fig. 10. Measured current I_P as a function of temperature for different supply voltages.

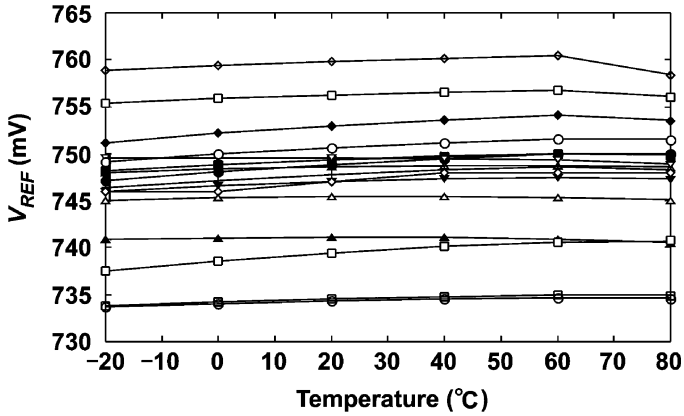

Fig. 11. Measured output voltage $V_{\rm REF}$ as a function of temperature for 17 samples on different chips from same wafer. Supply voltage was set to 1.5 V. Temperature coefficients from 7 to 45 ppm/°C were observed. Average TC was 15 ppm/°C.

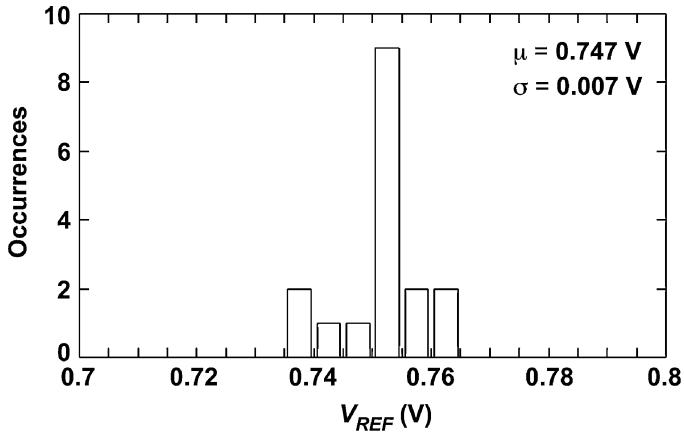

Fig. 12. Distribution of output voltage for 17 samples measured at room temperature.

variation in $V_{\rm REF}$ was 25 mV. This value was far smaller than expected from the Monte Carlo simulation. This is so because the sample chips were fabricated from the same wafer, the variation of the reference voltage became smaller, and in our simulations, we assumed a uniform distribution for the D2D variation. This seems, however, to be an overestimation on the D2D variation, and in practice, a broad Gaussian distribution would be more suitable to represent the D2D variation.

Temperature coefficients from 7 to 45 ppm/°C were observed in the 17 samples. The average TC of $V_{\rm REF}$ was 15 ppm/°C. Fig. 12 shows the distribution of output voltage $V_{\rm REF}$ at room temperature. The coefficient of variation σ/μ was 0.87%.

Table II summarizes the characteristics of our device in comparison with other low-power CMOS voltage references reported in [9]–[13]. Our device is comparable to other circuits in power dissipation, PSRR, and chip area, and it is superior to others in TC and line sensitivity. Our circuit is therefore useful as a voltage reference for power-aware LSIs.

V. Discussion

Regarding other applications, the output voltage of our circuit can be used as a monitor signal for the D2D process variation in MOSFET threshold voltage because the output voltage is equal to the 0-K threshold voltage of MOSFETs in an LSI chip. This output voltage can be used to compensate for the threshold voltage variation in LSI chips. For example, consider the application to a reference current source. The process variation of the current I_P flowing in our circuit [see (14)] can be expressed as

$$\frac{\Delta I_P}{I_P} = \frac{\Delta \mu}{\mu} + \frac{\Delta C_{\rm OX}}{C_{\rm OX}} + \frac{\Delta \kappa}{\kappa}. \tag{20}$$

The current is independent of the threshold voltage variation. Although the current depends on the variation of the mobility $\Delta\mu/\mu$, gate-oxide capacitance $\Delta C_{\rm OX}/C_{\rm OX}$, and the temperature coefficient of the threshold voltage $\Delta\kappa/\kappa$, these variations are far smaller than the threshold voltage variation.

This way, the circuit can be used as an elementary circuit block for on-chip D2D process compensation systems, such as process and temperature compensated current [23].

VI. Conclusion

We developed an ultra-low power CMOS voltage reference consisting of subthreshold MOSFET circuits. The device generates two voltages having opposite TCs, i.e., a MOSFET threshold voltage and a multiple of the thermal voltage, and adds them to produce an output voltage with a zero TC. We

TABLE II
COMPARISON OF REPORTED LOW-POWER CMOS VOLTAGE REFERENCE CIRCUITS

	This work	[9]	[10]	[11]	[12]	[13]
Process	0.35-μm, CMOS	0.35-μm, CMOS	0.6-μm, CMOS	0.35-μm, CMOS	1.2-μm, CMOS	0.18-μm, CMOS
Temperature range	–20 - 80℃	0 - 80℃	0 - 100℃	0 - 70℃	–25 - 125℃	20 - 120℃
V_{DD}	1.4 - 3 V	0.9 - 4 V	1.4 - 3 V	1.4 - 3 V	1.2 V	0.85 - 2.5 V
$\overline{V_{REF}}$	745 mV	670 mV	309.3 mV	579 mV	295 mV	221 mV
Power	0.3 μW(@1.4 V) Room temp.	0.036 μW(@0.9 V) Room temp.	29.1 μW(@3 V) Max. temp.	4.6 μW(@2 V) N.A.	4.3 μW (@1.2 V) N.A.	3.3 μW (@0.85 V) Average
TC	7 ppm/℃	10 ppm/℃	36.9 ppm/℃	62 ppm/℃	119 ppm/℃	271 ppm/℃
Line sensitivity	20 ppm/V	2700 ppm/V	800 ppm/V	6700 ppm/V	N.A.	9000 ppm/V
PSRR	–45 dB(@100 Hz)	–47 dB(@100 Hz)	–47 dB(@100 Hz)	–84 dB(@1 kHz)	N.A.	N.A.
Chip area	0.055 mm^2	0.045 mm^2	0.055 mm^2	0.126 mm^2	0.23 mm^2	0.0238 mm^2

made a prototype chip, using a 0.35 μm standard CMOS process, and demonstrated its operation by measurements. The TC and line sensitivity of the output voltage were 7 ppm/°C and 20 ppm/V. The power dissipation was about 0.3 μW. The circuit will be useful as a voltage reference circuit for a power-aware LSIs such as mobile devices, implantable medical devices, and smart sensor networks.

As other applications, because the reference voltage changes with the process conditions of threshold voltage in each LSI chip, the circuit can be used as an elementary circuit block for on-chip process compensation systems. The reference voltage of the proposed circuit enables us to monitor the D2D process variations in each LSI chip.

APPENDIX

On condition that $V_{\rm REF} - V_{\rm TH0} \ll \kappa T$ and $\eta V_T \ll \kappa T$, the TC of $V_{\rm REF}$ in (10) can be rewritten as

$$\begin{aligned}\frac{dV_{\rm REF}}{dT} &= -\kappa + \frac{\eta k_B}{q}\ln\left\{\frac{6\eta K_{R1}K_3K_5(V_{\rm REF}-V_{\rm TH0}+\kappa T)}{K_4K_6K_7(\eta-1)V_T}\right. \\ &\quad \left.\times \ln\left(\frac{K_2}{K_1}\right)\right\} \\ &\quad + \eta V_T\left\{\frac{1}{V_{\rm REF}-V_{\rm TH0}+\kappa T}\left(\frac{dV_{\rm REF}}{dT}+\kappa\right)-\frac{1}{T}\right\} \\ &= -\kappa + \frac{\eta k_B}{q}\ln\left\{\frac{6\eta K_{R1}K_3K_5\kappa T}{K_4K_6K_7(\eta-1)V_T}\ln\left(\frac{K_2}{K_1}\right)\right\} \\ &\quad + \frac{\eta V_T}{\kappa T}\left(\frac{dV_{\rm REF}}{dT}+\kappa\right)-\frac{\eta V_T}{T} \\ &= -\kappa + \frac{\eta k_B}{q}\ln\left\{\frac{6\eta K_{R1}K_3K_5\kappa T}{K_4K_6K_7(\eta-1)V_T}\ln\left(\frac{K_2}{K_1}\right)\right\} \\ &\quad + \frac{\eta V_T}{\kappa T}\frac{dV_{\rm REF}}{dT} \\ &= -\kappa + \frac{\eta k_B}{q}\ln\left\{\frac{6q\eta\kappa}{k_B(\eta-1)}\frac{K_{R1}K_3K_5}{K_4K_6K_7}\ln\left(\frac{K_2}{K_1}\right)\right\}. \end{aligned} \tag{21}$$

Therefore, (11) can be obtained.

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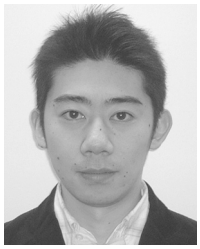

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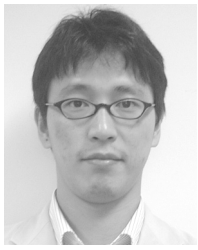

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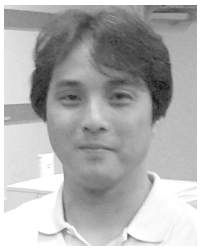

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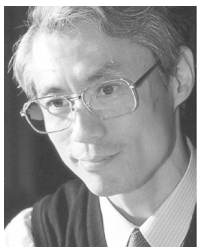

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