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Al_{0.44}Ga_{0.56}N spacer layer to prevent electron accumulation inside barriers in lattice-matched InAlN/AlGaN/AlN/GaN heterostructures

M. Akazawa, B. Gao, T. Hashizume, M. Hiroki, S. Yamahata, and N. Shigekawa

1Research Center for Integrated Quantum Electronics, Hokkaido University, Sapporo 060-6826, Japan
2JST–CREST, Sambancho, Chiyoda-ku, Tokyo 102-0075, Japan
3NTT Photonics Laboratories, NTT Corporation, Atsugi, Kanagawa 243-0198, Japan

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The barrier structure in lattice-matched InAlN/GaN heterostructures with AlGaN-based spacer layers grown by metal organic vapor phase epitaxy was studied by the capacitance-voltage (C-V) method. To investigate the characteristics under positive bias, an Al_{2}O_{3} overlayer was added. The C-V characteristic of a sample with an Al_{0.38}Ga_{0.62}N (5 nm)/AlN (0.75 nm) double spacer layer exhibited an anomalous saturation at a value far below the insulator capacitance under positive bias, which indicated electron accumulation at the InAlN/AlGaN interface. The C-V characteristic of an alternative sample with a single Al_{0.44}Ga_{0.56}N (1.5 nm) spacer layer did not exhibit the anomalous saturation. © 2011 American Institute of Physics [doi:10.1063/1.3578449]

A lattice-matched InAlN/GaN heterostructure provides a high-density two-dimensional electron gas (2DEG) due to the difference in spontaneous polarization at the interface without any doping. To enhance electron mobility, an AlN ultrathin layer has been used as a conventional spacer layer. Several reports have been published on the application of the InAlN/AIN/GaN structure to field-effect transistors (FETs) (Refs. 3–5) including normally off type FETs. A recent study, however, reported that the insertion of an Al_{0.38}Ga_{0.62}N layer improved surface flatness and electron mobility compared with those for a single AlN spacer layer. Since the band gap of an ultrathin AlN layer was deposited by electron-cyclotron resonance chemical vapor deposition using a SiH_{4}/Ar and N_{2} gas mixture at 260 °C. After opening a ring-shaped window by lithography and wet etching using buffered hydrofluoric acid (BHF, HF:NH_{3}F=1:5) solution, a ring-shaped Ti/Al/Ti/Au (30 nm/50 nm/20 nm/100 nm) Ohmic electrode was formed. Then the samples were annealed in N_{2} ambient at 800 °C for 1 min. After removing the SiN_{x} layer using BHF solution, an Al_{2}O_{3} overlayer was deposited by atomic layer deposition (ALD) at a substrate temperature of 250 °C. Finally, a circular Ni/Au (20 nm/50 nm) electrode was formed in the center of the Ohmic ring.

The Hall measurement showed that the In_{0.17}Al_{0.83}N (10 nm)/Al_{0.38}Ga_{0.62}N (5 nm)/AlN (0.75 nm)/GaN heterostructure in Fig. 1(a) produced a 2DEG with a sheet carrier density, n_{s}, of 2.2×10^{13} cm^{-2} and an electron mobility, μ, of 1400 cm^{2}/V s, reproducing the previously reported results. The obtained C-V characteristic for the Al_{2}O_{3}/In_{0.17}Al_{0.83}N/Al_{0.38}Ga_{0.62}N/AlN/GaN structure is plotted in Fig. 2. A step at approximately 0 V can be seen in the C-V curve in addition to the usual step at approximately −11.5 V, indicating the depletion of the 2DEG. From the capacitance values, the plateau at the negative bias corresponds to electron accumulation at the AlN/GaN interface. Even though the positive bias range was limited due to the leakage through the Al_{2}O_{3} layer, the capacitance step at 0 V tends to saturate at a value much lower than the insulator capacitance, C_{i}, of approximately 260 pF. The saturation capacitance corresponds to the value for electron accumulation at

![Schematic sample structures.](image)

**FIG. 1.** (Color online) Schematic sample structures.
the InAlN/AlGaN interface. This phenomenon may become a drawback of the heterostructure if it is applied to an FET gate, resulting in parallel conduction and a complicated change in potential.

Figure 3 shows conduction band, $E_C$, potential profiles with respect to the Fermi level, $E_F$, calculated for the In$_{0.17}$Al$_{0.83}$N/Al$_{0.38}$Ga$_{0.62}$N/AIn/GaN heterostructure by solving the Poisson and Schrödinger equations self-consistently$^7$ for several positions of the surface Fermi level, $E_F$$_{surf}$. The band alignment based on the amphoteric native-defect model$^8$ and related experimental data$^9,10$ was assumed in the calculation, while the interface charge due to polarization was estimated in accordance with Ref. 1. For the sample with an Al$_{0.38}$Ga$_{0.62}$N/AIn spacer layer, it can be seen that applying positive bias leads to electron accumulation at the InAlN/AlGaN interface. In the sample with the Al$_2$O$_3$ overlayer, electron accumulation at the InAlN/AlGaN interface because $E_C$ for the AlGaN layer is closer to $E_F$ than that for the InAlN layer, which is consistent with the measured C-V curve. The spacer layer should be thinner with a wider band gap to prevent electron accumulation inside the barrier layer.

An alternative heterostructure was designed as shown in Fig. 1(b). The Al molar fraction, $x$, of the Al$_x$Ga$_{1-x}$N spacer layer was increased to enlarge the band gap. The critical thickness, however, decreases as $x$ increases. The spacer layer should be as thick as possible to obtain a high 2DEG mobility to separate electrons from the bottom of the InAlN layer, even though it should be sufficiently thin to prevent electron accumulation inside the barrier layer. In addition, an excessively high value of $x$ may result in deterioration of the surface flatness. We, therefore, attempted to increase $x$ slightly from $x=0.38$ to 0.44. The corresponding increase in the conduction band offset relative to GaN was estimated to be about 0.1 eV by the calculation described above.

It was expected that the surface flatness of the InAlN/Al$_{0.44}$Ga$_{0.56}$N/GaN structure could be superior to that of the conventional InAlN/AIn/GaN structure because the lattice mismatch is reduced. To verify this, the surface morphology of the grown heterostructures was investigated using an atomic force microscope (AFM). The results are summarized in Fig. 4. When the thickness of the Al$_{0.44}$Ga$_{0.56}$N layer was greater than 1.5 nm, the number and size of pits increased remarkably as shown in Fig. 4(a) for 2.0 nm thick Al$_{0.44}$Ga$_{0.56}$N on GaN. Therefore, the optimal thickness of the Al$_{0.44}$Ga$_{0.56}$N layer was determined to be 1.5 nm. The surface morphology of 1.5 nm Al$_{0.44}$Ga$_{0.56}$N on GaN shown in Fig. 4(b) was superior to that of an AlN ($\sim$1 nm)/GaN surface$^6$, which led to a smoother InAlN/AlGaN/GaN surface [root mean square roughness (rms): 0.35 nm], as shown in Fig. 4(c), than that of the conventional InAlN/GaN (rms: 0.53 nm) structure. The Hall measurement showed that a 2DEG with $n_S=2.1\times10^{13}$ cm$^{-2}$ and $\mu=1100$ cm$^2$/V s was obtained for the In$_{0.18}$Al$_{0.82}$N/Al$_{0.44}$Ga$_{0.56}$N/GaN heterostructure. Although the mobility is lower for the sample with the Al$_{0.44}$Ga$_{0.56}$N single spacer layer, it is much higher than the typical value of less than 200 cm$^2$/V s for an InAlN/GaN structure without a spacer layer.$^{4,6}$

![Figure 2: Measured C-V curve for the Al$_2$O$_3$ (10 nm)/In$_{0.17}$Al$_{0.83}$N (10 nm)/Al$_{0.38}$Ga$_{0.62}$N (5 nm)/AIn (0.75 nm)/GaN structure. $C_p$ was estimated to be $\sim$260 pF. The bias voltage was swept from the positive side to the negative side at a sweep rate of 25 mV/s.](image)

![Figure 3: (Color online) $E_C$ potential profiles of the In$_{0.17}$Al$_{0.83}$N (10 nm)/Al$_{0.38}$Ga$_{0.62}$N (5 nm)/AIn (0.75 nm)/GaN structure calculated for several $E_F$$_{surf}$ positions.](image)

![Figure 4: (Color online) AFM images for (a) Al$_{0.44}$Ga$_{0.56}$N (2.0 nm)/GaN, (b) Al$_{0.44}$Ga$_{0.56}$N (1.5 nm)/GaN, and (c) In$_{0.18}$Al$_{0.82}$N (12 nm)/Al$_{0.44}$Ga$_{0.56}$N (1.5 nm)/GaN.](image)
and slightly increased as the bias increased toward the onset of electron accumulation at the AlN surface at approximately 4 V. The positive bias limit of this sample, due to the leakage through the Al2O3 layer, was higher than that of the sample with the Al0.38Ga0.62N/AlN double spacer layer in Fig. 2. Since the Al2O3 layer was as thin as 10 nm, its resistivity should have been affected by the roughness and native oxide components of the AlN surface before the deposition. The pretreatment, using the BHF solution to remove the SiNx layer, followed by the sample transfer in air to the ALD chamber was not optimized completely for the AlN surface, which possibly resulted in the difference of the insulator quality between two samples.

In summary, Al2O3 (10 nm)/In0.17Al0.83N (10 nm)/Al0.38Ga0.62N (5 nm)/AlN (0.75 nm)/GaN and Al2O3 (13 nm)/In0.18Al0.82N (12 nm)/Al0.44Ga0.56N (1.5 nm)/GaN structures were fabricated and studied. The C-V characteristic of the former structure exhibited an anomalous saturation at a value far below the insulator capacitance under positive bias, indicating electron accumulation at the AlN/AlGaN interface, while no such saturation was observed in the latter structure. The AlN/Al0.44Ga0.56N (1.5 nm)/GaN structure showed improved surface flatness compared with the conventional AlN/AlN/GaN structure. A 2DEG with $n_s=2.1 \times 10^{13} \text{ cm}^{-2}$ and $\mu=1100 \text{ cm}^2/\text{V/s}$ was obtained by using the Al0.44Ga0.56N single spacer layer. Since thinning the barrier layer is one of the ways of achieving a normally off FET, the AlN/Al0.44Ga0.56N (1.5 nm)/GaN structure with a thin spacer layer is advantageous from this viewpoint.

A calculation employing the same method used for Fig. 3 showed that InAlN (12 nm)/Al0.44Ga0.56N (1.5 nm) should operate normally as a barrier under positive bias as shown in Fig. 5. Actually, the measured C-V characteristic of the Al2O3/In0.18Al0.82N/Al0.44Ga0.56N/GaN structure exhibited a wide plateau as plotted in Fig. 6. The measured capacitance at approximately −3 V had a value corresponding to the electron accumulation at the Al0.44Ga0.56N/GaN interface

![Fig. 5. (Color online) $E_C$ potential profiles of the In0.18Al0.82N (12 nm)/Al0.44Ga0.56N (1.5 nm)/GaN structure calculated for several $E_F$-surf positions.](image)

![Fig. 6. Measured C-V curve for the Al2O3 (13 nm)/In0.18Al0.82N (12 nm)/Al0.44Ga0.56N (1.5 nm)/GaN structure. $C_i$ was estimated to be ~190 pF. The bias voltage was swept from the positive side to the negative side at a sweep rate of 25 mV/s.](image)