Title	Development and outdoor evaluation of an experimental platform in an 80-MHz bandwidth 2×2 MIMO-OFDM system at 5.2-GHz band
Author(s)	Yoshizawa, Shingo; Odagiri, Shinya; Asai, Yasuhiro; Gunji, Takashi; Saito, Takashi; Miyanaga, Yoshikazu
Citation	2010 IEEE 21st International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC), 1049-1054 https://doi.org/10.1109/PIMRC.2010.5672084
Issue Date	2010-09-26
Doc URL	http://hdl.handle.net/2115/47271
Rights	© 2010 IEEE. Reprinted, with permission, from Yoshizawa, S., Odagiri, S., Asai, Y., Gunji, T., Saito, T., Miyanaga, Y., Development and outdoor evaluation of an experimental platform in an 80-MHz bandwidth 2×2 MIMO-OFDM system at 5.2-GHz band, 2010 IEEE 21st International Symposium on Personal Indoor and Mobile Radio Communications (PIMRC), Sep. 2010. This material is posted here with permission of the IEEE. Such permission of the IEEE does not in any way imply IEEE endorsement of any of Hokkaido University products or services. Internal or personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution must be obtained from the IEEE by writing to pubs-permissions@ieee.org . By choosing to view this document, you agree to all provisions of the copyright laws protecting it.
Type	proceedings (author version)
File Information	PIMRC2010.pdf

[Instructions for use](#)

Development and Outdoor Evaluation of an Experimental Platform in an 80-MHz Bandwidth 2x2 MIMO-OFDM System at 5.2-GHz Band

Shingo Yoshizawa*, Shinya Odagiri*, Yasuhiro Asai*, Takashi Gunji†, Takashi Saito†, Yoshikazu Miyanaga*

* Graduate School of Information and Science Technology, Hokkaido University, Sapporo 060-0814, Japan

† Mitsubishi Electric TOKKI Systems Corporation, Tokyo 141-0032, Japan

Abstract—The IEEE802.11ac task group has started to establish a next-generation WLAN standard. The wider channel of more than 80 MHz achieving over a 1-Gbps data rate is discussed. We have developed an experimental platform consisting of baseband and RF units in a 2x2 MIMO-OFDM system for the wider channel and evaluated its system performance in a field experiment. A MIMO-OFDM transceiver in the baseband unit is designed to realize real-time MIMO detection and provide a maximum data rate of 600 Mbps. In the field experiment, we evaluated outdoor propagation characteristics at farm and between buildings for outdoor usage in WLAN systems.

I. INTRODUCTION

A Multiple-input multiple-output (MIMO) technique is commonly used to improve communication reliability or increase data throughput by spatial division multiplexing (SDM). Orthogonal division frequency multiplexing (OFDM) has been known as a powerful technique in equalizing received signals under multipath fading environments. A MIMO-OFDM system, given by combining these techniques, attracts a great deal of attention in current wireless communications. The IEEE802.11n standard supports MIMO-OFDM in a mandatory mode. The IEEE802.11ac task group (TG) has started to establish a next-generation WLAN standard below 6-GHz band [1], [2]. The throughput target is over 1 Gbps at MAC layer. Multi-user MIMO is a key technology to enhance space utilization efficiency under the limited frequency bands. Besides multi-user MIMO, the wider channel, extending a channel bandwidth into more than 80 MHz, is also discussed to achieve high-speed data rates.

While performance achievement of MIMO-OFDM is proven in theoretical modeling and numerical simulation, its hardware development still remains a challenging issue. A large-scale testbed for super 3G and IMT-Advanced systems have been employed in [3] and [4]. A experimental platform on FPGA and DSP boards limits only flat fading test due to the processing latency in MIMO detection [5]. Application-specific integrated circuit (ASIC) is desirable for consumer products, where VLSI implementation of a 4x4 MIMO-OFDM transceiver with a data rate of 192 Mbps is presented in [6]. In our previous work, we have designed 2x2 and 4x4 MIMO-OFDM transceiver LSIs in [7], [8], which provides a maximum data rates of 600 Mbps and 1.5 Gbps in an 80-MHz channel bandwidth, respectively. As a continuation of our work, we have developed a prototype based on baseband and RF units

Fig. 1. Block diagram in a 2x2 MIMO-OFDM transceiver.

in a 2x2 MIMO-OFDM system and evaluated its system performance in a field experiment. In the field experiment, we evaluated outdoor propagation characteristics at farm and between buildings for outdoor usage in WLAN systems. This evaluation meets the needs of outdoor usage model presented in the IEEE802.11ac TG [1]. Our experimental platform and evaluation contribute to providing practical knowledge for IEEE802.11ac WLAN implementations supporting the wider channel.

II. MIMO-OFDM TRANSCEIVER

Figure 1 shows a block diagram of a 2x2 MIMO-OFDM transceiver. The functions in the transmitter and receiver blocks are the same as those of IEEE802.11n PHY. The MIMO detection is used to recover data symbols from spatially multiplexed data streams. We have considered a new frame format for the wider channel of 80 MHz. The OFDM parameters are enumerated at Table I. Based on the 512-point FFT/IFFT, this specification reaches 600 Mbps and 1.5 Gbps in the maximum data rate for 2x2 MIMO and 4x4 MIMO, respectively.

We describe circuit design of the main blocks shown in Fig. 1. In the FFT/IFFT block, a pipeline FFT using a hybrid of Radix-2 and Radix-2² single-path delay Feedback (R2SDF and R2²SDF) architecture [9] is implemented, whose structure is shown in Fig. 2. It enables high speed computation and efficient memory utilization at the lowest clock frequency of a baseband sampling rate. The Viterbi decoder is illustrated

TABLE I
OFDM PARAMETERS FOR THE 80-MHz BANDWIDTH MIMO-OFDM.

Channel bandwidth	80 MHz
Number of FFT/IFFT points	512
Subcarrier frequency spacing	0.1563 MHz
Number of data subcarriers	480
Preamble duration	16 μ s
Symbol duration	7.2 μ s
FFT/IFFT window duration	6.4 μ s
Guard interval duration	0.4 μ s, 0.8 μ s
Supported modulation modes	QPSK, 16QAM, 64QAM
Supported coding rates	1/2, 3/4, 5/6
Maximum Data Rate (PHY)	600 Mbps (2x2 MIMO) 1.5 Gbps (4x4 MIMO)

Fig. 2. Circuit structure in the FFT/IFFT block.

Fig. 3. Circuit structure in the Viterbi decoder block.

in Fig. 3. It consists of an add compare selector (ACS), a survivor path memory (SVPM), and a trace back unit (TBU). We have adopted radix-4 architecture [10] in order to make use of concurrent processing in custom hardware.

Frame structure, block diagram, and processing timing in the MIMO detection block are illustrated in Fig. 4. The MIMO frame consists of a short symbol, long training symbols, and data symbols. The long training symbols $T[k]$ are used for estimating MIMO channel matrix $H[k]$. Each element in the training symbols is expressed as $T_{ij}[k]$ with a i -th symbol index, a j -th stream, and a k -th subcarrier index. At receiving the long training symbols, the MIMO detection block performs channel estimation and matrix inversion given by $G[k] = H[k]^{-1}$ (called as “pre-processing”) on subcarrier-by-subcarrier basis. At receiving the data symbols of $D[k]$, the MIMO block recovers transmitted data symbols by $y_i[k] = G[k] D_i[k]$. If the total processing delay caused by the channel estimation and the pre-processing is shorter than a guard interval time length, the MIMO detection can be performed by real-time operation processing (see “Latency” in Fig. 4). Zero-forcing (ZF) algorithm is simply given by inversion of the channel matrix H . QR decomposition is commonly utilized to

Fig. 4. Frame Structure, block diagram and processing timing in the MIMO detection.

Fig. 5. Circuit structure in the ZF algorithm.

reduce a complexity. However, the complexity for a 2x2 matrix does not so much differ between ZF and QR decomposition. Figure 5 shows the circuit structure in the ZF algorithm. This circuit has 8 pipeline stages including 6-stage complex division and performs pipeline processing on subcarrier-by-subcarrier basis. The total latency is 11 cycles including memory access. It latency time is 137.5 ns by clock frequency of 80 MHz, which is less than the guard interval time length of 400 or 800 ns.

Table II shows a FPGA synthesis result in the 2x2 MIMO-OFDM transceiver where we use Xilinx Virtex-5 XC5VLX330T FPGA device. The 2x2 MIMO-OFDM transceiver has 14 bits in input/output ports with a maximum of 20 bits in arithmetic precision. A maximum clock frequency of 108 MHz is available in this implementation. The utilization of LUTs and registers are evaluated in circuit scale. The total percentage of FPGA utilization is about 20 % at most. The transceiver can be implemented into a target device with the other peripheral circuits (mentioned in Section III.B). The FFT/IFFT processor, the Viterbi decoder, and the MIMO decoder occupy the entire circuit.

TABLE II

FPGA SYNTHESIS RESULT IN THE 2x2 MIMO-OFDM TRANSCEIVER.

Preamble		LUTs	Registers
	Preamble ROM	1,074	76
Transmitter		LUTs	Registers
	IFFT Processor	4,963	1,089
	Others	2,787	9,32
TX Total		7,750	2,012
Receiver		LUTs	Registers
	FFT Processor	8,864	1,338
	MIMO Decoder	7,176	1,831
	Viterbi Decoder	6,880	1,989
	Others	7,248	1,775
RX Total		30,168	6,933
Total (Percentage in FPGA Utilization)		38,992 (19%)	9,021 (4%)

TABLE III

COMPARISON OF THE FIR FILTER IMPLEMENTATIONS.

	Registers	LUTs	DSP Blocks (DSP48Es)
Multiplier (Percentage in FPGA Utilization)	1,204 (0.45 %)	1,152 (0.42 %)	256 (133.2 %)
CSD Representation (Percentage in FPGA Utilization)	11,328 (5.48 %)	6,952 (2.52 %)	0 (0 %)

III. EXPERIMENTAL PLATFORM

A. Structure

Our developed experimental platform is illustrated in Fig. 6. It consists of baseband and RF units. The baseband unit interfaces a FPGA board with a CPU board. The CPU board operates an embedded PC with display and network interfaces. We have developed a GUI-based measurement software on this computer platform in order to evaluate communication performance and characteristics in a field experiment. The measurement software is used for monitoring received signals, a bit error rate (BER), a packet error rate (PER), and signal constellation. The FPGA board executes baseband processing and interfacing with ADC and DAC modules. The RF unit is based on super heterodyne architecture where analog signals are modulated/demodulated at 5200 MHz and 374 MHz for radio frequency (RF) and intermediate frequency (IF) bands, respectively.

B. FPGA Board

The block diagram of the FPGA board is illustrated in Fig. 7. Transmit data sent from the CPU board are encoded and converted into MIMO-OFDM signals in “Data Encoding” and “MIMO-OFDM transmitter”, respectively. The block of “Up sampling” performs low-pass filtering with a flat frequency response. The DAC and ADC modules operate at 200 MHz with double-data-rate (DDR) transfers, which corresponds to

(a) Structure

(b) RF Unit

(c) Baseband Unit

(d) Measurement Software

Fig. 6. Experimental platform.

400 Msps in data sampling rate. We have applied a 100-MHz clock into the MIMO-OFDM transceiver so that baseband signals of 100 Msps can be up-sampled by a factor of four. According to shifting from 80 MHz to 100 MHz in a baseband sampling rate, we changed the number of data subcarriers from 480 to 408 (See Table I). In the up-sampling unit, signals are interpolated and filtered by a low-pass FIR filter. The circuit structure of the designed FIR filter with 64 orders is shown in Fig. 8. It has a polyphase structure given by a single input port and four output ports and operates at a single clock. The output data are fed to DAC modules by changing data transfer architecture (from 100 MHz with four parallel lines to 200 MHz with twist pair lines using DDR transfers). In order to reduce FPGA resource utilization, we have adopted canonic signed digit (CSD) representation for FIR filter coefficients. The CSD representation replaces filter coefficient multiplications with left shift operations and additions [11]. The comparison of the FIR filter implementations for four 64-order FIR filter circuits is shown in Table III. The CSD representation saves DSP block utilization and is suitable for implementing a high-order FIR filter. Power spectrum of the up-sampled signals with/without the low-pass filter is illustrated in Fig. 9. The unnecessary

Fig. 7. Block diagram in the FPGA board.

Fig. 8. Circuit structure of the low-pass FIR filter with a polyphase structure.

side-robe is eliminated by more than 30 dBr due to the low-pass filtering. The shape of power spectrum with an 100-MHz bandwidth can satisfy regulated spectrum mask at 5150-5250 MHz band.

C. RF Transceiver

Architectures of transmitter and receiver in the RF unit are illustrated in Fig. 10. Since non-linear distortion in OFDM causes bit errors and out-of-band spurious radiation, we carefully checked the non-linear distortion by our passband simulation using a non-linear amplifier model. The parameters of level diagrams have been determined by this simulation. In the result, the RF unit requires more than 10-dB back-off in the power amplifier and is capable of communication range up to 100 m in a design level. The other parameters have been based on those of the IEEE802.11a standard.

IV. WIRELESS EXPERIMENT

A. Experimental Condition

In a field experiment, we evaluated system performance in the experimental platform and investigated outdoor propagation characteristics at farm and between buildings. The experimental place and the farm and the passage (between buildings) environments are depicted in Fig. 11. The field experiment was done in Hokkaido University Sapporo Campus and we obtained an experimental radio license at 5150-5250 MHz band in Japan. We fixed a transmitter and moved a

(a) With the low-pass filter

(b) Without the low-pass filter

Fig. 9. Power spectrum with/without the low-pass FIR filter.

Fig. 10. RF transmitter and receiver architectures.

receiver by separating their distance, and evaluated communication performance such as BER, PER, and received SNR. The farm and the passage environments were tested to investigate their contrastive outdoor propagation characteristics. The experimental conditions about antenna types and MIMO-OFDM parameters are enumerated at Table IV. Directional and omni-directional receiver antennas were used to compare their characteristics in a line-of-sight (LOS) channel. Due to the imperfect performance in the baseband and RF units (e.g., sampling clock and frequency synchronization, and auto gain control (AGC)), we used only QPSK in a communication mode, which has a maximum data rate of 133 Mbps in PHY layer.

B. Experimental Results

The evaluation result of throughput performance is shown in Fig. 12. The passage environment gives stable throughput performance regardless of receiver antenna types. On the contrast, the farm environment shows the throughput degradation at longer distances. Use of a directional receiver antenna is more effective than omni-directional at the farm environment.

Next, we measured MIMO channel characteristics by using the received long training symbols indicated in Fig. 4. MIMO channel matrix and received SNR value are computed from the training symbols. The received SNR is given by a ratio of

(a) Experimental Place

(b) Passage between buildings

(c) Farm

Fig. 11. Experimental place and communication environments.

TABLE IV
EXPERIMENTAL CONDITIONS.

Radio Frequency Band	5150 - 5250 MHz
Transmit Power	50 [mW] (Available up to 500 mW in the Experimental Radio License)
TX Antenna (Directional)	NATEC PAT509S-4953 9 dBi / E-Plane 58 deg / H-Plane 76 deg
RX Antenna (Directional)	NATEC VA505A-W52 5 dBi / E-Plane 40 deg / H-Plane 360 deg
RX Antenna (Omni-Directional)	SANSEI ELECTRIC ANTDP-010A0 0 dBi / E-Plane 360 deg / H-Plane 360 deg
Channel	Line of Sight (LOS)
Sampling Rate in DAC/ADC	400 Msps
Communication System	2x2 MIMO-OFDM
OFDM Subcarrier Count	512
Data Subcarrier Count	408
Transmitted Signal Bandwidth	79.68 MHz
Modulation & Coding	QPSK
Coding	Convolutional Coding (Coding Rate 1/2)
Error Correcting	Viterbi Decoding

the measured signal power and noise power. Measured channel capacity of MIMO can be calculated from the MIMO channel matrix and SNR value [12]. We use the following equation:

$$C_{\text{MIMO}} = E \left[\frac{1}{K} \sum_{k=1}^K \log_2 \left(\det \left(\mathbf{I} + \frac{P}{\sigma^2} \mathbf{H}_k \mathbf{H}_k^H \right) \right) \right], \quad (1)$$

where $\mathbf{H}_k$ is a MIMO channel matrix with a k -th subcarrier matrix. P and σ^2 denote received signal power and noise variance, respectively. K is the number of data subcarriers. Figure 13 shows the result of measured channel capacity. The minimum value of 4 bps/Hz in this graph indicates that QPSK modulation with two spatial data streams is available in an ideal MIMO receiver. The measured throughput in Fig. ref4

Fig. 12. Evaluation of throughput performance.

Fig. 13. Evaluation of measured communication capacity.

does not reach this target, however we can observe the similar tendency in the evaluation of throughput performance at the farm environment, i.e., degradation at longer distances and comparison of directional and omni-directional receiver antennas. The evaluation result of eigenvalues, computed from the measured MIMO channel matrix, is presented in Fig. 14. This result is evaluated at the condition of a directional receiver antenna and the farm environment. The higher eigenvalue and lower eigenvalue are expressed as λ_1 and λ_2 , respectively. The lower eigenvalue becomes smaller as the distance increases from 10 m to 30 m. From these measurements, it can be seen that the farm environment gives high MIMO channel correlations for longer distances and causes the degradation of MIMO spatial separation.

V. CONCLUSION

This paper presents the development and outdoor evaluation of an experimental platform in a 2x2 MIMO-OFDM system assuming the wider channel on the IEEE802.11ac standard-ization. The MIMO-OFDM transceiver has been designed in order to support a new OFDM system with an 80-MHz channel bandwidth and achieved real-time MIMO detection by custom hardware design. The experimental platform consists of the baseband and RF units. The baseband unit has 400 Msps at

Fig. 14. Evaluation of cumulative probability in eigenvalues using a directional receiver antenna at the farm environment.

ADC/DAC modules and can satisfy regulated spectrum mask with a flat frequency response by using a high-order low-pass FIR filter. We evaluated system performance in the experimental platform and investigated outdoor communication characteristics at the farm and the passage (between buildings) environments. Our measurement indicated that the farm environment gives high MIMO channel correlation for longer distances and degrades MIMO spatial separation performance. In the future studies, we will improve system performance in the experimental platform and consider a solution to the degradation at the farm environment.

REFERENCES

- [1] Rolf de V, "802.11ac usage models document," doc.:IEEE802.11-09/0161r2.
- [2] Minho C and Peter L, "Proposal for TGac evaluation methodology," doc.:IEEE802.11-09/0376r1.
- [3] Noriaki Miyazaki, Toshihiko Komine, Yasuyuki Hatakeyama, Toshinori Suzuki, "Development and experiments of 100 MHz bandwidth testbed for IMT-advanced systems," IEEE Vehicular Technology Conference (VTC), pp. 1317–1321, Sep. 2007.
- [4] Hidekazu Taoka, Kenichi Higuchi, Mamoru Sawahashi, "Field experiments on real-time 1-Gbps high-speed packet transmission in MIMO-OFDM broadband packet radio access," IEICE Transactions, Vol. 92-B, Issue 5, pp. 1725–1734, May 2009.
- [5] V. Jungnickel, A. Forck, T. Haustein, et al., "1 Gbit/s MIMO-OFDM transmission experiments," IEEE Vehicular Technology Conference (VTC), Vol.2, pp. 25–28, Sep. 2005.
- [6] D. Perels, S. Haene, P. Luethi, A. Burg, N. Felber, W. Fichtner, H. Bolcskei, "ASIC implementation of a MIMO-OFDM transceiver for 192 Mbps WLANs," IEEE European Solid-State Circuits Conference (ESSCIRC), pp. 215–218, Sep. 2005.
- [7] Shingo Yoshizawa, Yoshikazu Miyanaga, "VLSI implementation of a 600-Mbps MIMO-OFDM wireless communication system," IEEE Asia Pacific Conference on Circuits and System (APSCAS), pp.93–96, Dec. 2006.
- [8] Shingo Yoshizawa, Yoshikazu Miyanaga, "VLSI implementation of a 4x4 MIMO-OFDM transceiver with an 80-MHz channel bandwidth," IEEE International Symposium on Circuits and Systems (ISCAS), pp. 1743–1746, May 2009.
- [9] Shousheng He and Torkelson M., "A new approach to pipeline FFT processor," Parallel Processing Symposium, 1996, pp. 766–770, Apr. 1996.
- [10] Peter J. Black and Teresa H. Meng, "A 140Mb/s 32-state radix-4 Viterbi decoder," IEEE Journal of Solid-State Circuits, Vol27, pp.1877–1885, Dec. 1992.
- [11] Zhangwen Tang, Jie Zhang, Hao Min, "A high-speed, programmable, CSD coefficient FIR filter," IEEE Transactions on Consumer Electronics, Vol. 48, Issue 4, pp. 834–837, Nov. 2002.
- [12] G. J. Foschini, M. J. Gans, "On limits of wireless communications in a fading environment when using multiple antennas," Wireless Personal Communications, Vol. 6, No. 3, pp. 311–335, 1998.