Dynamic Wordlength Calibration to Reduce Power Dissipation in Wireless OFDM Systems

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***Abstract*—This paper describes low power architecture by using a dynamic wordlength technique in wireless orthogonal frequency division multiplexing (OFDM) system. The number of wordlength in digital signal processing (DSP) has to be carefully determined because wordlength affects system performance and hardware cost. Dynamic wordlength technique is applied to a fast Fourier transform (FFT) processor and a Viterbi decoder in OFDM receiver. The proposed method searches an optimum wordlength combination of FFT processor and Viterbi decoder by comparing output binary data while changing wordlengths. This operation is done by use of intervals in packet waiting. This approach leads to achieve the power reduction up to 23.9% with a desirable packet error rate (PER) in multipath channel environment.**

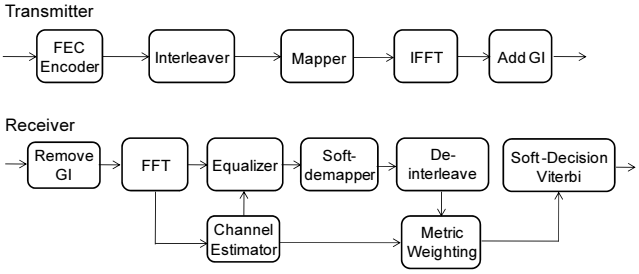

Fig. 1. Wireless OFDM transceiver.

I. Introduction

The orthogonal frequency division multiplexing (OFDM) technique is widely adopted to wireless communication systems such as IEEE802.11a/g/n, Worldwide Interoperability for Microwave Access (WiMAX) and Digital Audio/Video Broadcasting (DAB/DVB-T). Their systems are typically applied to portable electronics devices, which rely on the limited battery, thus, power reduction for hardware architecture becomes an important issue to extend battery time.

The number of wordlength in digital signal processing (DSP) has to be carefully determined because wordlength affects system performance and hardware cost. It is well known that a large wordlength leads to achieve better performance but increase hardware cost. On the other hand, a small wordlength degrades system performance if the dynamic range is insufficient. Variable wordlength technique dynamically changes a wordlength according to dynamic range conditions and can control a trade-off between system performance and power consumption. This technique system is an efficient approach for reducing power dissipation in wireless communication because a dynamic range in wireless systems is sensitive to multipath fading conditions.

Variable wordlength has been applied into an OFDM demodulator [1], [2], an equalizer [3] and to a soft-decision Viterbi decoder [4] for reducing power dissipation in various wireless environments. However, their techniques have considered a single wordlength condition. Applying multiple wordlengths in circuit blocks can reduce power more than a single wordlength because an optimal wordlength depends on individual circuit blocks. Optimization of multiple wordlengths has studied in [5] where a search algorithm has been presented to have different wordlengths in FFT processors, equalizer, and estimator for OFDM demodulator. However, this technique has to be done in circuit design process. We consider optimization of multiple wordlengths while a system is working.

We propose dynamic wordlength calibration which searches optimum wordlengths while an OFDM demodulator is working. In an OFDM demodulator, binary decoded data are outputted from a Viterbi decoder. When a demodulator decrease wordlengths, their output data can be used as a measure of wordlength rounding errors. If a rounding error is trivial, output data in smaller wordlengths are the same as those in maximum wordlengths. Otherwise, the difference can be observed as bit errors in output data. This dynamic calibration is executed during intervals in packet waiting. We apply this technique into a FFT processor and a Viterbi decoder in an OFDM demodulator. Gated clock design [6] is utilized implementing dynamic wordlength variations. This approach can reduce a power by optimizing multiple wordlengths with a desirable packet error rate (PER) for various wireless environments.

II. IEEE802.11a based on OFDM System

IEEE802.11a wireless LAN provides from 6 to 54 Mbps data transmission rate with BPSK, QPSK, 16-QAM, or 64-QAM modulation schemes and 1/2, 2/3 and 3/4 coding rates. Block diagrmas of IEEE802.11a transceiver is shown in Fig. 1. Convolutional encoder with generator polynomials $(133, 171)_8$ and constraint length 7, is used for forward error correction (FEC) coding. Coded bit is interleaved for preventing burst error. The symbols that is after interleaving bit, is mapped according to a various constellation, then a OFDM symbol

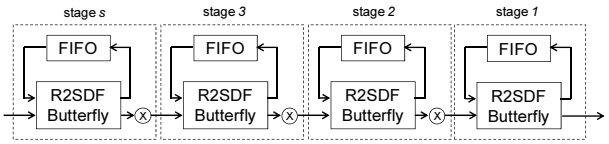

Fig. 2. Pipeline FFT structure.

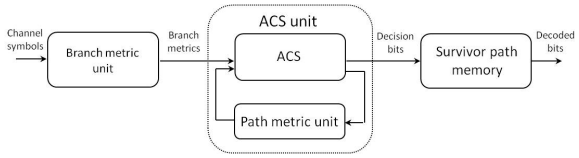

Fig. 3. Block diagram for a Viterbi decoder.

is created by performing N-point IFFT processing. OFDM receiver carry out reversal operation of the transmitter with additional operation. FFT performs demodulating the received symbols which consist of 48 data and 4 pilot subcarriers. Channel equalization is performed by zero forcing algorithm for the IEEE802.11a receiver, assuming slow-fading channels. Then the equalized signal passes to a soft-demapper and de-interleaver for a Viterbi decoding. Soft-decision Viterbi decoder is applied for improving its performance without higher computational cost in OFDM receiver.

III. Fast Fourier Transform and Viterbi Decoder

A. FFT Processor

FFT processor is the most important role in digital signal processing. Time domain symbols are obtained from data symbols using the IFFT at the transmitter, and FFT is performed for obtaining the data with demodulating time domain symbols at the receiver. A pipeline FFT processor, radix-2 single delay feedback (R2SDF) architecture, is designed for OFDM receiver. R2SDF FFT architecture can reduce memory size comparing with radix-2 multi-delay commulator FFT architecture [7]. Figure 2 shows the typical R2SDF pipeline FFT processor implementation. Each FFT stage is composed of first-in first-out (FIFO) memory units and butterfly arithmetic units. Our FFT processor is composed of 64-point with total 6 stages. The gated clocks control the registers of FIFO units.

B. Viterbi Decoder

Soft-decision Viterbi decoding is an attractive solution to improve performance with using multiple quantization levels of signal in OFDM receiver. The modified euclidean distance, which is used for soft decision, calculates for improving performance in fading channel environments [8]. Viterbi decoder is composed of a branch metric unit (BMU), an add-compare-select unit (ACSU), and a survivor path memory unit (SMU) as shown in Fig. 3. BMU measures the distance between the received symbol and reference symbol as a branch metrics. Key feature in Viterbi decoding is an ACSU, which is composed of the add-compare-selector and path metric unit.

TABLE I
Synthesis Results for a FFT and Viterbi Decoder.

	FFT	Viterbi decoder
Technology	CMOS 90-nm	
Clock Frequency	200 MHz	
No. of Logic Gates	71,269	113,117
Maximum Power Dissipation (mW)	21.6	32.3

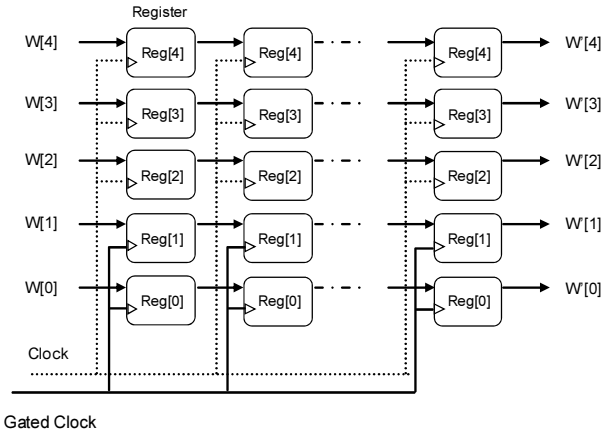

Fig. 4. Gated clock design for registers.

Survivor path is updated by ACSU calculating. A gated clock design is applied with ACSU to control wordlength in Viterbi decoder.

We have designed the FFT processor and Viterbi decoder based on IEEE802.11a standard and synthesized them with the supply voltage 1.0 V and 200 MHz clock frequency in 90-nm CMOS standard cell library. Table I shows the synthesis results of FFT processor and Viterbi decoder for an OFDM receiver. The circuits were designed using Verilog in RTL description. The gated clock design [6] is utilized for implementing dynamic wordlength circuit as shown in Fig. 4. In this example, 5-bit mode can be changed to 3-bit mode by adjusting the gated clocks for the registers. This design is applied with the FFT processor and Viterbi decoder for dynamic wordlength OFDM receiver as shown in Fig. 5 at the section IV.

IV. Proposed System

Dynamic wordlength calibration method finds optimum multiple wordlengths, FFT processor and Viterbi decoder, to reduce power consumption with a desirable communication quality in various wireless environments. 16-bit and 8-bit wordlengths are applied a maximum wordlength (The highest precision) for FFT processor and Viterbi decoder, respectively. FFT processor and Viterbi decoder have different characteristics, which is applied to demodulator and channel decoder, respectively.

Output data of Viterbi decoding is composed of 0 or 1. An example of the output data is for wordlength combinations is shown in Table II. When a demodulator decreases

TABLE II
OUTPUT DATA OF VITERBI DECODING FOR MAX. WORDLENGTH COMBINATION COMPARE WITH DIFFERENT WORDLENGTH COMBINATIONS.

Wordlength (FFT , Viterbi)	Output Data	Hamming Distance for Max. wordlength
16 , 8	1010001001001 … 010110	0
14 , 8	1010001001001 … 010110	0
12 , 8	1010101001001 … 010110	1
…	…	…
12 , 2	1010011001101 … 110110	3
10 , 2	1010011001101 … 100110	4
9 , 2	1110011001101 … 100111	6

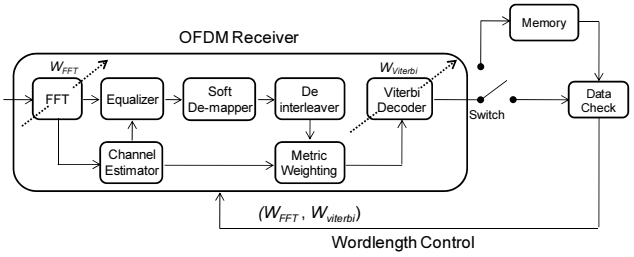

Fig. 5. The proposed dynamic wordlength calibration system for OFDM receiver.

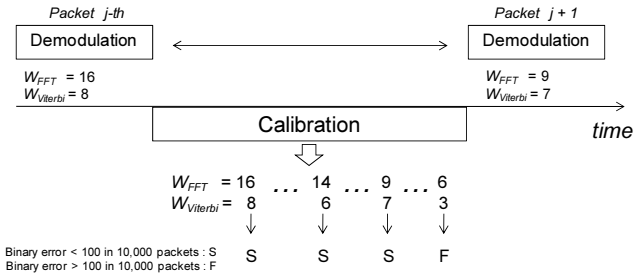

Fig. 6. Wordlength Calibrating between $packetj - th$ and $packetj + 1$.

TABLE III
SIMULATION PARAMETERS.

Multipath Channel Model	HIPERLAN/2 Model A
Modulation	QPSK / 16-QAM / 64-QAM
Number of Data Symbols	40 / 20 / 10
Number of Data Carriers	48
Doppler Frequency	50 Hz
Guard Interval	$0.8\mu s$
FFT Size	64
Error Correcting	Convolutional Code (R = 1/2)
Constraint Length	K = 7
Symbol Timing	Ideal
Packet Counts for Calibration	10,000
Packet Counts	100,000

wordlengths, it degrades a signal-to-noise ratio (SNR) in received signals. However, if the degradation is small, demapper signal detection and error correcting absorbs these rounding errors and do not cause bit errors in output data. It indicates that an OFDM demodulator can reduce wordlengths as long as output data do not increase bit errors. We check hamming distance in output data between a combination of maximum wordlengths (W_{FFT}=16, $W_{Viterbi}$=8) and other combinations. If the distance is not zero, it assumed that a bit error happen due to rounding errors by reducing wordlengths. Hence, we detect a combination of minimum wordlengths having a zero value in the hamming distance, which is treated as optimum wordlengths.

Figure 5 shows the proposed dynamic wordlength calibration system, which is composed of memory and data check block in OFDM receiver. The output data of the Viterbi decoding with the maximum wordlength combination is into the memory to hold its binary data, then data check block is performed to compare it with the others wordlength combinations, and to determine an optimum wordlength combination by counting the number of bit errors. We consider the number of bit errors of 100 in 10,000 packet to prevent a desirable PER between 10^{-2} and 10^{-3}. Therefore, an optimum wordlength combination is detected by a condition S of less than 100 binary errors in 10,000 packet transmission. However, a number of iterative operations are required to compare the number of binary data for 10,000 packet transmission. This operation is difficult to execute during packet receiving. Hence, we make use of intervals at packet waiting where dynamic wordlength calibration is performed between a packet j-th and packet j+1 as shown in Fig. 6. By recording received OFDM signals and output data in Viterbi decoding, an OFDM demodulator can calibrate with trying a lot of different wordlength combinations in empty intervals. As shown in Fig. 6, the combination satisfying the condition of less than 100 bit errors is determined as wordlengths for the next packet.

V. EVALUATION

A. Simulation Parameters

The simulation parameters are described in Table III. The OFDM system based on IEEE802.11a standard [9] was assumed in this evaluation. We used multipath fading channel model (channels A) in HIPERLAN/2 [10]. We used zero forcing algorithm for a channel equalizer in IEEE802.11a receiver, assuming slow-fading channel in indoor environment. We consider using wordlengths of 16, 14, 12, 10, 9 and 8 bits for a FFT processor. The wordlengths of Viterbi decoder between 8 and 2 bits are considered for a dynamic wordlength combination. The power consumption results of (a) FFT and (b) Viterbi decoder are summarized in Table IV.

B. Simulation Results

The PER performance results, for maximum wordlength (16 and 8-bit) and the proposed method with dashed lines and solid lines respectively, appear in Fig. 7. The results show that the desirable PER between 10^{-3} and 10^{-2} can be achieved with the proposed method in multipath channel environment. The determined wordlength combinations for a FFT processor and Viterbi decoder denoted as WD_{FFT}, $WD_{Viterbi}$ are summarized in Table V. The determined wordlength combinations

TABLE IV
POWER CONSUMPTION WITH EACH WORDLENGTHS FOR A FFT PROCESSOR AND VITERBI DECODER.

(a) FFT

Wordlength (No. of bits)	16	14	12	10	9	8
Power (mW)	21.6	17.5	16.2	14.6	14.3	13.6
Ratio	1	0.811	0.753	0.693	0.629	0.629

(b) Viterbi decoder

Wordlength (No. of bits)	8	7	6	5	4	3	2
Power (mW)	32.3	31.4	30.6	29.7	28.8	27.8	26.8
Ratio	1	0.971	0.946	0.918	0.89	0.86	0.83

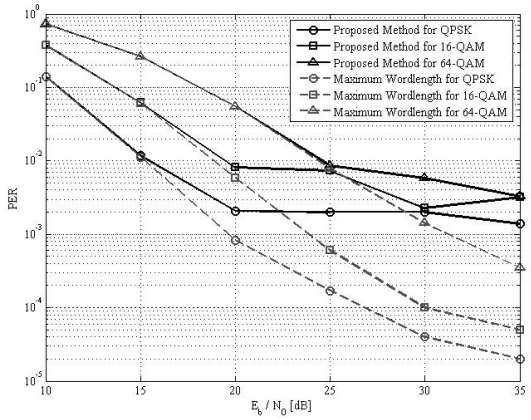

Fig. 7. PER performance for the proposed calibration wordlength combination.

were decreased between 15 and 35dB for QPSK, 16-QAM and 64-QAM modulations. Figure 7 and Table V show that the proposed method can achieve a desirable PER in lower wordlength combinations.

The power value function $P[\cdot]$ at each wordlength is given by Table IV. The power consumption is expressed as

$$Power = P[WD_{FFT}, WD_{Viterbi}] \quad , \tag{1}$$

where the WD_{FFT} and $WD_{Viterbi}$ indicate the determined wordlength of FFT processor and Viterbi decoder, respectively. As shown in Fig. 8, the plots show the power dissipation of QPSK, 16-QAM and 64-QAM modulations, respectively. Our results indicate that the proposed method reduces power dissipation of up to 23.9% with a desirable PER performance under multipath fading environment.

VI. CONCLUSIONS

We have proposed the power reduction method by applying a dynamic wordlength technique with a FFT processor and a Viterbi decoder in wireless OFDM systems. The optimum wordlength combination is determined by utilizing the output data of Viterbi decoding. The simulation results indicated that the proposed method reduced power dissipation of up to 23.9% and 20.7% for 16-QAM and 64-QAM respectively while wireless OFDM system is working with a desirable PER under multipath channel environment.

TABLE V
THE DETERMINED WORDLENGTH COMBINATION FOR QPSK, 16-QAM AND 64-QAM.

Eb/N0 / Modulation	10dB	15dB	20dB	25dB	30dB	35dB
QPSK	16:8	12,8	9,7	10,5	9,2	9,2
16-QAM	16,8	16,8	9,8	10,5	10,3	9,2
64-QAM	16,8	16,8	16,8	12,8	12,3	10,3

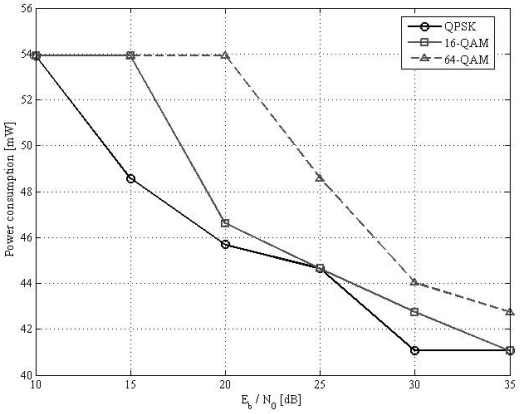

Fig. 8. Power consumption for a FFT and Viterbi decoder with the proposed method under multipath fading channel.

REFERENCES

[1] Shingo Yoshizawa, Yoshikazu Miyanaga, "Tunable wordlength architecture for a low power wireless OFDM demodulator," IEICE Trans. on Fundamentals, Vol. E89-A, pp. 2866–2873, Oct. 2006.

[2] Shingo Yoshizawa, Yoshikazu Miyanaga,"Use of a Variable Wordlength Technique in an OFDM Receiver to Reduce Energy Dissipation," IEEE International Symposium on Circuits and Systems (ISCAS), pp.3175-3178, May 2007.

[3] Kosuke Tarumi, Masanori Muroyama, Seiichiro Yamaguchi, Hiroto Yasuura, "A design method for a low power equalization circuit by adaptive bitwidth control," IEEE International Symposium on Communications and Information Technologies (ISCIT), pp. 704–709, Oct. 2004.

[4] Jaeseong Kim, Shingo Yoshizawa, Yoshikazu Miyanaga, "Design of variable wordlength Viterbi decoder in BICM-OFDM systems," IEEE International Symposium on Communications and Information Technologies (ISCIT), pp. 849–852, Sep. 2009.

[5] Kyungtae Han and Brian L. Evans, "Wordlength optimization with complexity and distortion measure and its application to broadband wireless demodulator design," IEEE Int. Conf. Acoust., Speech, Signal Process. (ICASSP), May 2004, vol. 5, pp. 37–40, May. 2004.

[6] Luca Benini, Polly Siegel, Giovanni De Micheli, "Saving power by synthesizing gated clocks for sequential circuits," IEEE Design and Test of Computers, vol. 11, no. 4, pp. 32–41, Oct. 1994.

[7] Shousheng He, Torkelson, M., "Design and implementation of a 1024-point pipeline FFT processor," Proceedings of the IEEE Custom Integrated Circuits Conference, pp. 131–134, May. 1998.

[8] John Terry, Juha Heiskala, "OFDM Wireless LANs : A Theoretical and Practical Guide," Sams Publishing, 2002.

[9] IEEE Std. 802.11a-1999, "Wireless LAN medium access control (MAC) and physical layer (PHY) specifications: high-speed physical layer in 5GHz band," 1999 edition.

[10] Channel models for HIPERLAN/2 in different in door scenarios," ETSI Doc. 3 ERI085B, Eur. Telecom. Standards Inst., 1998.