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Architectural exploration of embedded systems

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Organization of the verification environment and DUT

Interactions between ISX and the DUT

Example Low Power System Overview

Interactions between ISX and the DUT

Interactions between ISX and the DUT

Example Low Power System Overview

Interactions between ISX and the DUT

Example Low Power System Overview
Example Software Platform - Details

ISX enables layered SW stimulus generation in order to hit all potential HW/SW power management scenarios and capture coverage.

Hibernate Button

Example Software Platform - Details

There are 4 MACs in this simple system. Below there are a multitude of power-down/power-up states and state transitions.

Collecting simulation data, for different architectures

Currently, we fix the architecture, and then simulate the design with many stimuli representing various scenarios. Repeat this for different architectures.

- Can we efficiently collect simulation data over multiple architectures, and then issue various queries to the database?
  - Which architectures have the number of thread activations less than X?
  - For given transactions, which architectures have cache misses less than X on those transactions?

- If we create such a database for some set of architectures, then can we ask such questions for other architectures, without doing the simulations for those architectures?