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Research Article

WPG-Controlled Quantum BDD Circuits with BDD Architecture on GaAs-Based Hexagonal Nanowire Network Structure

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One-dimensional nanowire quantum devices and basic quantum logic AND and OR unit on hexagonal nanowire units controlled by wrap gate (WPG) were designed and fabricated on GaAs-based one-dimensional electron gas (1-DEG) regular nanowire network with hexagonal topology. These basic quantum logic units worked correctly at 35 K, and clear quantum conductance was achieved on the node device, logic AND circuit unit, and logic OR circuit unit. Binary-decision-diagram- (BDD-) based arithmetic logic unit (ALU) is realized on GaAs-based regular nanowire network with hexagonal topology by the same fabrication method as that of the quantum devices and basic circuits. This BDD-based ALU circuit worked correctly at room temperature. Since these quantum devices and circuits are basic units of the BDD ALU combinational circuit, the possibility of integrating these quantum devices and basic quantum circuits into the BDD-based quantum circuit with more complicated structures was discussed. We are prospecting the realization of quantum BDD combinational circuitries with very small of energy consumption and very high density of integration.

1. Introduction

One of the interesting issues for the next-generation LSI technology is how to utilize a variety of quantum devices, for their manipulation of individual electrons, dissipation of little power, and fabrication in sizes ranging to molecular scale. However, on the other hand, it is quite difficult to introduce quantum devices to the current mainstream Si CMOS technology, since extremely precise and very complicated architecture as well as fabrication process is required. A simple circuit technology is necessary. Tucker and Yoshikawa et al. suggested the use of single-electron tunneling transistors in an architecture very similar to CMOS [1, 2]. Likharev and Korotkov proposed reversible logic elements with small energy dissipation per switching event much less than $K_B T$ [3]. At present, there are lots of reports about individual single-electron devices (SET) that work at room temperatures. Those fabrication processes do not allow wires to cross, and no voltage gain existed. These two conditions are necessary for making complex logic circuits. Another problem that SET circuitries are confronting is the parasitic components; the operation of many circuits is completely disrupted by the presence of the parasitic capacitance [4].

Binary decision diagram (BDD) technique provides a possible way to utilize quantum devices due to its simple and graphical logic architecture and passive operation characters with no gain [5, 6]. It is similar to pass gate logic. It has also been applied to non-Si circuits such as rapid single flux quantum (RSFQ) circuits [7, 8]. Recently, a hexagonal BDD logic circuit was proposed and has been developed. A logic function is represented by a directed graph with hexagonal topology [9–11], and the logical structure is directly implemented on a semiconductor nanowire network also having the same topology [10, 11]. This technique makes it possible to simplify design, circuit layout, device structure, and fabrication process. Redundancy available in nanostructures is also useful. Redundant network gives simplicity and flexibility in design and layout. It can give an opportunity to
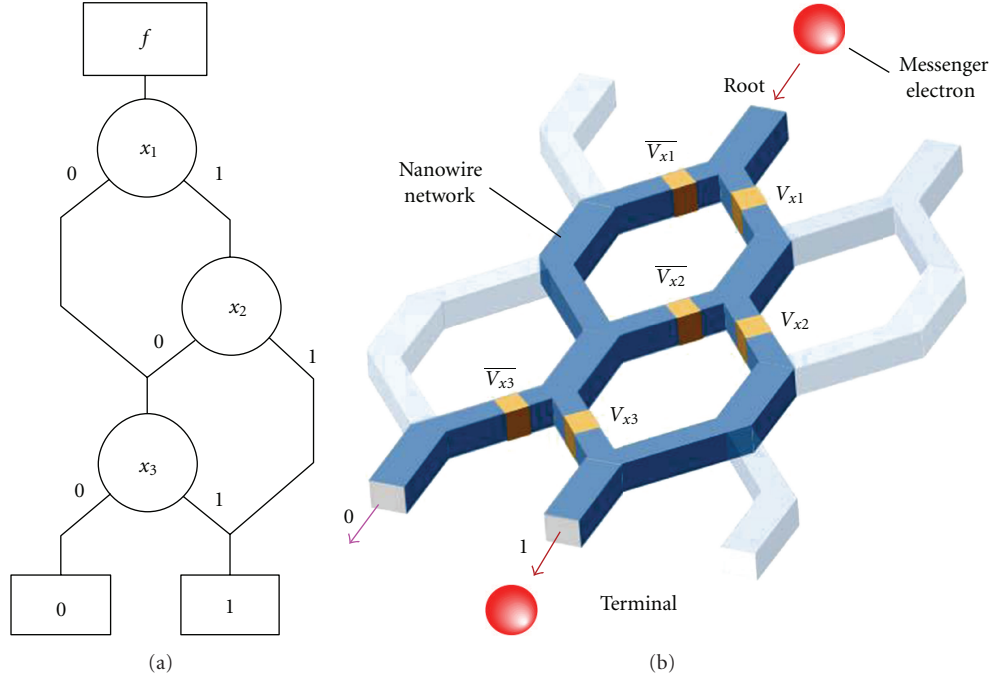
FIGURE 1: (a) Example of circuit with BDD-based logical architecture and (b) method of the physical implementation directly transferred from the graphical logic architecture.

add reconfigurable capability to the circuitry [12]. Successful demonstration of 2-bit full adder [13] and implementation of small signal processor utilizing the hexagonal BDD by circuit simulation [14] has confirmed its feasibility. It is noted that the BDD allows us to use quantum nanodevices such as quantum wire or single-electron transistors in small circuits [11, 15] although these devices have been understood quite difficult to implement conventional logic gate architecture due to small gain, small current drivability, and fluctuation. From the features described above, the hexagonal BDD circuit is found to have better possibility to apply nanowires, their networks, and nanodevices produced by various nanotechnologies to electronic circuits as compared with the Si CMOS logic circuit technology.

In this study, we demonstrate the correct operation of quantum device fabricated on the GaAs-based 1-DEG nanowire and characterized the quantum logic AND and OR units. The capability of the hexagonal BDD circuit to implement a highly functional circuit, ALU, was also characterized. The ALU integrating a set of subsystems is designed with a simple and regular structure and is implemented using GaAs-based hexagonal nanowire network together with Schottky wrap gates (WPGs). From elemental device characteristics and the measured ALU operations, the possibility to operate it in low voltage or in the quantum transport regime is discussed for the future option.

2. Experimental

2.1. Physical Implementation.
Physical implementation method is schematically shown in Figure 1(a). In this study,

hexagonal nanowire network formed of AlGaAs/GaAs heterostructure is used as the host network structure. The logical structure in Figure 1(a) is directly transferred to the physical network structure in Figure 1(b). Logic can be directly verified by checking the physical network structure on the chip even in ALU-level functional circuits. Node devices are implemented by attaching a nanometer-scale Schottky wrap gate (WPG) on each exit branch in the suitable network node, as shown in Figure 2(a) [16]. The WPG controls the carrier density in the channel by the field effect. As the logic input, complementary WPG voltages are given to the two exit branches. The path switching is carried out by on/off the conduction of exit branches by WPGs in complementary fashion. The overall network can be formed with unipolar channel nanowires. Each node device needs neither Ohmic contact nor pn junction. Physical architectures of the device and the circuit and their operations are very simple.

The WPG can squeeze the nanowire electrostatically, and thus, a one-dimensional channel is formed [15, 17]. Therefore, the BDD node device in Figure 2(a) can operate as a quantum wire device which precisely switches the path of a small number of electrons at suitable temperature. Although the quantum wire device with conductance quantization has voltage gain less than unity, the BDD circuit is expected to operate correctly with a passive operation style.

2.2. Fabrication Processes.
The hexagonal nanowire network was fabricated by electron beam (EB) lithography and wet chemical etching on a conventional AlGaAs/GaAs modulation-doped heterostructure wafer. The mobility and carrier density of the 2-dimentional electron gas (2DEG)
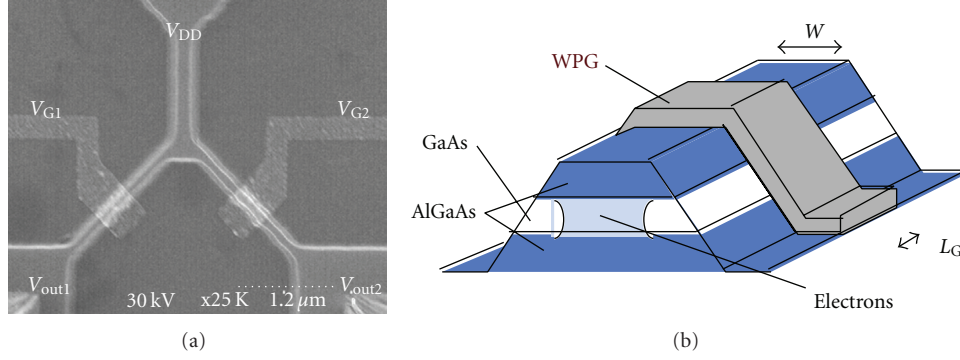
(a)

(b)

Figure 2: (a) BDD node device controlled by WPG and (b) WPG-controlled device structure.
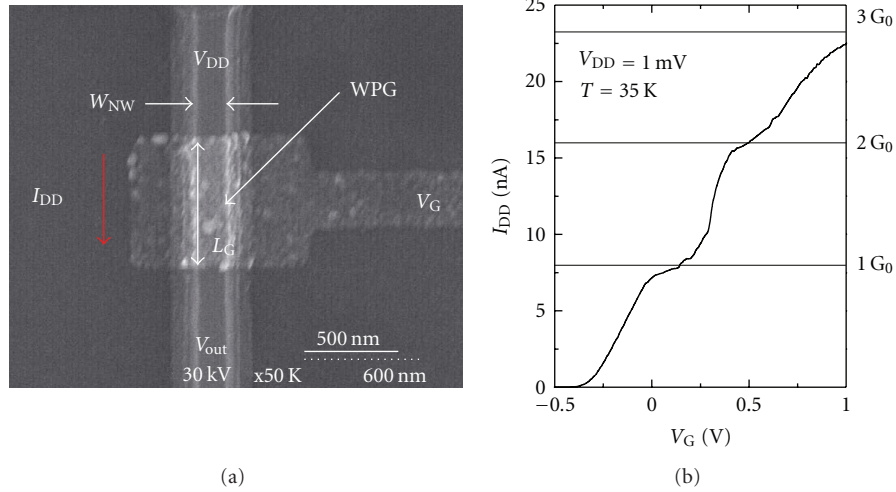

(a)

(b)

Figure 3: (a) SEM image of a quantum device controlled by a WPG on the hexagonal nanowire network (b) quantized conductance of the device measured at 35 K ($G_0 = 2e^2/h$), where V_{DD} is the driving voltage for the device, I_{DD} is the driving current in the 1-DEG channel, V_G is the applied voltage on the wrap gate (WPG), and V_{out} is the output voltage from the device.

were 5.0×10^3 cm^{2}V^{-1}s^{-1} and 1×10^{12} cm^{-2} at 297 K and 1.1×10^5 cm^{2}V^{-1}s^{-1} and 1×10^{12} cm^{-2} at 77 K, respectively. Mean free path was 90 nm at 297 K and 1,800 nm at 77 K. The etching depth was 150 nm, reaching the GaAs buffer. Using an isotropic chemical etching and choosing low index $\langle -110 \rangle$ and $\langle 111 \rangle$ directions, uniform nanowires with facetted smooth sidewalls could be formed. Fabricated nanowire width W_{NW} was typically 100 nm for the quantum conductance devices and 500 nm for ALU circuit. The node density was 2×10^6 nodes/cm^2. Next, Ohmic contacts for the roots and terminals were made by Ge/Au/Ni/Au deposition and subsequent alloying. Then, Schottky wrap gates were formed by EB lithography, Pd/Pt or Cr/Au deposition, and lift-off with a typical length of 600 nm. Interconnect metal lines with 100 nm width were formed at the same level to WPGs. Although they were directly formed on the nanowires without insulators, they did not work as gate, since the threshold voltage was kept in negative by the short channel effect.

3. Experimental Results and Discussion

3.1. Quantum Devices on the 1-DEG Hexagonal Nanowire Network. The 1-dimensional electron gas (1-DEG) device structure is schematically shown in Figure 2(b). Clear quantized conductance was measured at 35 K on a WPG-controlled quantum device, confirming one-dimensional quantum transport controlling a small number of electrons, as shown in Figure 3(b). The typical nanowire width W_{NW} is about 100 nm, with the WPG length L_G 600 nm. Reducing the nanowire width, temperature where the quantum transport took place was found to increase, and the probability of appearance of conductance quantization also increased, and 80% of devices showed the conductance quantization at 30 K when W_{NW} = 200 nm [18]. From viewpoint of circuit application, the abrupt current switch at the edge of the quantized conductance is expected to give ultrasmall input voltage swing [19]. Measured slope of the quantized conductance edge also depended on the temperature as expected
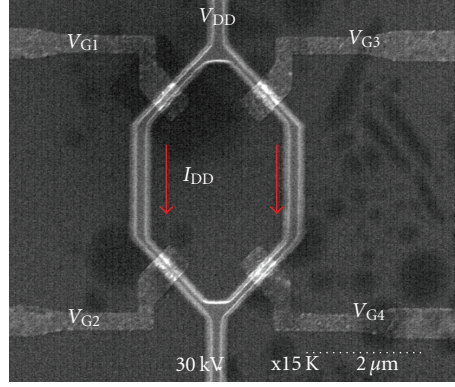
(a)
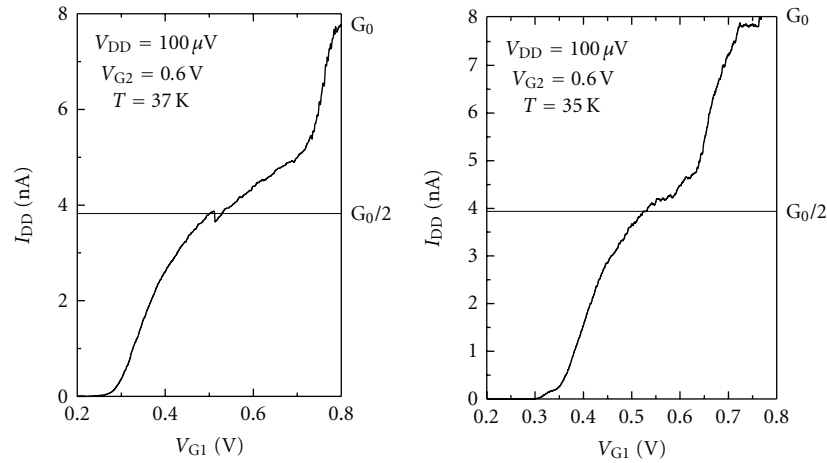
(b)

(c)

FIGURE 4: (a) SEM image of the quantum logic AND and OR units on the hexagonal nanowire unit, (b) left side (when right sides of input voltages were zero), and (c) right side (when left sides of input voltages were zero) of quantized conductance dependence on one input voltage. The parameters in this figure stand for the same meaning as in Figure 3.

theoretically [20]. Very steep edge with large V_G-to-E_F scaling factor of $\alpha = 0.7$ could be obtained by reducing the nanowire width in the present device structure [18] although conventional quantum wire (point contact) devices with split gate structures showed $\alpha < 0.1$ [21]. WPG-controlled nanowire showed small input voltage swing for path switching in wide temperature range.

Logic AND and OR quantum units were fabricated on the GaAs-based hexagonal nanowire unit controlled by four WPGs as shown in Figure 4(a), with about 100 nm of nanowire width and 600 nm of gate length. Experiments were performed at 35 K cooled by a liquid Helium system. When the left or right side of the wrap gate input voltages were set to zero, the other side of the hexagon worked as a quantum logic AND. For example, when $V_{G1} = V_{G2} = 0$ V, the V_{G3} and V_{G4} worked as a quantum logic AND circuit. When the upside or downside of the input voltages is set to a high voltage

level, for example, $V_{G2} = V_{G4} = 0.6$ V, V_{G1} and V_{G3} worked as a quantum logic OR circuit. The quantized conductance characterization was shown in Figures 4(b) and 4(c) for the left side (when right side inputs were zero) and right side (when left side inputs were zero), respectively. Both sides of the circuit can be operated in the quantized conductance region correctly. This provided the possibility for the circuit unit to be applied in the quantum integration circuitries.

3.2. 4-Instruction 2-Bit ALU Circuit on the Hexagonal Nanowire Network.
Figure 5(a) shows an SEM image of the fabricated 4-instruction 2-bit ALU. This unit integrated 32 node devices with 47 WPGs. It was realized by using 3 M nodes/cm^2 fabrication process, in which size of each hexagon was $6 \times 6 \, \mu m^2$. Total circuit area was $70 \times 45 \, \mu m^2$. L_G and W_{NW} were 550 nm and 570 nm, respectively. The fabrication process was completely the same as that for
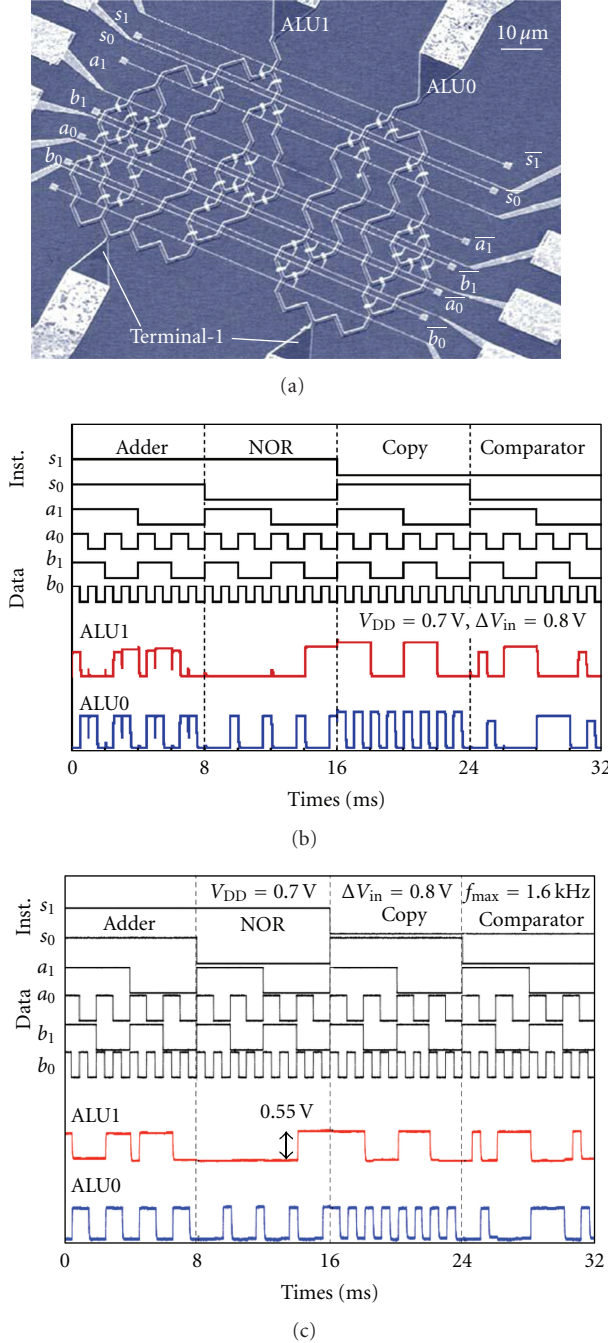
(a)

(b)

(c)

FIGURE 5: (a) SEM image of the fabricated 4-instruction 2-bit ALU on hexagonal nanowire network, (b) measured input-output waveforms, and (c) input-output waveforms obtained from circuit simulation of the ALU circuit.

FIGURE 6: Input voltage swing dependence of the output of the fabricated 4-instruction 2-bit ALU circuit.

discrete node devices. Higher-density fabrication process for 45 M nodes/cm² was already developed [22], which would result in 93% smaller area of the circuit in Figure 5(a).

Measured input-output waveforms are shown in Figure 5(b). In this measurement, supply voltage was applied to the terminals. Output voltages were measured in the roots through 1 MΩ resistance. The Same DC offset voltag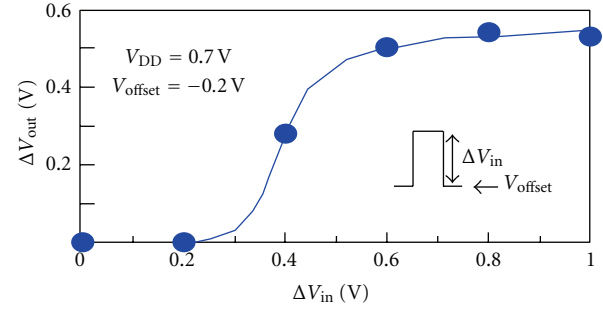e of 0.2 V was applied to all the WPGs except S_1 to obtain uniform high value of outputs. Supply voltage, V_{DD}, of −0.8 V was applied to the roots for sending electron from the root to terminals. Relatively large input voltage swing, ΔV_{in}, of 0.7 V was applied to overcome the threshold variation. The fabricated ALU operated correctly. Obtained output logic values reproduced the result from the circuit simulation in Figure 5(c).

To find possible voltage condition for the ALU operation in detail, input voltage swing dependence of the output was characterized. The obtained result is shown in Figure 6. The fabricated ALU showed output signals when $\Delta V_{in} > 0.2$ V, and V_{out} increased with increasing ΔV_{in}. V_{out} was saturated when $\Delta V_{in} > 0.8$ V, since the WPGs operated in the saturated region of the FET. The threshold of ΔV_{in} is roughly evaluated by the next formula:

$$\Delta V_{in} = \frac{4kT}{\alpha e} + \Delta V_{th}, \tag{1}$$

where α is V_G-to-E_F scaling factor. The former term in the right side of the equation is switching voltage to overcome the thermal energy, kT. The latter term expresses the excess voltage for compensating the V_{th} variation, ΔV_{th}. α can be estimated by $1/\alpha = S_{exp}/\{kT/e\ \ln(10)\}$. S_{exp} is the measured subthreshold swing. This equation is also applicable to the switching in the quantum transport regime [18]. Evaluated ΔV_{in} by (1) with measured α and ΔV_{th} was 0.21 V. This value is reasonably in agreement with the measured value of 0.2 from Figure 6. WPG-controlled nanowire can operate as a quantum wire transistor, and the BDD circuit is also expected to operate in the quantum transport regime, even though the scale of the circuit is increased. It is noted that the quantum wire device has voltage transfer gain less than 1 [23, 24]. According to (1) and measured α in the quantum transport regime, ΔV_{in} was determined by ΔV_{th} rather than input voltage swing, since small ΔV_{in} was obtained in low temperatures. On the other hand, giving enough large ΔV_{in}, the circuit is expected to operate even in the quantum transport regime. Due to the operation principle of the present circuit, V_{DD} can be independently set and can be kept small so as not to smear out the conductance quantization, which is not possible in conventional CMOS logic gate architecture.

4. Conclusion

One-dimensional nanowire quantum devices and basic quantum logic AND and OR unit on hexagonal nanowire units controlled by wrap gate (WPG) were designed and fabricated on GaAs-based regular 1-DEG nanowire network with hexagonal topology and worked correctly at 35 K. BDD-based arithmetic logic unit (ALU) is realized on GaAs-based regular nanowire network with hexagonal topology with the same fabrication process. It exhibits correct output waveforms at room temperature, allowing V_{th} variation of 0.2 V. Applicability for quantum nanodevice is also discussed. These circuits can be fabricated using completely the same process without any special technique.

Acknowledgments

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