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Non-localized trapping effects in AlGaN/GaN heterojunction field-effect transistors subjected to on-state bias stress

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For AlGaN/GaN heterojunction field-effect transistors, on-state-bias-stress (on-stress)-induced trapping effects were observed across the entire drain access region, not only at the gate edge. However, during the application of on-stress, the highest electric field was only localized at the drain side of the gate edge. Using the location of the highest electric field as a reference, the trapping effects at the gate edge and at the more distant access region were referred to as localized and non-localized trapping effect, respectively. Using two-dimensional-electron-gas sensing-bar (2DEG-sensing-bar) and dual-gate structures, the non-localized trapping effects were investigated and the trap density was measured to be $\sim 1.3 \times 10^{12}$ cm^{-2}. The effect of passivation was also discussed. It was found that both surface leakage currents and hot electrons are responsible for the non-localized trapping effects with hot electrons having the *dominant* effect. Since hot electrons are generated from the 2DEG channel, it is highly likely that the involved traps are mainly in the GaN buffer layer. Using monochromatic irradiation (1.24–2.81 eV), the trap levels responsible for the non-localized trapping effects were found to be located at 0.6–1.6 eV from the valence band of GaN. Both trap-assisted impact ionization and direct channel electron injection are proposed as the possible mechanisms of the hot-electron-related non-localized trapping effect. Finally, using the 2DEG-sensing-bar structure, we directly confirmed that blocking gate injected electrons is an important mechanism of Al_2O_3 passivation. © *2012 American Institute of Physics*.
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I. INTRODUCTION

The wide band gap, heterostructure, and polarization-induced high density of two-dimensional electron gas (2DEG) guarantee that AlGaN/GaN heterostructure field-effect transistors (HFETs) have tremendous advantages over other competing technologies in the field of high-voltage and high-power applications, such as high-power radio frequency amplifiers and high-voltage switching devices. However, the performances of these devices have been greatly undermined by so-called current collapse, which was firstly reported by Khan *et al.* in 1994.[1] Since then, the mechanism of current collapse has been intensively investigated,[2] including on-stress ($V_{GS} > V_T$ and high V_{DS})—and off-stress ($V_{GS} < V_T$ and high negative V_{GS}) induced current collapse. Here, V_{GS} and V_{DS} are the gate and drain biases, respectively, and V_T is the threshold voltage. Almost simultaneously, Binari *et al.*[3] and Vetury *et al.*[4] proposed different models to explain current collapse. Binari *et al.* attributed on-stress- and off-stress-induced current collapse to GaN buffer traps and AlGaN surface traps, respectively. Vetury *et al.* proposed the concept of "virtual gate" to explain both types of current collapse. The virtual gate is actually a narrow surface trapping region located in the vicinity of the drain side edge of the metal gate, where the highest electric field exists. Furthermore, very recently, Tajima and Hashizume[5] proposed a third model, in which current collapse can also be induced by surface trapping at the source side of the gate edge, where an electric field of as high as 5 MV/cm exists during the application of off-stress. Owing to the success of using surface passivation to suppress the current collapse,[6–9] the virtual gate mechanism has become widely accepted as the main mechanism for current collapse.[10] Following this understanding, regarding the reliability of AlGaN/GaN HFETs, degradation at the gate edge has been recognized as the only degradation mechanism regardless of whether on-stress or off-stress is applied.[11–14]

In short, the reported trapping and degradation mechanisms of AlGaN/GaN HFETs have mainly focused on the gate edge. Actually, this is reasonable since the highest electric field always exists there regardless of the type of stress. Therefore, such trapping effects at gate edge will be referred to as *localized* trapping effects in the following. However, owing to the effects of surface leakage currents and/or hot electrons, it is highly likely that the trapping region will extend to the entire gate-drain opening during the application of on-stress, which will be referred to as *non-localized* trapping effects in the following.

In fact, for on-stress, Meneghesso *et al.* proposed that a trapping and degradation effect might occur across the *entire* gate-drain opening.[11] They then carried out two-dimensional (2D) numerical device simulations to support this hypothesis.[15] Sometimes, such non-localized trapping effects can even shift the peak of the electroluminescence distribution from the gate edge to the drain edge of an AlGaN/GaN HFET under on-state operation.[16,17] Using cathodoluminescence, Lin *et al.*[18] even directly observed on-stress-induced non-localized degradation in both the source and drain access regions. They also confirmed an enhanced blue band

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(2.8–3.2 eV) emission, which was widely distributed across the access region. Furthermore, in our previous work, we observed that the on-stress-induced trapping region did indeed extend to the entire gate-drain opening.[19] We also observed such an extension of the trapping region in gateless AlGaN/GaN HFETs, suggesting that the non-localized trapping effects might be not related to the high electric field at the gate edge.[20] Although such non-localized trapping effects have been observed by different researchers in different ways, they have not been specifically investigated. Actually, for AlGaN/GaN power-switching devices, the gate-drain distance (L_{GD}) is normally longer than 10 μm. Such non-localized trapping effects should have a strong adverse effect on the performance. In fact, Saito *et al.*[21,22] have pointed out that the operation voltages of these devices are always much lower than the breakdown voltages owing to the increased conduction loss caused by current collapse. To address this issue, they suppressed the high electric field at the gate edge using optimized field plate (FP) structures,[21,22] implying that the non-localized trapping effects were not specifically considered.

In this work, on-stress-induced non-localized trapping effects were specifically investigated using 2DEG-sensing-bar[23] and dual-gate structures. We found that both hot electrons and surface leakage currents are responsible for the non-localized trapping effects observed in our AlGaN/GaN HFETs. Furthermore, it was confirmed that hot electrons have the dominant effect.

Here, we emphasize that we do not intend to question the *localized* mechanisms of current collapse. We are simply discussing another possible mechanism that has not received sufficient attention but should be specifically considered.

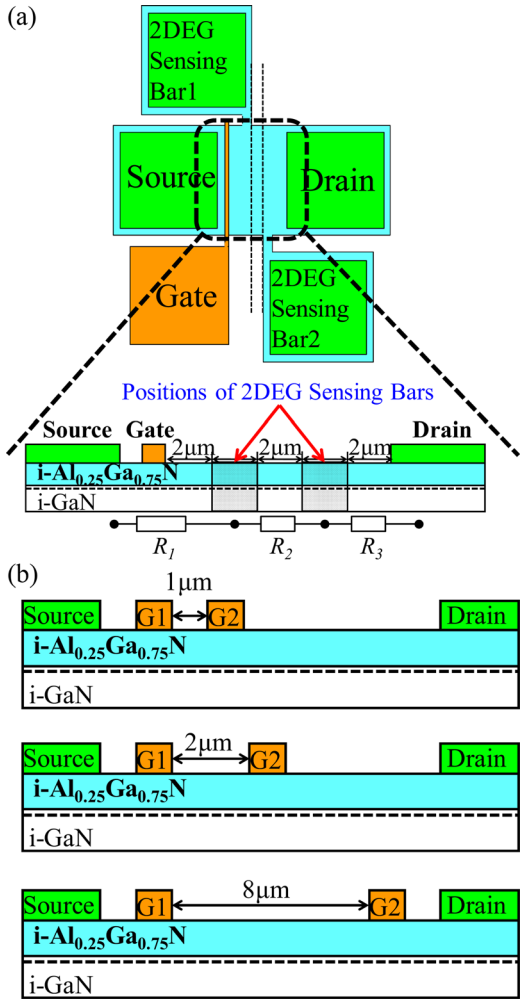

FIG. 1. Device patterns: (a) 2DEG-sensing-bar structure and (b) Dual-gate structure.

II. DEVICE PATTERNS AND EXPERIMENTS

The $Al_{0.25}Ga_{0.75}N$/GaN heterostructure used for this study was grown on a sapphire substrate using a metal-organic chemical vapor deposition (MOCVD) system. The thickness of the AlGaN barrier is 30 nm. Typical values of the electron concentration and the mobility of the 2DEG at room temperature are 1.0×10^{13} cm^2 and 1350 cm^2/Vs, respectively.

The 2DEG-sensing-bar and dual-gate structures are shown in Figs. 1(a) and 1(b), respectively. For both devices, the gate-source distance (L_{SG}), gate length (L_G), and gate-drain distance (L_{GD}) are 1, 1, and 10 μm, respectively. The channel width (W) is 100 μm. Two 2DEG-sensing bars have been defined. They are 2 μm away from the gate and drain contact, respectively. The distance between the 2DEG-sensing bars is also 2 μm. The electrodes on the pads of the 2DEG-sensing bars are in ohmic contact with the 2DEG. Thus, the partial resistances at the gate edge, the center, and the drain edge of the gate-drain access region can be separately measured as R_1, R_2, and R_3, respectively, as shown in the cross-section diagram in Fig. 1(a). For the dual-gate structures, three different patterns were designed with the second gate (G2) 1, 2, and 8 μm away from the first gate (G1), as shown in Fig. 1(b). The L_G for the G2 is 1 μm.

The mesa and electrode patterns were defined by electron beam (EB) lithography using a JEOL JBX-6300SF EB writer. Electron-cyclotron-resonance-assisted reactive ion beam etching (ECR-RIBE) was used to form the isolation. The etching gas was a mixture of $CH_4/H_2/Ar/N_2$ with flow rates of 5/15/3/3 standard cubic centimeters per minute, respectively. Ti/Al/Ti/Au (30/50/20/100 nm) ohmic electrodes were deposited by an EB evaporation system followed by annealing at 800 °C for 1 min in N_2 ambient. Then, Ni/Au (30/50 nm) Schottky electrodes were also deposited by the EB evaporation system. To investigate the effect of passivation, 10 nm of Al_2O_3 and 10 nm of SiN_x were deposited on two different samples using atomic layer deposition (ALD) and electron cyclotron resonance chemical vapor deposition (ECR-CVD), respectively.

An Agilent 4156C semiconductor parameter analyzer was used for all characterizations. To measure the partial resistances R_1, R_2, and R_3 in the on-state, the device with 2DEG-sensing bars was biased as shown in Fig. 2(a). The source was grounded and the gate was biased at 0 V ($V_{GS} = 0$ V). To avoid a thermal effect, the drain was swept from 0 to 0.05 V and the current (I_{IN}) was measured. At the same time, the voltages on the 2DEG-sensing bars (V_{SNS1} and V_{SNS2}) were monitored. In the on-stress state, the device was biased as shown in Fig. 2(b). The gate was biased at 0 V

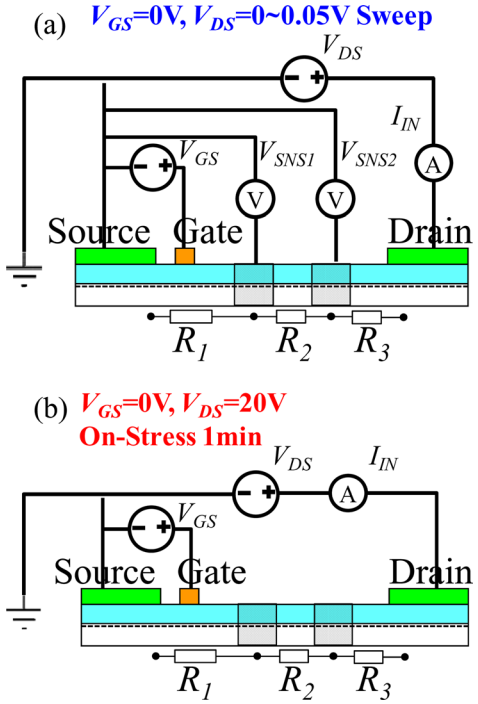

FIG. 2. Measurement configurations of (a) partial resistances R_1, R_2, and R_3 and (b) on-stress condition

and the drain voltage was maintained at 20 V. Except where explicitly stated, the stress time was always 1 min.

To ensure the same initial condition, the devices were first illuminated with microscope incandescent light for 3 min. After that, in dark condition, R_1, R_2, and R_3 were measured before and after application of the on-stress and are denoted as $R_{i,Before}$ and $R_{i,After}$, respectively, where $I = 1$, 2, or 3. Then, the non-localized trapping effects were evaluated by the on-stress-induced resistance variations: $\Delta R_i = R_{i,After}\text{-}R_{i,Before}$.

III. RESULTS AND DISCUSSION

The 2DEG-sensing-bar and dual-gate structures were used to study the trapping mechanisms. It was necessary to confirm that these new structures only serve as sensing terminals and have no effect on device performance. For this purpose, devices with and without the 2DEG-sensing bars were designed and placed adjacent to each other. Similar test patterns were also designed for the dual-gate structure. Figure 3 shows the output characteristics of the devices with and without the 2DEG-sensing bars. No obvious difference was observed. Similarly, the feasibility of the dual-gate structure was also confirmed. The main results are now given in the following six sub-sections.

A. Observation of non-localized trapping effects

Figure 4 shows the on-stress-induced non-localized trapping effects at R_2 and R_3, which correspond to the center and drain edge of the drain access region, respectively, as shown in Fig. 1(a). The data were normalized by $R_{i,Before}$ and denoted as $\Delta R/R$. The error bar data are from 5 devices. The passivation effects of SiN_x and Al_2O_3 films are shown in

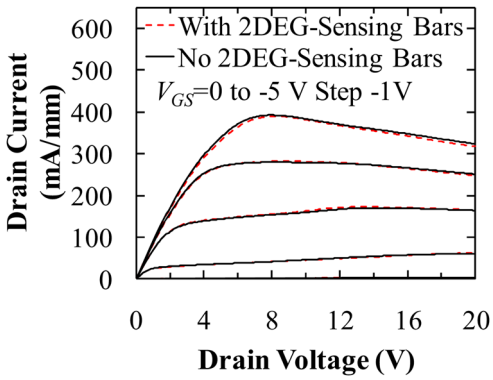

FIG. 3. Output characteristics of the devices with and without 2DEG-sensing bars.

Figs. 4(a) and 4(b), respectively. Both figures show that $\Delta R/R$ is almost the same at R_2 and R_3, indicating that the non-localized trapping effects are reasonably uniform across the drain access region. Passivation slightly reduces the on-stress-induced resistance variations at R_2 and R_3, suggesting that surface traps are involved in the non-localized trapping effects. However, the effect of passivation is limited and the majority of the non-localized trapping effects still exist in the passivated devices.

Since the trapping effects are reasonably uniform across the drain access region, the on-stress-induced variation of 2DEG density (Δn_s) can be estimated as

$$\Delta n_s = \frac{1}{q\mu}\frac{L}{W}\Delta\left(\frac{1}{R_i}\right), \tag{1}$$

where q is the elementary charge, μ is the 2DEG mobility, L is the length of the partial resistance, W is the width of the

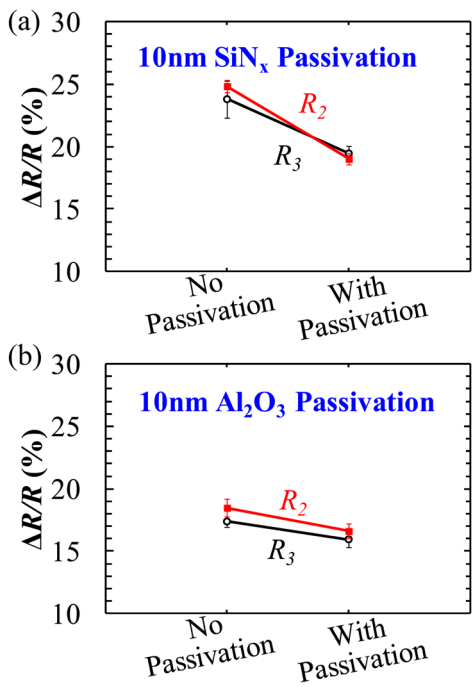

FIG. 4. On-stress-induced resistance variations at the center (R_2) and drain edge (R_3) of the drain access region with (a) SiN_X and (b) Al_2O_3 passivation.

channel, and R_i is the measured partial resistance ($I = 2$ or 3). $\Delta(1/R_i)$ was calculated from $R_{i,Before}$ and $R_{i,After}$.

For unpassivated devices, Δn_s was calculated to be $\sim 1.3 \times 10^{12}$ cm^{-2}, with similar values of Δn_s at R_2 and R_3. Assuming that the horizontal charge distribution is uniform in the AlGaN/GaN heterostructure, the electroneutrality condition in the perpendicular direction should be maintained, giving $\Delta n_s = n_{T,\Delta R}$, where $n_{T,\Delta R}$ is the trap density calculated from ΔR_2 or ΔR_3. Although the location of these traps cannot yet be specified, similar density values have also been reported for the traps on AlGaN surface[24–26] and in GaN buffer.[27,28] The possible location of the observed traps will be discussed in the following subsections.

B. Observation of surface leakage current

Since surface traps are involved in the non-localized trapping effects, a surface leakage current must exist. To confirm this, we used dual-gate devices and directly measured the surface leakage current by the same method as Kotani *et al.* have used.[29] For the investigated dual-gate devices, G2 is 8 μm away from G1. During the measurement, the drain and G2 were grounded and G1 was scanned from 0 to −5 V. By grounding G2 and the drain at the same time, G2 has almost the same potential as the underneath 2DEG. Therefore, the current measured from G2 (I_{G2}) can only come from G1 through surface conduction. We measured the surface leakage currents for the devices with and without 10 nm of ALD-Al_2O_3 passivation. For details of this measurement, please refer to Ref. 29. Figure 5 shows the measurement results. Although the surface leakage current (I_{G2}) only accounts for less than 1/10 or 1/100 of the total gate leakage current (I_{G1}) for the unpassivated and passivated devices, respectively, it does exist and might be responsible for the surface-trap-related non-localized trapping effect. With Al_2O_3 passivation, the surface leakage current was reduced by one order. For our samples, the reduced surface leakage current is consistent with the reduced non-localized trapping effect for the passivated devices. However, we do not intend to correlate the extent of the non-localized trapping effect with the magnitude of the surface leakage current. Actually, many researchers have reported that surface passivation might increase the surface leakage current even if the passivation effect has been confirmed.[30,31] We just want to show that surface leakage currents do exist and it will induce surface-trap-related non-localized trapping effect. If the surface traps were reduced by the passivation, the corresponding non-localized trapping effect will be also suppressed.

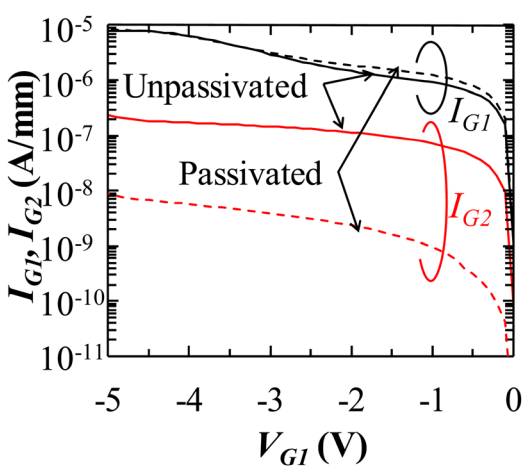

FIG. 5. Surface leakage current observed using a dual-gate structure for the devices with and without 10 nm of Al_2O_3 passivation.

C. Observation of non-localized hot electron effect

Barry *et al.*[32] have theoretically shown by Monte Carlo simulation that hot electrons can be generated at moderate electric fields (several kV/cm). Using the geometry of the fabricated devices ($L_{GS}/L_G/L_{GD} = 1/1/10$ μm), we performed 2D device simulations under the on-stress condition ($V_{GS} = 0$ V, $V_{DS} = 20$ V). Figure 6 shows the simulated horizontal electric field at the 2DEG channel as a function of horizontal position. The electric field at the drain access region is around 7 kV/cm. Therefore, hot electrons can be generated in the drain access region. The hot electrons there are referred to as non-localized hot electrons hereafter. The existence of non-localized hot electrons has also been experimentally demonstrated by Tapajna *et al.*[33] They found that the electron temperature is much higher than the lattice temperature across the entire drain access region for their AlGaN/GaN HFETs in the on-state.

To investigate the non-localized hot electron effect, the dual-gate structures shown in Fig. 1(b) were designed. First, the threshold voltage of G2 (V_{T2}) was measured by $I_{DS}V_{GS}$ scan ($V_{DS} = 0.1$ V, $V_{GS} = 0$ to −6 V) with G1 floating. Then, on-stress was applied to G1 with G2 floating. After that, V_{T2} was measured again with G1 floating, as shown in Fig. 7(a). Figure 7(b) shows that the threshold voltage of G2 is positively shifted by 0.467 V by applying on-stress to G1. For this device, G2 is 8 μm from G1. For the devices with G2 at a distance of 1 and 2 μm from G1, the measured ΔV_{T2} is 0.465 and 0.463 V, respectively. We also applied on-stress to G1 under the illumination of an incandescent lamp and measured ΔV_{T2} in the dark. In this case, no shift of V_{T2} was observed, suggesting that the previously observed ΔV_{T2} was not due to the degradation of the gate metal. Therefore, we can conclude that the positive shift of V_{T2} is only caused by non-localized hot electrons. As a result, ΔV_{T2} can be expressed as

$$\Delta V_{T2} = \frac{q n_{T,\Delta V_t} d_{AlGaN}}{\varepsilon_0 \varepsilon_{AlGaN}}, \quad (2)$$

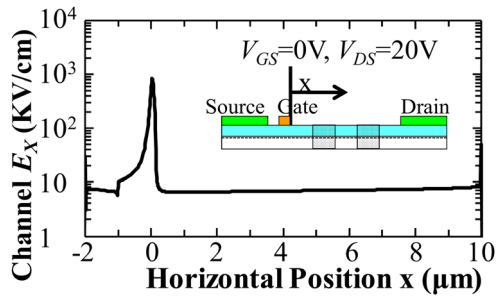

FIG. 6. Simulated horizontal electric field in the channel as a function of horizontal position.

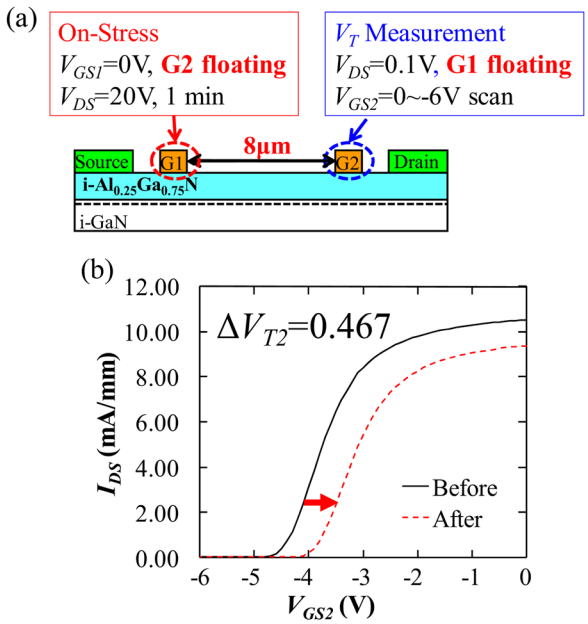

FIG. 7. (a) Measurement method for confirming the hot electron effect and (b) transfer characteristics of G2 before and after applying on-stress to G1.

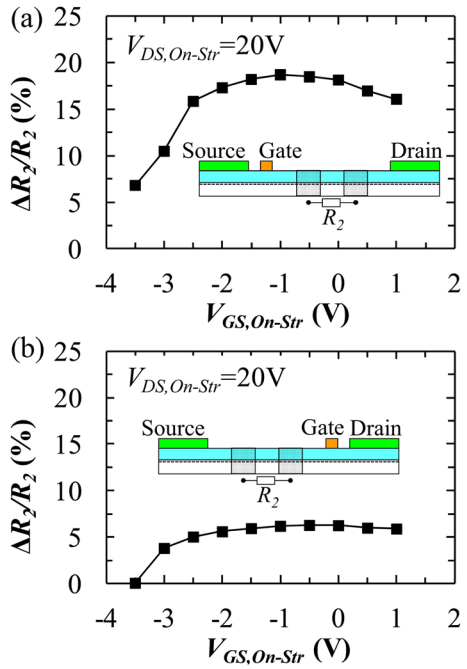

FIG. 8. On-stress-induced resistance variations at the center of (a) drain access and (b) source access regions.

where d_{AlGaN} is the thickness of the AlGaN barrier, $n_{T,\Delta Vt}$ is the trap density exposed by non-localized hot electrons, and ε_0 and ε_{AlGaN} are the vacuum permittivity and relative dielectric constant of AlGaN, respectively. Using this equation, $n_{T,\Delta Vt}$ was calculated to be $\sim 1 \times 10^{12}$ cm^{-2}. By comparison with the value of $n_{T,\Delta R}$ obtained in Subsection III B,we can conclude that the non-localized trapping effects are mainly caused by non-localized hot electrons and that the responsible traps are mainly inside the AlGaN barrier or the GaN buffer, not on the surface. The similar ΔV_{T2} for different distances of G2 indicates that the non-localized hot electron effect is reasonably uniform across the drain access region. This is consistent with the similarity of ΔR_2 and ΔR_3 shown in Fig. 4. Such consistency also shows that the non-localized trapping effects are mainly induced by non-localized hot electrons. It is deserved to be mentioned that Neuburger *et al.* have also used a dual-gate structure to investigate the trapping effect under the second gate.[34] However, the second gate is only 300 nm away from the first gate and is over the passivation dielectric film. Their bias stress is off-stress, different from our approach in this work. Due to these differences, they focused on the charge injection at the gate edge, a localized trapping effect, which is totally different from the non-localized trapping effect observed in this work.

Figure 6 also shows that the electric field in the source access region is similar to that in the drain access region. This is reasonable considering the current continuity condition. Therefore, hot electrons should also exist in the source access region and the non-localized trapping effects might also be observed there. On the same device, we changed the bias polarity during the application of on-stress and measured the on-stress-induced resistance variation. As a result, the same partial resistance (R_2) will be in the drain and source access regions for the conventional and reversed on-stress polarities, respectively, as shown in the insets of Figs. 8(a) and 8(b). Then, the on-stress-induced ΔR_2 can be investigated in the drain and source access regions, as shown in Figs. 8(a) and 8(b), respectively. Under the same on-stress polarity, the drain voltage ($V_{DS,On\text{-}Str}$) was fixed at 20 V and the gate voltages ($V_{GS,On\text{-}Str}$) were changed. When $V_{GS,On\text{-}Str}$ is close to the threshold voltage (~ -4.2 V), ΔR_2 decreases sharply under both polarities, implying that non-localized hot electrons have the dominant effect. The hot-electron-related non-localized trapping effect in the source access region should be similar to those in the drain access region owing to the similar electric field shown in Fig. 6. However, under the reversed on-stress polarity, a large source access resistance is introduced, so the on-stress current is much lower than that under the conventional on-stress polarity. As a result, the observed ΔR_2 in the source access region is much lower than that in the drain access region. This phenomenon also confirmed the hot-electron nature of the non-localized trapping effects in the source access region. Such non-localized trapping effects are consistent with Lin *et al.*'s observation that on-stress-induced non-localized degradation exists in both the source and drain access regions.[18] Figure 8 also shows that ΔR_2 will decrease for higher $V_{GS,On\text{-}Str}$. The mechanism for this phenomenon is not clear, and further investigation is needed.

D. Investigation of trap levels using monochromatic irradiation

To investigate the trap levels, on-stress was applied under monochromatic irradiation (1.24–2.81 eV). The partial resistance R_2 was measured in the dark before and after applying the on-stress, so the investigated traps were directly related to the non-localized trapping effects. Figure 9 shows the normalized variation of R_2 ($\Delta R_2/R_2$) as a function of monochromatic photon energy. The photoionization energies of the traps are between 1.8 and 2.81 eV, suggesting that the

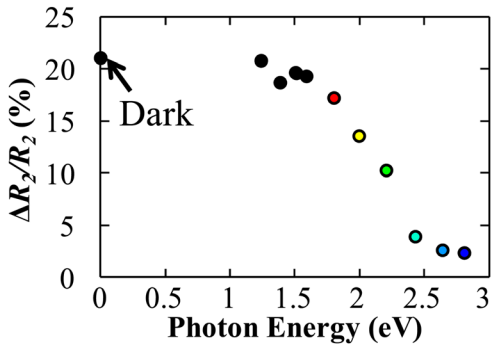

FIG. 9. Effect of monochromatic irradiation on the on-stress-induced resistance variation at the center of the drain access region.

traps might have continuous trap levels[35–37] of 1.8–2.81 eV below the conduction band. Hereafter, unless otherwise stated, all the trap levels are relative to the conduction band edge.

The trap levels in the energy range of 1.8–2.81 eV have been frequently reported. For bulk AlGaN, trap levels of 1.5–2.3 eV were observed in the photo-assisted capacitance transient of AlGaN Schottky diodes.[34] For bulk GaN, using photoionization spectroscopy, Klein *et al.*[38] found trap levels of 1.8 and 2.85 eV were responsible for hot-electron-induced current collapse in GaN metal-semiconductor field-effect transistors (GaN MESFETs). Using the same method, Meneghesso *et al.*[39] came to the same conclusion as Klein *et al.*, but the trap levels were found to be 1.75, 2.32, and 2.67 eV. For AlGaN/GaN HFETs, diverse results have been reported concerning the location of traps. Using photocurrent spectra, Dang *et al.*[36] found continuous trap levels between 2.2 and 3.4 eV in both AlGaN barrier and GaN buffer. Using photoionization spectroscopy, Klein and co-workers[27,40] found the same trap levels in the GaN buffer of AlGaN/GaN HFETs as they had previously found in GaN MESFETs.[38] Using deep-level optical spectroscopy, Nakano *et al.*[41] identified trap levels of ~1.70 and ~2.08 eV at the AlGaN/GaN interface. By photo-assisted CV measurement, Mizue *et al.*[26] observed trap levels of 1.5–2.5 eV on the AlGaN surface of an AlGaN/GaN heterostructure.

Recently, yellow luminescence (YL) at ~2.2 eV and blue luminescence (BL) at ~2.8 eV have been found to be related to the hot-electron-induced kink[42,43] or degradation[18,44,45] effects in AlGaN/GaN HFETs. The YL has been widely recognized as corresponding to a transition between shallow donors and deep acceptors in GaN. The deep acceptors have a typical trap level of ~0.9 eV above the valence band and might be related to Ga vacancies (V_{Ga}).[46,47] The BL has been attributed to deep acceptors (V_{Ga} complexes) at ~2.8 eV (Ref. 48) in GaN. Furthermore, Puzyrev *et al.*[49] carried out a first-principle density-functional calculation and proved the correlation between the YL and the degradation of AlGaN/GaN HFETs. Lin *et al.*[18] located the BL and YL specifically at the GaN buffer layer by depth-resolved micro-cathodoluminescence spectroscopy.

In short, the trap levels observed in our devices have also been reported elsewhere for both AlGaN and GaN. However, among these reports, the traps responsible for hot-electron-induced trapping or degradation effects are mainly in the GaN buffer layer, where the channel hot electrons flow during the application of on-stress. Consistently, it is highly likely that the traps observed in our devices are also mainly located in the GaN buffer layer. On the other hand, the non-localized trapping effects occur in the drain access region far from the gate metal where no vertical gate leakage exists, so the effect of AlGaN barrier traps should be small. In the following, our discussion about the traps and the related hot electron effect will be based on the GaN buffer layer, and we can assume that the trap levels are 0.6 ~ 1.6 eV from the valence band of GaN.

E. Trapping mechanism of non-localized hot electrons

For the non-localized trapping effects, the involved traps are below the midgap of GaN. Upon close examination of Fig. 9, it can be seen that most of the involved traps are close to the valence band and are deep acceptor traps. However, these traps must be empty before the application of on-stress. Meneghesso *et al.* has proposed that these traps might be relatively far from the 2DEG, where the electron density is extremely low and the possibility of electron capture is correspondingly reduced.[42,50] Considering the energy levels of these traps, we think that these traps might be hole traps, which will exchange electrons mainly with valence band.[28] That means the occupancy of these traps will mainly be adjusted by the hole quasi-Fermi level. However, under thermal equilibrium, electron quasi-Fermi level and hole quasi-Fermi level should be coincident with each other and these hole traps should still be filled with electrons. Since we did observe these traps, it is very possible that thermal equilibrium was not achieved before applying the on-stress. In fact, to keep the same initial condition, we always illuminated the devices with microscope incandescent light for 3 min before the on-stress measurement, as Binari *et al.*,[35] Klein *et al.*,[27,38,40] and Meneghesso *et al.*[39] have done. This process will empty all or most of the traps. To investigate the building-up time of thermal equilibrium, we kept the device at $V_{GS} = V_{DS} = 0$ under the dark condition for 30 min after turning off the light. We observed that the increase of R_{ON} is less than 2%. This is much smaller than the on-stress induced variation, as shown in Fig. 4. Therefore, the majority of traps are still empty before the on-stress measurements. This observation is consistent with Megeghesso's data shown in Ref. 50, where they can observe the trap-related kink effect after keeping the device under dark for 5 min. This means that it takes at least 5 min to fill the traps.

Actually, many researchers have observed hole traps in AlGaN/GaN heterostructures. Hu *et al.*[28] have directly observed hole traps in the buffer layer of AlGaN/GaN HFETs regrown on a p-GaN substrate layer. Recently, Meneghini *et al.*[51] observed that hole injection from a p-type gate causes detrapping, suggesting the hole-type nature of the traps in their gate-injection transistors. Polyakov *et al.*[52] identified hole traps of 0.6 ~ 1.2 eV in n-GaN grown by different methods. Saadaoui *et al.* observed hole traps of 0.75 eV in their AlGaN/GaN Schottky barrier diodes.[53]

The non-localized hot electrons might simply be injected into the deep acceptor traps.[42,43,50] They also might knock out the valence band electrons into these traps. This trap-assisted impact ionization process might occur at relatively low electric field.[42,43,50] We hereafter refer to this as non-localized impact ionization. In this process, the impact-ionized electrons are captured by the deep acceptor traps, causing the variation of 2DEG density. Therefore, the on-stress-induced Δn_s at R_2 is proportional to the non-localized impact ionization coefficient.

For impact ionization, the logarithm of the impact ionization coefficient (α_n) has a linear relationship with the reciprocal of the electric field ($1/E$).[54] An impact-ionized hole current[55,56] or gate-edge electroluminescence (EL) (Refs. 11 and 43) should be observed for the impact ionization induced at the gate edge. Meneghesso *et al.*[11] used the ratio of gate-edge EL intensity to drain current ($\text{Intensity}_{EL}/I_{DS}$) to quantify the impact ionization coefficient. For the reciprocal of the electric field, they used $1/(V_{DS}\text{-}V_{DSAT})$ assuming that gate-edge depletion width is the same for different V_{DS}, where V_{DSAT} is the drain saturation voltage. Then, they confirmed the occurrence of impact ionization from the linear relationship between $\log(\text{Intensity}_{EL}/I_{DS})$ and $1/(V_{DS}\text{-}V_{DSAT})$.

In this work, the on-stress-induced Δn_s at R_2 was used to quantify the non-localized impact ionization. Using the 2DEG-sensing bars, the electric field (E) at R_2 can be directly measured. Under fixed $V_{GS,On\text{-}Str}$, different $V_{DS,On\text{-}Str}$ were applied on the same device. For each on-stress condition, $\Delta n_s/I_{DS}$ and $1/E$ at R_2 were measured. Figure 10 shows a semilog plot of $\Delta n_s/I_{DS}$ versus $1/E$. The linear relationship is confirmed, indicating that trap-assisted impact ionization might be responsible for the non-localized trapping effects. At the moment, the occurrence of non-localized impact ionization is only a hypothesis. To finally confirm such a mechanism, it is necessary to measure the impact-ionized hole current generated at R_2. This is very difficult since the impact ionization at the gate edge will also generate a hole current. Therefore, it must be emphasized that, we cannot yet determine the exact trapping mechanism of non-localized hot electrons and both trap-assisted impact ionization and direct hot electron injection are possible.

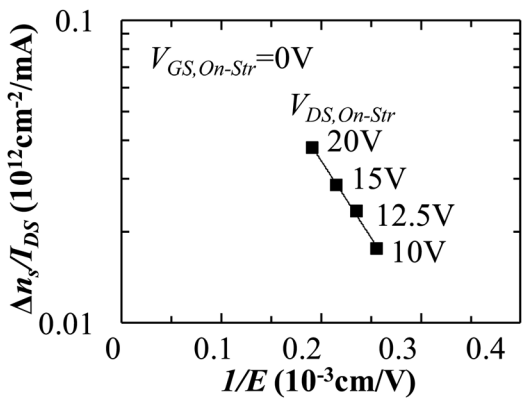

FIG. 10. Ratio of on-stress-induced variation of 2DEG density (Δn_s) to drain current as a function of reciprocal of electric field at the center of the drain access region.

F. Charge injection effect at the gate edge

Using scanning Kelvin probe microscopy, Sabuktagin *et al.*[24] and Koley *et al.*[57] have directly observed charge injection at the gate edge. Using the 2DEG-sensing bars, such an effect can also be observed.

We applied $V_{GS,On\text{-}Str}$-dependent on-stress to the same AlGaN/GaN HFET device with $V_{DS,On\text{-}Str}$ fixed at 20 V. Before the on-stress was applied, the device was illuminated with microscope incandescent light for 3 min to induce detrapping. The on-stress-induced resistance variations were separately measured at the gate edge (ΔR_1) and the center (ΔR_2) of the drain access region. Figures 11(a) and 11(b) show the measured results for unpassivated and passivated devices, respectively, where the passivation film was 10 nm Al_2O_3 deposited by ALD. Without passivation, Fig. 11(a) shows that ΔR_1 increases with decreasing gate voltage, suggesting that a higher electric field at the gate edge causes more charge injection. However, for the passivated devices (Fig. 11(b)), such a tendency disappears and ΔR_1 exhibits the same behavior as ΔR_2, suggesting that passivation substantially suppresses charge injection at the gate edge, and the trapping mechanism at R_1 becomes similar to that at R_2. This result indicates that Al_2O_3 passivation can suppress current collapse by blocking the electrons injected from the gate metal.[5,58] To the best of our knowledge, this is also the first time that such an effect has been directly observed. As for other dielectric films, more investigations are undergoing to evaluate their effect on charge injection.

G. The overall picture of non-localized trapping effects

From the above results, we can now describe the overall picture of non-localized trapping effects, as shown in Fig. 12. Both surface leakage currents and hot electrons can induce the non-localized trapping effects. The presence of the surface leakage current was verified by directly measuring the surface current at G2, 8 μm from G1 (Fig. 5). The surface leakage currents cause trapping at surface traps

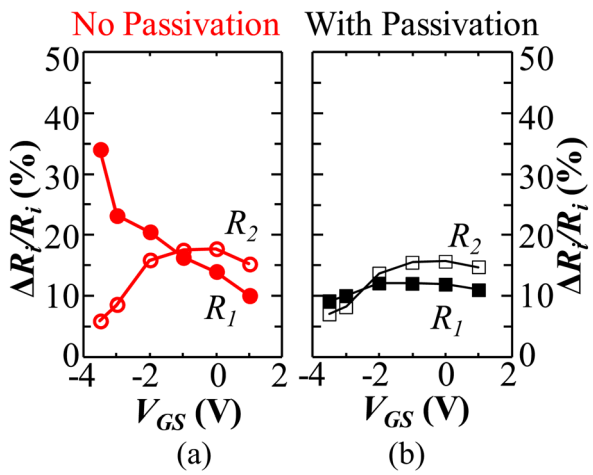

FIG. 11. (a) On-stress-induced charge injection at the gate edge (R_1) for the device without passivation and (b) suppression of charge injection at the gate edge with a 10 nm Al_2O_3 passivation film.

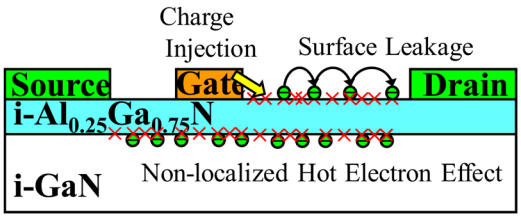

FIG. 12. Overall picture of the on-stress-induced trapping effects in AlGaN/GaN HFETs.

across the entire drain access region. This was verified by the fact that passivation can reduce the on-stress-induced resistance variations at the center and drain edge of the drain access region, as shown in Fig. 4. The effect of hot electrons was confirmed by Fig. 7, where the shift in G2 threshold voltage is induced by applying on-stress to G1 even when G2 is 8 μm away from G1. Figure 8 indicates that hot electrons induce non-localized trapping effects in both the source and drain access regions. Therefore, in the schematic diagram of Fig. 12, we indicate the non-localized hot electron effects across the entire channel from the source to the drain. Furthermore, the surface leakage currents and hot electrons do not contribute equally to the non-localized trapping effects with the hot electrons having the dominant effects. This was verified by the small difference between $n_{T,\Delta R}$ and $n_{T,\Delta Vt}$, as discussed in Subsection III C.

In addition to the non-localized trapping effects, the strong gate-edge electric field also induces a charge injection effect at the gate edge, as shown in Fig. 11. This is consistent with the virtual gate mechanism, the dominant mechanism of current collapse. Figure 12 also depicts this effect.

IV. CONCLUSION

Using 2DEG-senging-bar and dual-gate structures, we investigated the on-stress-induced trapping effects. We found that the trapping effects were not only localized at the gate edge but also appeared in both the source and drain access regions far from the gate edge. We refer to such trapping effects as non-localized trapping effects. Both surface leakage currents and hot electrons are responsible for the trapping mechanisms. However, the hot electrons have the dominant effect. From the resistance variation at the center of the drain access region, the trap density was calculated to be $\sim 1.3 \times 10^{12}$ cm^{-2}. In the case of applying on-stress under monochromatic irradiation, the trap levels were determined to be 0.6–1.6 eV from the valence band of GaN. We proposed trap-assisted impact ionization and direct hot electron injection as the mechanisms of the hot-electron-related non-localized trapping effects.

Using the 2DEG-sensing-bar structure, we also confirmed the existence of a charge injection effect at the gate edge and demonstrated that a 10 nm Al_2O_3 passivation film can substantially suppress this charge injection, suggesting that an important mechanism of Al_2O_3 passivation is blocking electrons injected from the gate metal. As for other passivation materials, more experiments are undergoing to investigate this effect.

[1]M. A. Khan, M. S. Shur, Q. C. Chen, and J. N. Kuznia, Electron. Lett. **30**, 2175 (1994).
[2]S. C. Binari, P. B. Klein, and T. E. Kazior, Proc. IEEE **90**, 1048 (2002).
[3]S. C. Binari, K. Ikossi, J. A. Roussos, W. Kruppa, D. Park, H. B. Dietrich, D. D. Koleske, A. E. Wickenden, and R. L. Henry, IEEE Trans. Electron Devices **48**, 465 (2001).
[4]R. Vetury, N. Q. Zhang, S. Keller, and U. K. Mishra, IEEE Trans. Electron Devices **48**, 560 (2001).
[5]M. Tajima and T. Hashizume, Jpn. J. Appl. Phys. Part 1, **50**, 061001 (2011).
[6]B. M. Green, K. K. Chu, E. M. Chumbes, J. A. Smart, J. R. Shealy, and L. F. Eastman, IEEE Electron Device Lett. **21**, 268 (2000).
[7]J. S. Lee, A. Vescan, A. Wieszt, R. Dietrich, H. Leier, and Y. S. Kwon, Tech. Dig. - Int. Electron Devices Meet. **2000**, 381.
[8]T. Hashizume, S. Ootomo, T. Inagaki, and H. Hasegawa, J. Vac. Sci. Technol. B **21**, 1828 (2003).
[9]T. Hashizume, S. Ootomo, and H. Hasegawa, Appl. Phys. Lett. **83**, 2952 (2003).
[10]R. J. Simms, J. W. Pomeroy, M. J. Uren, T. Martin, and M. Kuball, Appl. Phys. Lett. **93**, 203510 (2008).
[11]G. Meneghesso, G. Verzellesi, F. Danesin, F. Rampazzo, A. Tazzoli, M. Meneghini, and E. Zanoni, IEEE Trans. Device Mater. Reliab. **8**, 332 (2008).
[12]K. V. Smith, S. Brierley, R. McAnulty, C. Tilas, D. Zarkh, M. Benedeck, P. Phalon, and A. Hooven, ECS Trans. **19**, 113 (2009).
[13]R. J. Trew, D. S. Green, and J. B. Shealy, IEEE Microw. Mag. **10**, 116 (2009).
[14]J. H. Leach and H. Morkoc, Proc. IEEE **98**, 1127 (2010).
[15]M. Faqir, G. Verzellesi, G. Meneghesso, E. Zanoni, and F. Fantini, IEEE Trans. Electron Devices **55**, 1592 (2008).
[16]Y. Ohno, T. Nakao, S. Kishimoto, K. Maezawa, and T. Mizutani, Appl. Phys. Lett. **84**, 2184 (2004).
[17]M. Bouya, D. Carisetti, N. Malbert, N. Labat, P. Perdu, J. C. Clement, M. Bonnet, and G. Pataut, Microelectron. Reliab. **47**, 1630 (2007).
[18]C. H. Lin, T. A. Merz, D. R. Doutt, M. J. Hetzer, J. W. Joh, J. A. del Alamo, U. K. Mishra, and L. J. Brillson, Appl. Phys. Lett. **95**, 033510 (2009).
[19]C. Y. Hu, T. Hazhizume, K. Ohi, and M. Tajima, paper presented at the 2010 International Workshop on Nitride Semiconductors, 19–24 September (2010), I3.5 Tampa, USA.
[20]C. Y. Hu, T. Hashizume, K. Ohi, and M. Tajima, Appl. Phys. Lett. **97**, 222103 (2011).
[21]W. Saito, M. Kuraguchi, Y. Takada, K. Tsuda, T. Domon, I. Omura, and M. Yamaguchi, Tech. Dig. - Int. Electron Devices Meet. **2005**, 586.
[22]W. Saito, T. Nitta, Y. Kakiuchi, Y. Saito, K. Tsuda, I. Omura, and M. Yamaguchi, IEEE Electron Device Lett. **29**, 8 (2008).
[23]K. v. Klitzing, G. Dorda, and M. Pepper, Phys. Rev. Lett. **45**, 494 (1980).
[24]S. Sabuktagin, S. Doğan, A. A. Baski, and H. Morkoç, Appl. Phys. Lett. **86**, 083506 (2005).
[25]R. Stoklas, D. Gregušová, J. Novák, A. Vescan, and P. Kordoš, Appl. Phys. Lett. **93**, 124103 (2008).
[26]C. Mizue, Y. Hori, M. Miczek, and T. Hashizume, Jpn. J. Appl. Phys. Part 1, **50**, 021001 (2011).
[27]P. B. Klein, S. C. Binari, K. Lkossi, A. E. Wickenden, D. D. Koleske, and R. L. Henry, Appl. Phys. Lett. **79**, 3527 (2001).
[28]C. Y. Hu, D. Kikuta, K. Nakatani, J.-P. Ao, M. Sugimoto, and Y. Ohno, IEEE Trans. Electron Devices **58**, 4265 (2011).
[29]J. Kotani, M. Tajima, S. Kasai, and T. Hashizume, Appl. Phys. Lett. **91**, 093501 (2007).
[30]W. S. Tan, M. J. Uren, P. A. Houston, R. T. Green, R. S. Balmer, and T. Martin, IEEE Electron Devices Lett. **27**, 1 (2006).
[31]M. Higashiwaki, Z. Chen, R. Chu, Y. Pei, S. Keller, U. K. Mishra, N. Hirose, T. Matsui, and T. Miura, Appl. Phys. Lett. **94**, 053513 (2009).
[32]E. A. Barry, K. W. Kim, and V. A. Kochelap, Appl. Phys. Lett. **80**, 2317 (2002).
[33]M. Tapajna, R. J. T. Simms, Y. Pei, and U. K. Mishra, and M. Kuball, IEEE Electron Device Lett. **31**, 662 (2010).
[34]M. Neuburger, J. Allgaier, T. Zimmermann, I. Daumiller, M. Kunze, R. Birkhahn, D. W. Gotthold, and E. Kohn, IEEE Electron Device Lett. **25**, 256 (2004).
[35]S. C. Binari, W. Kruppa, H. B. Dietrich, G. Kelner, A. E. Wickenden, and J. A. Freitas, Jr., Solid-State Electron. **41**, 1549 (1997).
[36]X. Z. Dang, C. D. Wang, E. T. Yu, K. S. Boutros, and J. M. Redwing, Appl. Phys. Lett. **72**, 2745 (1998).

[37]K. Sugawara, J. Kotani, and T. Hashizume, Appl. Phys. Lett. **94**, 152106 (2009).
[38]P. B. Klein, J. A. Freitas, Jr., S. C. Binari, and A. E. Wickenden, Appl. Phys. Lett. **75**, 4016 (1999).
[39]G. Meneghesso, A. Chini, E. Zanoni, M. Manfredi, M. Pavesi, B. Boudart, and C. Gaquiere, Tech. Dig. - Int. Electron Devices Meet. **2000**, 389.
[40]P. B. Klein, S. C. Binari, K. Ikossi-Anastasiou, A. E. Wickenden, D. D. Koleske, R. L. Henry, and D. S. Katzer, Electron. Lett. **40**, 661 (2001).
[41]Y. Nakano, Y. Irokawa, and M. Takeguchi, Appl. Phys. Express **1**, 091101 (2008).
[42]G. Meneghesso, F. Rossi, G. Salviati, M. J. Uren, E. Muñoz, and E. Zanoni, Appl. Phys. Lett. **96**, 263512 (2010).
[43]M. Meneghini, A. Stocco, N. Ronchi, R. Rossi, G. Salviati, G. Meneghesso, and E. Zanoni, Appl. Phys. Lett. **96**, 063508 (2010).
[44]C. H. Lin, D. R. Doutt, U. K. Mishra, T. A. Merz, and L. J. Brillson, Appl. Phys. Lett. **97**, 223502 (2010).
[45]C. Hodges, N. Killat, and M. Kuball, paper presented at the 9th International Conference on Nitride Semiconductors, Glasgow, 10–15 July (2011), J1.5.
[46]J. Neugebauer and C. G. Van de Walle, Phys. Rev. B **50**, 8067 (1994); J. Neugebauer and C. G. Van de Walle, Appl. Phys. Lett. **69**, 503 (1996).
[47]K. Saarinen, T. Laine, S. Kuisma, J. Nissila, P. Hautojarvi, L. Dobrzynski, J. M. Baranowski, K. Pakula, R. Stepniewski, M. Wojdak, A. Wysmolek, T. Suski, M. Leszczynski, I. Grzegory, and S. Porowski, Phys. Rev. Lett. **79**, 3030 (1997).
[48]M. A. Reshchikov and H. Morkoc, J. Appl. Phys. **97**, 061301 (2005).
[49]Y. S. Puzyrev, B. R. Tuttle, R. D. Schrimpf, D. M. Fleetwood, and S. T. Pantelides, Appl. Phys. Lett. **96**, 053505 (2010).
[50]G. Meneghesso, F. Zanon, M. J. Uren, and E. Zanoni, IEEE Electron Device Lett. **30**, 100 (2009).
[51]M. Meneghini, C. de Santi, T. Ueda, T. Tanaka, D. Ueda, G. Meneghesso, and E. Zanoni, paper presented at the 9th International Conference on Nitride Semiconductors, Glasgow, 10–15 July (2011), I2.3.
[52]A. Y. Polyakov, N. B. Smirnov, A. V. Govorkov, and E. A. Kozhukhova, paper presented at the 9th International Conference on Nitride Semiconductors, Glasgow, 10–15 July (2011), B3.7.
[53]S. Saadaoui, M. M. B. Salem, M. Gassoumi, H. Maaref, and C. Gaquiere, J. Appl. Phys. **110**, 013701 (2011).
[54]A. G. Chynoweth, Phys. Rev. **109**, 1537 (1958).
[55]C. M. Hu, Tech. Dig. - Int. Electron Devices Meet. **1983**, 176.
[56]K. Kunihiro, K. Kasahara, Y. Takahashi, and Y. Ohno, IEEE Electron Device Lett. **20**, 608 (1999).
[57]G. Koley, V. Tilak, L. F. Eastman, and M. G. Spencer, IEEE Trans. Electron Devices **50**, 886 (2003).
[58]T. Mizutani, Y. Ohno, M. Akita, S. Kishimoto, and K. Maezawa, IEEE Trans. Electron Devices **50**, 2015 (2003).