Fabrication of double-dot single-electron transistor in silicon nanowire

Mingyu Jo[a], Takuya Kaizawa[a], Masashi Arita[a], Akira Fujiwara[b], Yukinori Ono[b], Hiroshi Inokawa[c] Jung-Bum Choi[d] and Yasuo Takahashi[a*]

[a]Graduate School of Information Science and Technology, Hokkaido Univ., Sapporo, 060-0814, Japan

[b]NTT Basic Research Laboratories, NTT Corporation, 3-1 Morinosato Wakamiya, Atsugi, 243-0198, Japan

[c]Research Institute of Electronics, Shizuoka Univ., 3-5-1, Johoku, Hamamatsu, 432-8011, Japan

[d]Physics and Research Institute of NanoScience and Technology, Chungbuk National Univ., Cheongju, Chungbuk 361-763, Korea

Abstract We propose a simple method for fabricating Si single-electron transistors (SET) with coupled dots by means of a pattern-dependent-oxidation (PADOX) method. The PADOX method is known to convert a small one-dimensional Si wire formed on a silicon-on-insulator (SOI) substrate into a SET automatically. We fabricated a double-dot Si SET when we oxidized specially designed Si nanowires formed on SOI substrates. We analyzed the measured electrical characteristics by fitting the measurement and simulation results and confirmed the double-dot formation and the position of the two dots in the Si wire.

Keywords Quantum dots, Coulomb blockade; single-electron tunneling, double-dot SETs.

*Corresponding author. Tel.: + 81117066794; fax: + 81117066457.
E-mail address: y-taka@nano.ist.hokudai.ac.jp (Yasuo Takahashi)

1. Introduction

Double-dot single-electron transistors (double-dot SETs) have attracted much attention in single-electron transfers [1-4] and quantum computing [5-7] because they provide a highly tunable quantum-dot system in which artificial two-levels can be adjusted by gate and drain voltages. In the initial stage of this research, these kinds of devices have mainly been fabricated in the two-dimensional (2D) electron-gas system by using tunable gate to control electrical potential barriers [5, 8-11]. If the devices can be fabricated on the Si wafer, extremely low power operation in combination with conventional CMOS LSIs will be possible. Recently the silicon-based devices, which were fabricated on a silicon-on-insulator (SOI) wafer by electron beam lithography, have been studied [3, 7, 12]. However, fabricating small silicon-based double-dot structures is not easy because of the limits on the minimum feature size of the lithography. In this study, we developed a simple fabrication method for double-dot SETs on a SOI wafer by using a pattern-dependent-oxidation (PADOX) method [13]-[16], which is a CMOS compatible process and can possibly make small dots smaller than the lithographic limit.

The PADOX method uses special phenomena that occur during oxidation of one-dimensional Si nanowires on a silicon-on-insulator (SOI) wafer and achieves 10-nm Si islands. The great advantage of this method is that tunnel barriers are automatically formed between the island and source/drain electrodes in a self-aligned manner. The process of PADOX is very simple: Si nanowires connected to wide Si layers are thermally oxidized. The thermal oxidation of Si is known as one of the most stable processes in LSI technology. Although the process is simple, the principle of PADOX is complicated. The basic principle of the formation is the band-gap modulation of the Si wire due to both the quantum size effect and the strain caused by the oxidation [16]. However, conventional PADOX only produces a single dot in the middle of the one-dimensional Si wire. Here, we describe and demonstrate the Si double-dot formation by using specially designed Si nanowires and the PADOX method.

2. Device fabrication

We fabricated SETs on an SOI substrate using conventional Si-CMOS processes. We made a specially designed Si nanowire— which had small constrictions at the end of the drain side of the wire, as shown in the scanning electron microscope (SEM) image in Fig. 1— on the SOI substrate by electron-beam lithography and dry etching. The initial wire width was 44 nm, the length was 100 nm, and the height, which corresponded to the thickness of the SOI layer, was 25 nm. Then we used the PADOX method at 1000°C

in the dry oxygen ambient. After depositing a 50-nm-thick SiO_2 interlayer, we attached a phosphorus-doped polycrystalline Si gate electrode over the pattern shown in Fig. 1. Here, we also used the Si substrate of the SOI as a backgate.

3. Results and discussion

Electrical characteristics were measured at 8 K in a low-temperature probe station by using an Agilent 4156C precision semiconductor parameter analyzer. The measured I_d versus top-gate voltage V_g characteristics at a drain voltage V_d of 5 mV and a contour plot of differential conductance as a function of drain voltage V_d and gate voltage V_g are shown in Figs. 2(a) and (b), respectively. Clear current oscillations and Coulomb diamonds are observed. We can also observe long-period beats in current oscillations as well as in Coulomb diamonds. The period of current oscillations and Coulomb diamonds depends on the capacitance between the gate and dot in a single-electron device. Therefore, the observed characteristics (short period oscillations with long-period beats) suggest the double-dot formation, in which dots 1 and 2 are connected in a series. The short period oscillations are caused by the dot with larger gate capacitance, and long period beats are caused by the dot with smaller gate capacitance.

To confirm that the device has double-dot, we simulated the characteristics by using the Monte Carlo method [17]. Figure 3 shows the equivalent circuit of the double-dot SET used for the analysis. Here, tunnel resistances, R_s, R_m and R_d were fixed at 2 MΩ because these vales only determine the current level and are less important for analyzing oscillation periods. The capacitance parameters obtained from the fitting between simulated and measured data as follows: C_{g1} = 0.8 aF, C_{g2} = 0.1 aF, C_s = 7 aF, C_m = 5 aF, and C_d=15 aF. Here we ignore backgate capacitances because they are too small to affect the characteristics in the simulation. As shown in Figs. 4(a) and (b), simulated current oscillations and Coulomb diamonds with beats resemble the measured results, although in the measured data current increases and diamond width decreases as V_g increases. These phenomena are attributed to the tunnel resistance decrease and tunnel capacitance increase due to the gate voltage suppressing the potential barrier. In the SET device made by the PADOX method, since the tunnel barriers are formed in the Si layer by the stress and quantum size effect, the voltage applied to the gates modulates the tunnel barrier height.

We also measured the I_d-V_g oscillation characteristics at various backgate voltages V_{bg}. Figure 5(a) shows the results in which the short-period oscillation shift in the lower gate voltage direction as V_{bg} increases. The peak V_g of the short period oscillation A is plotted as a function of V_{bg} in Fig. 5(b). The slope of the graph corresponds to the capacitance ratio between frontgate and backgate [18], which means that C_{bg1}/C_{g1} =

0.11. As shown in Fig. 5(a), long-period beats also shift in the lower gate voltage direction as V_{bg} increases. The valleys V_g of the envelope of the long period oscillation (beat) B are also plotted as a function of V_{bg} in Fig. 5(c). The results show that C_{bg2}/C_{g2} = 0.10. The fact that C_{bg1}/C_{g1} and C_{bg2}/C_{g2} are almost the same indicates that the two dots exist in the same plane in parallel with both the Si substrate and the top gate electrode.

The formation of the double-dot could be estimated on the basis of these results. Since the gate capacitance C_{g1} of 0.8 aF is similar to those of SETs fabricated by the conventional PADOX method, dot 1 is the dot formed in the center of the wire by the PADOX mechanism. Although dot 2 has a small gate capacitance C_{g2} of 0.1 aF, which is 1/8 of C_{g1}, the total capacitance of dot 2 is about 20 aF, which is almost twice as large as that of dot 1, 12.8 aF. This fact indicates that the electric flux lines from dot 2 mainly go to the drain area not to the gate, which means that dot 2 is strongly coupled with the drain area. Since the two dots should be in the same plane parallel to the gate and substrate as mentioned above, the arraignment of dots 1 and 2 in the wire can be drawn schematically, as shown in Fig. 6(b). Although the total capacitance of dot 1 is smaller than that of dot 2, dot 1 is strongly coupled with frontgate and backgate. Meanwhile, the electric flux lines originating from dot 2 go to the drain because dot 2 shares a large junction area with the drain as shown in Fig. 6(b). Thus it is considered that the gate capacitance of dot 2 shrinks despite dot 2 being relatively large.

The formation mechanism of the double dots is explained as follows. As mentioned above, dot 1 is formed by the conventional PADOX method, in which the combination of the strong-stress induced band-gap shrinkage and potential increase caused by the quantum size effect forms a single-electron island (dot) together with a tunnel barrier at both sides of the island. This is illustrated in the potential diagram along the Si wire shown in Fig. 6(a) [15]. When the 2D Si layer pattern formed on the SOI substrate is oxidized, the oxidation from the Si/buried oxide interface plays an important role. Although the amount of oxygen diffusing from the pattern edge is largest at the area closer to the pattern edge, stress accumulated during the oxidation suppresses the oxidation there. As a result, the oxidation from the back precedes more at the area a little further from the pattern edge. When we made small constrictions at the end of the Si wire as shown in Fig. 1, this enhanced the stress accumulation at the edge and provided more oxygen for the area a little further from the edge [12, 14]. This thins the 2D Si layer in this area, as shown in Fig. 6(c), which is a cross sectional view of the device. This thin Si region acts as a tunnel barrier, as shown in Fig. 6(a). Dot 1 is located between the two potential barriers formed at the end of the wire by the PADOX, and dot 2 is located at the drain side surrounded by the drain.

Figure 7 shows measured I_d-V_g oscillation characteristics at various temperatures. The long-period beats were observed as well as short-period oscillations up to about 16K, but only short-period oscillations were observed at 32K. This reveals that the beats disappear at lower temperatures than the short-period oscillations because the charging energy of dot 2 is smaller than that of dot 1. These results confirm the accuracy of the capacitance parameters calculated by the simulation.

Figure 8 shows the I_d-V_g characteristics measured for another device fabricated using almost the same design rules. Similar current oscillations with beats are also observed. In this device, the evaluated gate capacitance of dot 1 is 2.8 aF, and that of the dot 2 is 0.56 aF. These results also confirm that the method proposed here is applicable to forming the double-dot SETs. As shown in the two results, the asymmetry of the gate capacitances of the two dots sometimes inconveniences the application in the single-electron transfers or quantum computing. Further investigation to improve the initial pattern is needed to achieve more sophisticated and freer island design.

4. Conclusion

We demonstrated the fabrication method of the double-dot structure by using a specially designed Si nanowire that had small constrictions and by using the PADOX method. We analyzed the oscillation characteristics and revealed the position of the two dots and estimated the mechanism of the formation. The method demonstrated here is efficient because coupled dots are automatically formed in accordance with the initial pattern on the SOI wafer. The mechanism may enable us to make a triple-dot system. We believe that we can also fabricate a double-dot that has equivalent gate capacitances though further experimental and theoretical studies are needed to design the initial pattern.

Acknowledgments

This work was partly supported by a Grant-in-Aid from the Japan Society for the Promotion of Science (KAKENHI (18560640), (20035001), (20241036), (20222755)), and MOST through the Frontier 21 National Program for Tera-level Nano-Devices (TND) of Korea.

[1] L. J. Geerligs, V. J. Anderegg, P. A. M. Holweg, J. E. Mooji, H. Pothier, D. Esteve, C. Urbina, and M. H. Devoret, Phys. Rev. Lett. 64 (1990) 2691.

[2] H. Pothier, P. Lafarge, R. F. Orfila, C. Urbina, D. Esteve, and M. H. Devoret, Phys. B 169 (1991) 573.

[3] A. Fujiwara, Y. Takahashi, K. Yamazaki, H. Namatsu, M. Nagase, K. Kurihara, and K. Murase, IEEE Transactions on Electron Devices 46 (1999) 954.

[4] Y. Ono, A. Fujiwara, K. Nishiguchi, H, Inokawa, and Y. Takahashi, J. Appl. Phys. 97 (2005) 031101.

[5] W. G. van der Wiel, S. De Franceschi, J. M. Elzerman, T. Fujisawa, S. Tarucha, and L. P. Kouwenhoven, Rev. Mod. Phys. 75 (2003) 1.

[6] T. Hayashi, T. Fujisawa, H. D. Cheong, Y. H. Jeong, and Y. Hirayama, Phys. Rev. Lett. 91 (2003) 226804.

[7] J. Gorman, D. G. Hasko, and D. A. Williams, Phys. Rev. Lett. 95 (2005) 090502

[8] U. Meirav, M. A. Kastner, and S. J. Wind, Phys. Rev. Lett. 65 (1990) 771.

[9] F. R. Waugh, M. J. Berry, D. J. Mar, and R. M. Westervelt, K. L. Campman, and A. C.Gossard, Phys. Rev. Lett. 75 (1995) 705.

[10] C. Livemore, C. H. Crouch, R. M. Westervelt, K. L. Campman, and A. C. Gossard, Science 274 (1996) 1332.

[11] M. A. Kastner, Rev. Mod. Phys. 64 (1992) 849.

[12] G. Yamahata, Y. Tsuchiya, S. Oda, Z. A. K. Durrani, and H. Mizuta, Jpn. J. Appl. Phys. 47 (2008) 4820.

[13] Y. Takahashi, M. Nagase, H. Namatsu, K. Kurihara, K. Iwadate, Y. Nakajima, S. Horiguchi, K. Murase, and M. Tabe, Electronics Letters 31 (1995) 136.

[14] Y. Takahashi, H. Namatsu, K. Kurihara, K. Iwadate, M. Nagase, and K. Murase, IEEE Trans. Electron Devices 43 (1996) 1213.

[15] Y. Ono, Y. Takahashi, K. Yamazaki, M. Nagase, H. Namatsu, K. Kurihara, and K.Murase, IEEE Trans Electron Devices ED-47 (2000) 147.

[16] S. Horiguchi, M. Nagase, K. Shiraishi, H. Kageshima, Y. Takahashi, and K. Murase, Jpn. J. Appl. Phys. 40 (2001) L29.

[17] N. Kuwamura, K. Taniguchi and C. Hamaguchi, Electron. Communi. Jpn. Part 2, 77 (1994) 65.

[18] M. Jo, T. Kaizawa, M. Arita, A. Fujiwara, K. Yamazaki, Y. Ono, H. Inokawa, Y. Takahashi, and J.-B. Choi, Materials Science in Semiconductor Processing (to be published). [doi:10.1016/j.mssp.2008.12.001]

Figure captions

Fig. 1. SEM image of the fabricated Si nanowire.

Fig. 2. I_d-V_g characteristics (a) and Coulomb diamond diagram (b) measured at backgate voltage V_{bg} of 20 V at 8 K.

Fig. 3. An equivalent circuit of the device.

Fig. 4. Calculated I_d-V_g characteristics (a) and Coulomb diamond diagram (b).

Fig. 5. The I_d-V_g characteristics at various backgate voltage V_{bg} (a), and peak shift of peak A (b) and valley shift of peak B (c) as functions of V_{bg}.

Fig. 6. I_d-V_g oscillation characteristics at V_{bg} = 0 V measured at various temperatures.

Fig. 7. (a) schematic potential diagram along the Si wire, (b) schematic view of the device in which the formation of dots 1 and 2 is estimated, and (c) schematic cross sectional view of the device along the wire.

Fig. 8. I_d-V_g oscillation characteristics of another device measured at 8 K and V_{bg} = 0 V

Figures

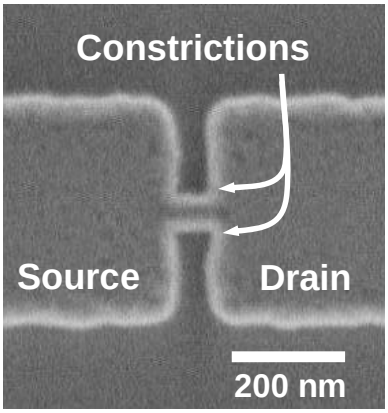
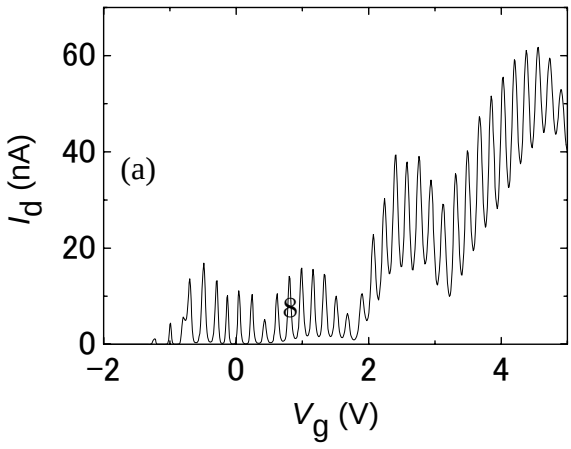


Fig. 1 Mingyu Jo et al.



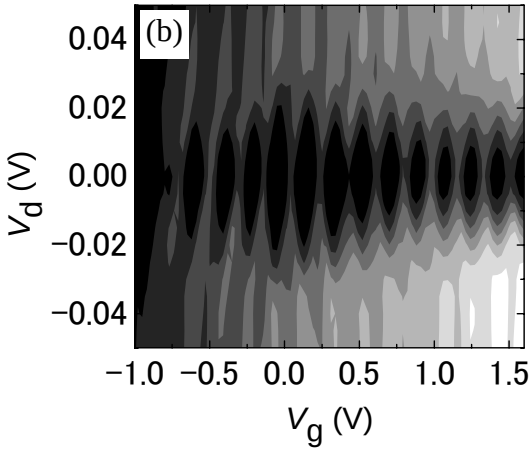


Fig. 2 Mingyu Jo et al.

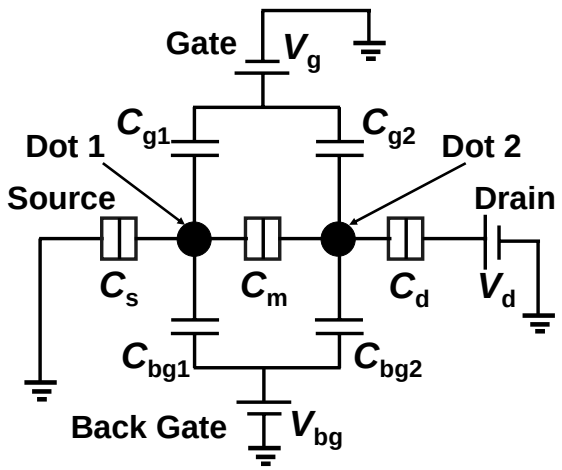


Fig. 3 Mingyu Jo et al.

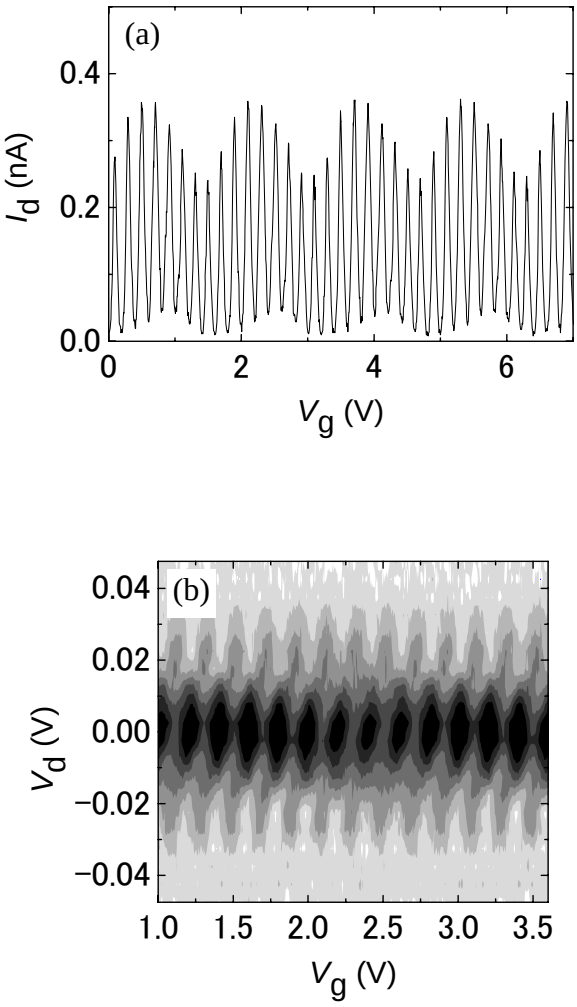


Fig. 4 Mingyu Jo et al.

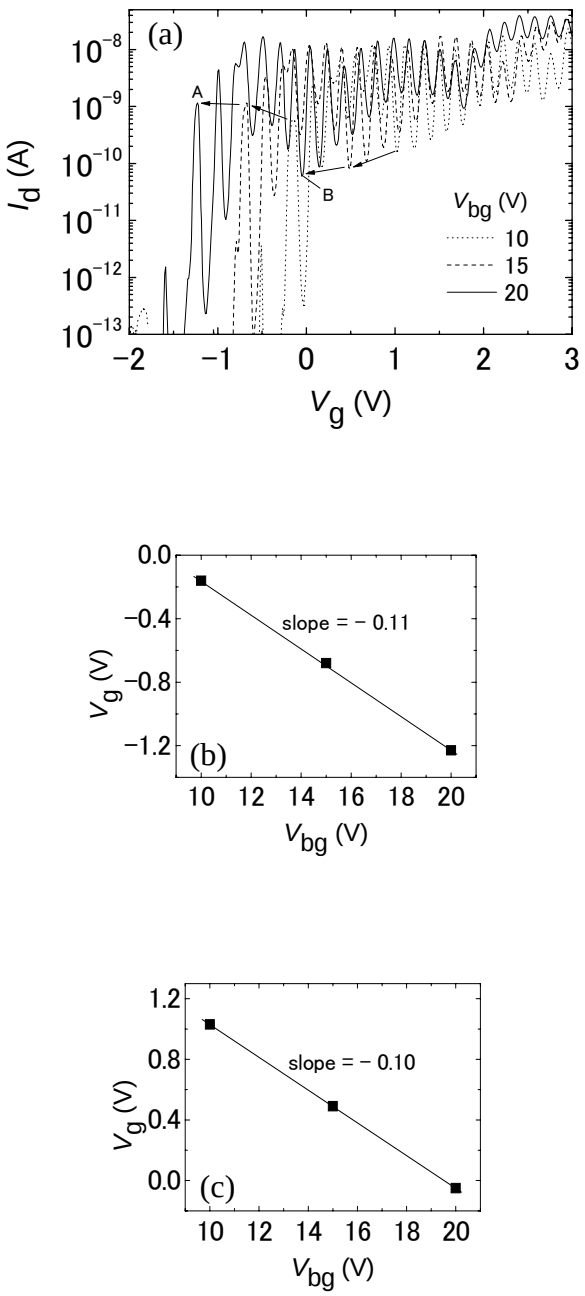


Fig. 5 Mingyu Jo et al.

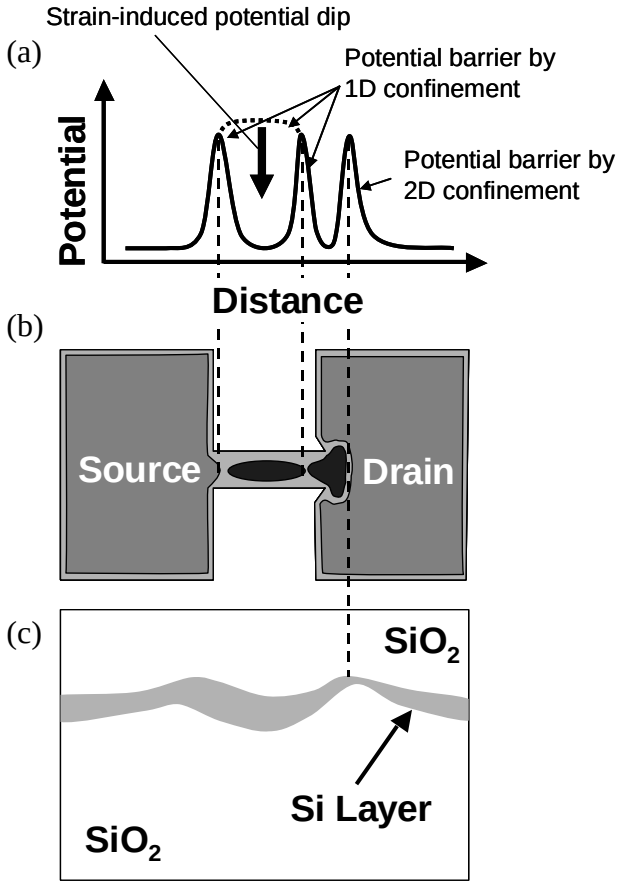


Fig. 6 Mingyu Jo et al.

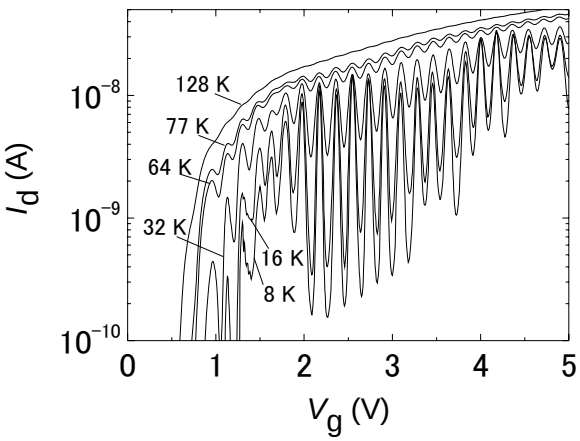


Fig. 7 Mingyu Jo et al.

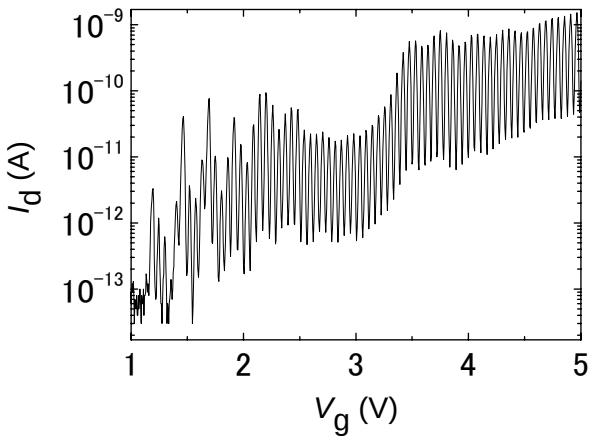


Fig. 8 Mingyu Jo et al.