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Si-based ultrasmall multiswitching single-electron transistor operating at room-temperature

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An ultrasmall single-electron transistor has been made by scaling the size of a fin field-effect transistor structure down to an ultimate limiting form, resulting in the reliable formation of a sub-5 nm Coulomb island. The charge stability data feature the first exhibition of three and a half clear Coulomb diamonds at 300 K, each showing a high peak-to-valley current ratio. Its charging energy is estimated to be more than one order magnitude larger than the thermal energy at room-temperature. The hybrid literal gate integrated by this single-electron transistor combined with a field-effect transistor displays >5 bit multiswitching behavior at 300 K with a large voltage swing of ~1 V. © *2010 American Institute of Physics*. [doi:10.1063/1.3483618]

Single-electron transistor (SET), the ultimate limit of switching devices, has been intensively studied because of its unique multifunctionality with ultralow power and scalability down to subnanometer regime.[1] However, the reliability of room-temperature (RT) operation and requirement of complementary metal-oxide-semiconductor-compatible processes have been the main bottlenecks for implementing further practical device applications. Significant earlier work has been aimed at implementing a RT-operating SET, using various schemes, device structures, and fabrication processes,[2–7] but reliable processes for the controlled fabrication of ultrasmall size Coulomb islands of less than 5 nm have not been firmly established yet, limiting practical device applications at RT.

We have modified a state-of-the-art fin field-effect transistor (finFET) structure[8] to scale the device to an ultimate form, by using deep-trench and pattern-dependent oxidation, which can be used to form an SET with a Coulomb island size of less than 5 nm. By wrapping a fin-gate almost completely around this island, good control of the local electron potential is maintained. Figure 1(a) shows a schematic three-dimensional (3D) layout of the device. A cross-sectional schematic view along the channel (cutline a-b) is seen in Fig. 1(b). Devices were fabricated using a 50-nm-thick undoped silicon-on-insulator substrate. First, a 20-nm-wide nanowire, connecting the source and drain (S/D) electrodes, was formed using electron-beam lithography (EBL) with polymethyl-methacrylate resist and subsequent reactive ion etching (RIE) using $SF_6/CF_4/O_2$. After deposition of a 100-nm-thick tetraethyl-orthosilicate (TEOS) layer, an 80-nm-wide trench was etched across the nanowire using EBL with ZEP520A resist and subsequent RIE etching using CHF_3/O_2. The exposed silicon area under the trench was etched by a further 30 nm in depth by dry etching using $SF_6/CF_4/O_2$, and followed by gate oxidation at 900 °C for 50 min (SET_A) and 40 min (SET_B). See Figs. 1(c) and 1(d) for transmission electron microscope (TEM) images of the cross-sectional view of the etched wires (along the cutline c-d) after oxidation, showing the island size reduced to ~2 nm (SET_A) and 4 nm (SET_B), respectively. Good control over the island size was achieved through this oxidation process. Next, a 20 nm thick TEOS layer was deposited

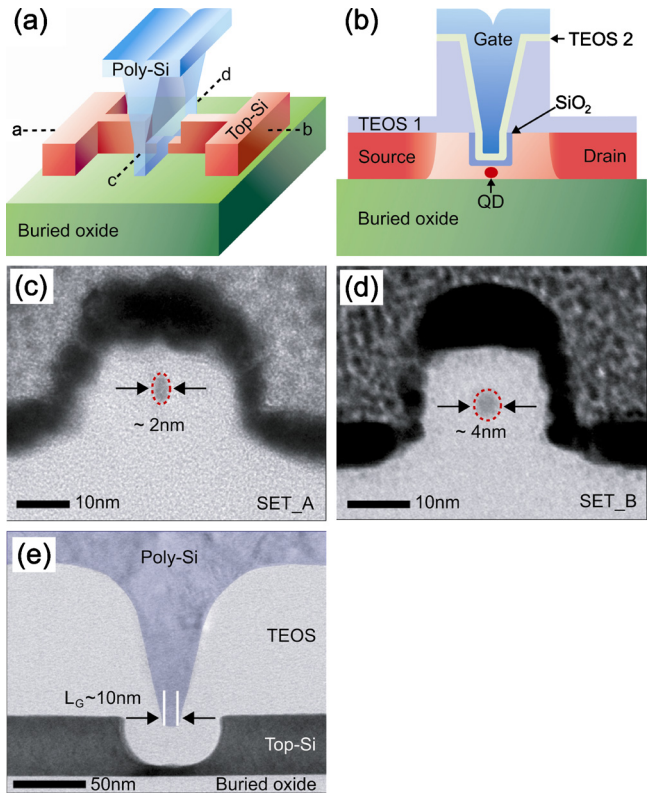

FIG. 1. (Color online) (a) Schematic 3D layout of the SET device. (b) Cross-sectional view along the channel (the cutline a-b). [(c) and (d)] Cross-sectional TEM image of the etched Si wires (along the cutline c-d) after oxidation at 900 °C for 50 and 40 min, showing Coulomb island sizes of ~2 nm for SET_A and ~4 nm for SET_B. (e) Cross-sectional TEM images along the cutline a-b after deposition of the poly-Si fin-gate.

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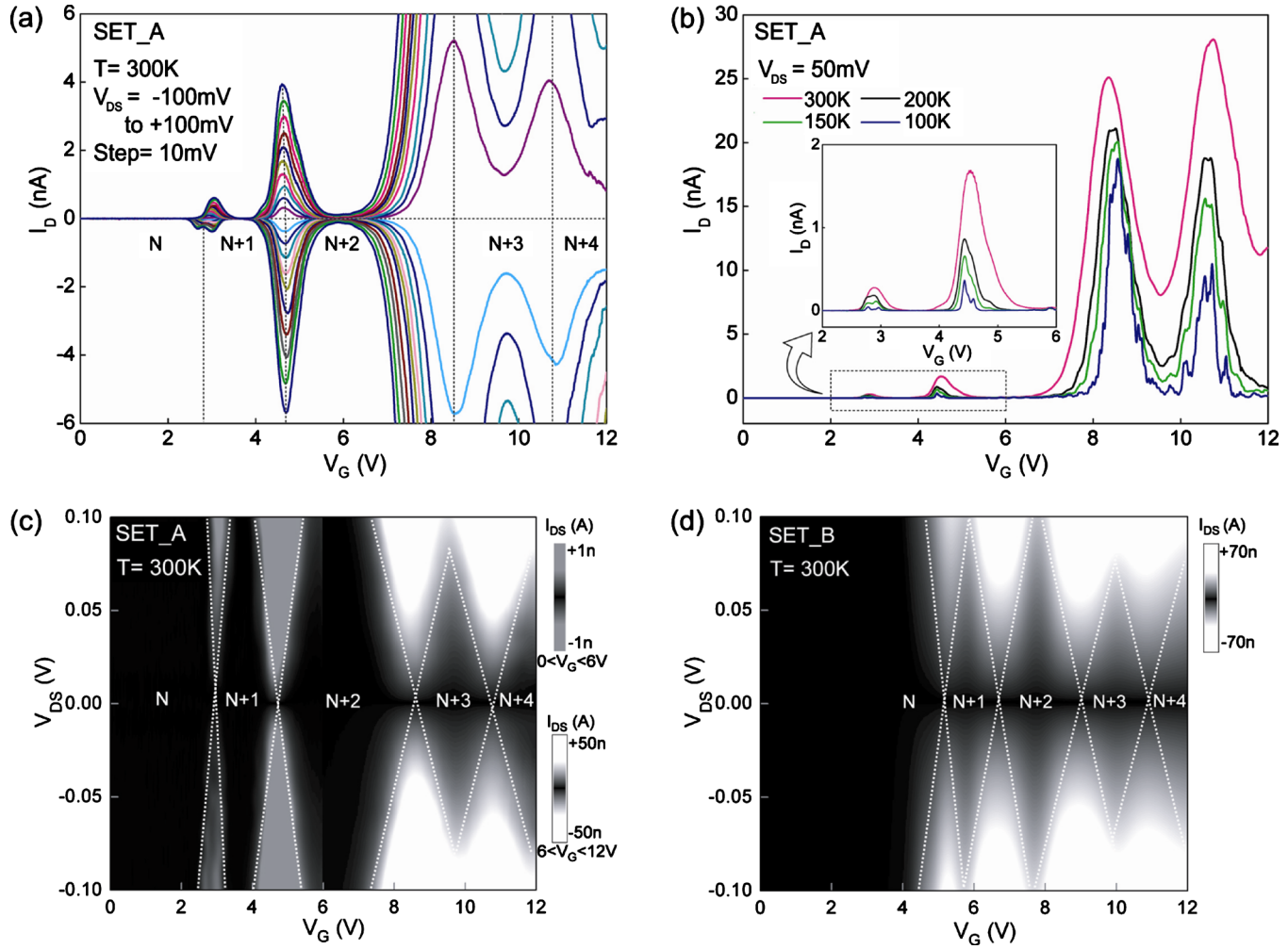

FIG. 2. (Color online) (a) Drain current of SET_A measured at 300 K as a function of fin-gate voltage V_G using drain voltages from −100 to 100 mV with a step of 10 mV. (b) Temperature dependence of SET_A at a fixed drain voltage of V_{DS}=50 mV. The inset shows detail from the first two Coulomb peaks in the current regime marked with dotted line. [(c) and (d)] Charge stability plot at room temperature for SET_A and SET_B; each diamond corresponds to a stable charge configuration state with fixed electron occupancy N.

into the trench to form spacers on the sidewalls of the source and drain (S/D) electrodes.[9] Doped poly-silicon was then deposited into the trench to form a self-aligned fin-gate very close to the Coulomb island. The fabrication was completed with conventional S/D ion implants, annealing, and contact processes. Figure 1(e) shows a TEM image of the top-Si nanowire active channel, the polycrystalline silicon (poly-Si) fin-gate and the TEOS spacer profiles along the cutline (a)-(b). The fin-gate above the center of the etched region of the active channel is about 10 nm wide and wraps most of the way around the active channel. This gate is important for realizing a large peak-to-valley current ratio (PVCR) in the Coulomb oscillations at RT. Note how the top-Si nanowire, exposed by the nanogap between the source and the drain, is further etched down to <5 nm in thickness, by dry etching and gate oxidation. This key process step, different from the conventional finFET process, enables an ultrasmall size Coulomb island to be formed with nearly identical tunnel barriers in a self-aligned manner.

Figure 2(a) shows typical Coulomb oscillations from the SET_A measured at room temperature; these characteristics show high and nearly symmetric PVCRs, indicating that the tunnel barriers at both sides of a Coulomb island are practically identical. The temperature dependence of these characteristics is shown in Fig. 2(b); as the temperature is reduced, the Coulomb peak positions barely change, but the PVCRs increase. Room temperature charge stability plots are shown in Figs. 2(c) and 2(d) for SET_A and SET_B, where three and a half Coulomb diamonds are clearly seen; each diamond corresponds to a stable charge configuration on the Coulomb island with the number of occupied electrons N. As seen in Fig. 2(a), the lack of any feature for $V_G \leq 3$ V may indicate that the Coulomb island of SET_A is unpopulated by electrons in this region. This view could be supported by the Coulomb diamond data, where as the gate voltage is made less positive, the slope of each Coulomb diamond steeply increases, and the Coulomb diamond (for $V_G < 3$ V) does not close. This could allow the dot occupancy N=1 for the first diamond. However, a charge sensing experiment by means of a separated circuit (such as a quantum point contact) can, without doubt, show the dot occupancy level.[10]

It is noted that substantial change in slopes and diagonal sizes of each successive diamond implies that the charging energy is not constant over the gate voltage range studied, and the orthodox Coulomb blockade theory may break down in this case. This behavior may be caused by strong interplay of the Coulomb interaction and additional quantum effects associated with very low electron number on the island. Nevertheless, we can roughly estimate the size of the island and calculate the Coulomb charging energy because the first dia-

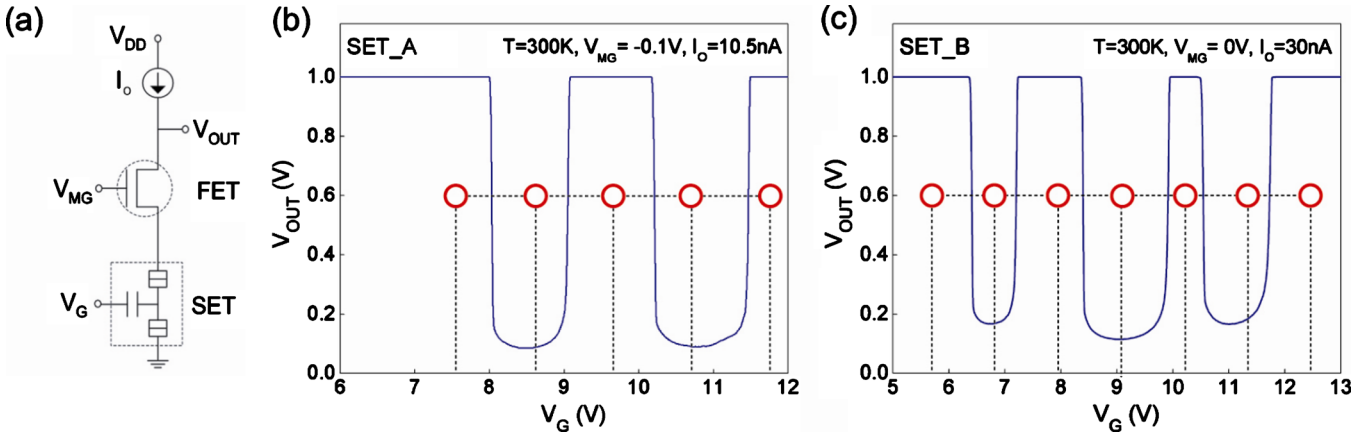

FIG. 3. (Color online) (a) Circuit layout of the SET/FET literal gate that comprises of a SET, a MOSFET, and a constant-current load. [(b) and (c)] The input-output voltage transfer of the resultant SET/FET literal gate measured at 300 K, displaying more than 5 bits multiple switching with a sharp swing as high as ~1 V. The constant-current I_0 is 10.5 nA (30 nA) and the V_{MG} for the MOSFET is set to −0.1 V (0 V) for SET_A (SET_B).

mond associated with the lowest dot occupancy N=1 is determined mainly by the Coulomb charging energy.[1] Values for the gate and junction capacitances can be directly obtained from the Coulomb peak spacing ΔV_G and the slopes of the first diamond. We find that, for SET_A, $C_G \sim 0.094$ aF, $C_S \sim 0.16$ aF, and $C_D \sim 0.17$ aF, yielding the total capacitance $C_\Sigma \sim 0.42$ aF, which corresponds to a ~1.94 nm diameter spherical dot, in good agreement with the TEM image of SET_A in Fig. 1(c). Similarly, the total capacitance of SET_B is estimated to be $C_\Sigma \sim 1.04$ aF, which corresponds to a ~4.6 nm diameter dot. The charging energy of the SET_A (SET_B) is thus $e^2/C_\Sigma \sim 0.377$ eV (~0.154 eV) which is more than one order magnitude larger than the thermal energy at room temperature, yielding the clear Coulomb oscillations with high PVCRs even at RT.

The quantum effect is expected to be enhanced in such a small dot of <5 nm, which must be stronger in the SET_A whose size is much smaller than the SET_B. If we assume the dot occupancy N=2 for the second diamond, the unusual large shift in the third Coulomb peak of the SET_A could be related to the electron filling in a spin-up-spin-down sequence, i.e., spin-filling of the next orbital state for the third electron number following Pauli's exclusion rule. (Similarly, the third Coulomb peak of the SET_B is observed to have an additional gate voltage shift of ~0.6 V, which is ~40% larger than the other two V_G spacings.) The level spacing due to the quantum confinement can be roughly estimated based on the effective mass approach. For a 2 nm silicon dot modeled by a 3D hard-wall potential, the level spacing is estimated to be ~0.493 eV, which is comparable to the Coulomb energy $e^2/C_\Sigma \sim 0.377$ eV. More exact explanation considering quantum effects may need extensive ultralow temperature measurements, which will be carried out and reported elsewhere.

For practical circuit applications, we integrated the SET with a FET and measured the multiple-valued literal gate functionality at RT. A schematic layout of the SET/FET hybrid circuit is seen in Fig. 3(a), showing that it comprises of a SET, a MOSFET, and a constant-current load. The FET connected in series with the SET was to attain the SET bias voltage under a range of Coulomb blockade. Our circuit, called universal literal gate,[11] operates under a constant current mode with a drain voltage limit. The voltage transfer characteristics of the resultant SET/FET literal gate measured at 300 K are seen in Figs. 3(b) and 3(c), displaying five (seven) periodic voltage outputs of high/low level multiple switching with a sharp swing as high as ~1 V for SET_A (SET_B). This enables multibit (>5 bit) functionality at RT and can provide a basic block for the practical implementation of the SET-based multi-valued memory and logic architectures with ultralow power consumption.

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