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Measurement of interface-state-density distribution near conduction band at interface between atomic-layer-deposited Al_2O_3 and silicon-doped InAlN

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The Al_2O_3/InAlN interface formed by atomic layer deposition on a sufficiently thick silicon-doped InAlN layer lattice matched to GaN was investigated electrically. A metal-oxide-semiconductor (MOS) diode fabricated through careful interface formation showed a minimized leakage current and a capacitance-voltage (C-V) characteristic with a capacitance change large enough to evaluate the interface-state density, in the range of $10^{12}\,eV^{-1}cm^{-2}$, near the conduction band. However, the MOS diode with careless interface formation resulted in degraded electrical characteristics, which indicated the process dependence of the interface properties. The effects of the acceptor-like interface states on the C-V curves are discussed. © *2013 AIP Publishing LLC*. [http://dx.doi.org/10.1063/1.4810960]

A lattice-matched InAlN/GaN heterostructure with a large spontaneous polarization difference and a high electron barrier can provide a two-dimensional electron gas (2DEG) with a high density exceeding $2 \times 10^{13}\,cm^{-2}$.[1,2] To exploit the excellent properties of the InAlN/GaN heterostructure in a high-electron-mobility transistor (HEMT), leakage current through the InAlN barrier should be suppressed. For this purpose, the use of an insulator in forming a metal-oxide-semiconductor (MOS) gate structure has been proposed.[3] Recently, a MOSHEMT with a minimal gate-leakage current achieved a cut-off frequency of up to 400 GHz.[4] Further improvement of the insulator/InAlN interface may improve device performance. However, the properties and the most suitable formation process of the interface between InAlN and various candidate insulators are not yet fully clarified. In particular, they have not been clarified for the Al_2O_3 layer formed by atomic layer deposition (ALD), although it is one of the most attractive insulators. For the Al_2O_3/InAlN interface in a MOSHEMT structure with 2DEG, an extensive investigation has been performed to evaluate the interface-state density (D_{it}) distribution on the lower side of the band gap near the valence band.[5] Here, an attempt was made to characterize the properties of the Al_2O_3/InAlN interface separately from those of the InAlN/GaN heterointerface using a sufficiently thick doped InAlN layer lattice-matched to GaN. As an initial work, we would like to report the experimental results on the D_{it} distribution near the conduction band at the Al_2O_3/InAlN interface formed by ALD.

The structure of the investigated MOS diode sample is illustrated in Fig. 1. To characterize the insulator-semiconductor interface separately from the InAlN/GaN heterointerface, a sufficiently thick doped $In_{0.17}Al_{0.83}N$ layer compared with the depletion layer width was prepared. A 160-nm-thick Si-doped epitaxial InAlN layer and an underlying 2-μm-thick Si-doped GaN buffer layer were grown on a sapphire substrate by metal-organic vapor-phase epitaxy (MOVPE). After the crystal growth, the InAlN surface was treated with hydrofluoric acid (HF) to remove the surface native oxide layer formed by air exposure. Then, a 20-nm-thick SiN_x layer for cap annealing was deposited by electron-cyclotron-resonance chemical vapor deposition (ECRCVD) at 320 °C using a SiH_4/Ar and N_2 gas mixture. Subsequently, an annular Ti/Al/Ti/Au (20 nm/50 nm/20 nm/100 nm) ohmic electrode was formed via the insulator window opened by photolithography and buffered HF (BHF) etching. Annealing to alloy the ohmic electrode was then performed at 850 °C for 1 min in nitrogen atmosphere with a SiN_x cap layer. After removing the SiN_x cap layer by BHF etching, the Al_2O_3 layer was deposited by ALD at 350 °C using H_2O and trimethylaluminum (TMA). Finally, a circular Ni/Au (20 nm/50 nm) electrode was formed on the Al_2O_3 layer at the center of the annular ohmic electrode, to complete the sample hereafter referred to as the cap-annealed MOS diode. For comparison, another MOS diode and a Schottky barrier diode were fabricated on separate chips cut from the same epitaxial wafer. The compared MOS diode, referred to as the capless-annealed MOS diode hereafter, was fabricated by a similar process without the SiN_x surface protection during annealing for ohmic contact alloying, whereas the Schottky barrier diode was fabricated by the cap-annealing process excluding the deposition of Al_2O_3.

To clarify the applicability of the Al_2O_3 layer as a gate insulator, the current-voltage (I-V) characteristics for the MOS diodes were measured and compared with those of the

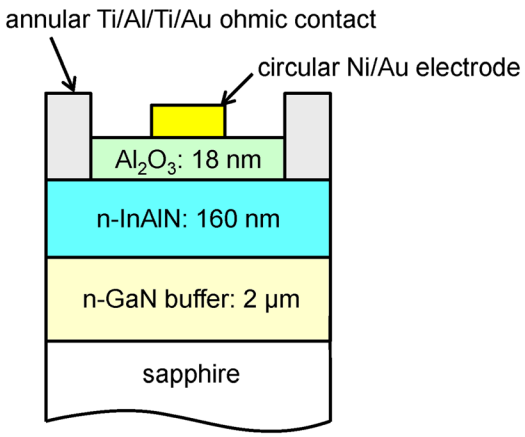

FIG. 1. Structure of fabricated MOS diode.

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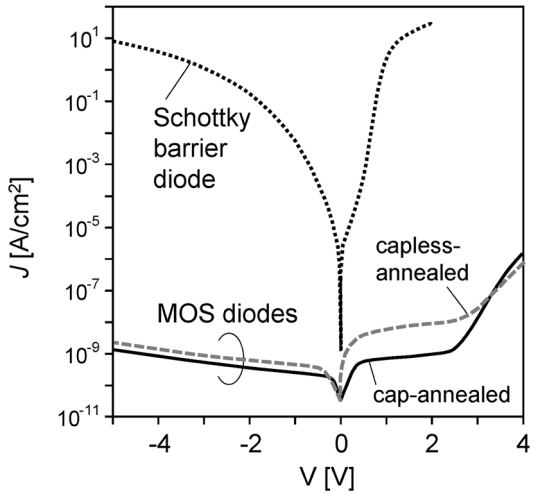

FIG. 2. Measured I-V characteristics. The solid and broken lines are for the cap-annealed and capless-annealed MOS diodes, respectively. The dotted line is for the Schottky diode.

Schottky barrier diode. The results are summarized in Fig. 2. Although a high leakage current was measured for the Schottky diode, the MOS diodes indicated marked current suppression. This result justified the use of the Al_2O_3 layer as a gate insulator on the InAlN layer to enhance the barrier for electrons. The carrier density of $2.0 \times 10^{18}\,cm^{-3}$ was evaluated for the bulk InAlN by the capacitance-voltage (C-V) measurement of the Schottky barrier diode in order to use the $1/C^2$-V plot. Therefore, it is highly likely that tunneling through the thin depletion layer under a high electric field contributed to the high current of the Schottky barrier diode at a high negative bias, although the investigation of the detailed mechanism is under way and is beyond the scope of this letter.

The C-V curves measured at 1 MHz for the MOS diodes are shown in Fig. 3 in comparison with the ideal high-frequency C-V curve. Here, the Ni/Au electrode area was 3.14×10^{-4} cm^2. The oxide capacitance C_{ox} was measured using the Si MOS diode with the Al_2O_3 layer deposited

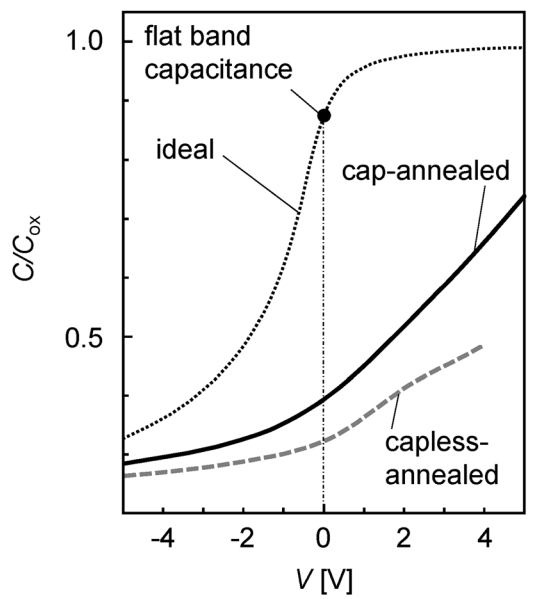

FIG. 3. C-V curves. The solid line indicates the 1 MHz C-V curve for the cap-annealed MOS diode, while the broken line shows that for the capless-annealed one. The dotted line is the high-frequency ideal curve.

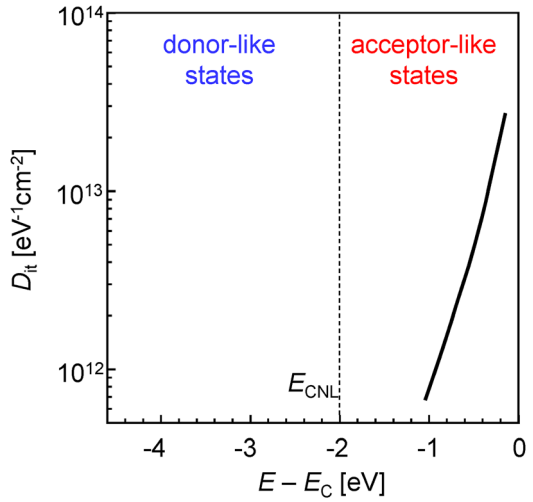

FIG. 4. D_{it} distribution evaluated for the cap-annealed MOS diode.

simultaneously with the InAlN MOS diodes, resulting in a relative dielectric constant ε_r of 9.5. For the cap-annealed sample, the entire capacitance change of the measured C-V curve was large enough to investigate the characteristics of the insulator-semiconductor interface. On the other hand, the capless-annealed MOS diode showed a reduced capacitance change with a low breakdown voltage of around 4 V.

The D_{it} distribution shown in Fig. 4 was evaluated by applying an ordinary high-frequency method to the analysis of the C-V curve of the cap-annealed MOS diode. Since the time constant of interface states deep inside the band gap can become very long compared with the practical measurement time, the evaluation range was limited in the region near the conduction band edge E_C. Nevertheless, D_{it} in the range of $10^{12}\,eV^{-1}cm^{-2}$ was measured in the upper part of the InAlN band gap, although D_{it} should be reduced by further optimization of the fabrication process. For the capless-annealed MOS diode, the D_{it} distribution is not shown here because the measured capacitance values were small corresponding to the surface Fermi level E_{Fsurf} position located deep inside the band gap. As is discussed below, most probably, the high-density acceptor-like interface states should have existed deep inside the band gap to prevent the Fermi level from shifting toward the conduction band, resulting in also a small capacitance change. The high-density interface states of the capless-annealed sample probably resulted from the interface disorder caused by an unintentional and uncontrolled surface oxidation due to trace contamination inside the furnace. The low-voltage breakdown was not seen for the cap-annealed sample despite the wider swing of E_{Fsurf} toward E_C. Therefore, for the capless-annealed sample, it was likely that the high-density interface states terminated the electric field and produced the electric-field stress across the insulator to cause the breakdown. In Fig. 2, the current for the cap-annealed sample was higher than that for the capless-annealed sample at a high positive bias, despite the lower current in the other voltage region. This must have been caused by the closer approach of E_{Fsurf} to E_C for the cap-annealed sample.

Let us discuss the behavior of the Fermi level at the Al_2O_3/InAlN interface of the cap-annealed MOS diode. The flat band voltage V_{FB} of the 1 MHz C-V curve compared with that of the ideal high-frequency curve was very large,

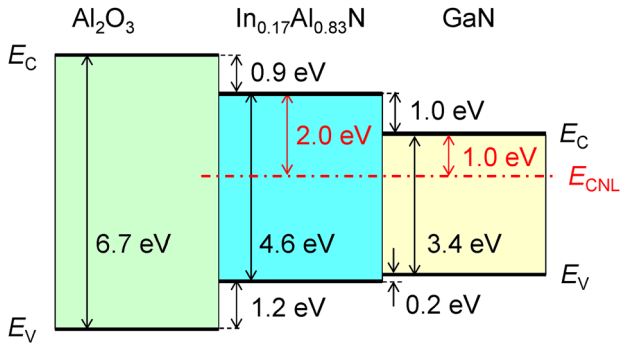

FIG. 5. Schematic band alignment for Al_2O_3-InAlN-GaN system based on our previously reported ΔE_V values[8,12] combined with band gaps reported in Refs. 9–11. The E_{CNL} location is based on the value reported in Ref. 6 for GaN.

beyond the voltage range in Fig. 3. On the basis of our calculation, the bulk Fermi level E_F was close to E_C, i.e., $E_C - E_F = 16$ meV. The quantitative analysis for the origin of V_{FB} has not yet been achieved, mainly because the amounts of fixed charges at the interface and inside the insulator are unclear. Nevertheless, the behavior of E_{Fsurf} in accordance with the applied bias voltage can be discussed as follows. To understand the charging behavior of the interface states, the charge neutrality level E_{CNL}[6] is an important parameter that is intrinsic and independent of any extrinsic factors, e.g., the doping density, fixed charge, and interface state charge. The interface states on the conduction-band side above E_{CNL}, which acts as a boundary, should be acceptor-like states that are ionized negatively when they are occupied by electrons, while those on the valence-band side are donor-like states.[7] For GaN, E_{CNL} is reported to be 2.4 eV above the valence band edge E_V.[6] By considering the valence band offset ΔE_V at the InAlN/GaN interface measured to be 0.2 eV in our previous study,[8] E_{CNL} for $In_{0.17}Al_{0.83}N$ is estimated to be at 2.6 eV above E_V, i.e., 2.0 eV below E_C. To clarify this relation, band alignment among Al_2O_3, InAlN, and GaN is schematically illustrated with E_{CNL} in Fig. 5 using reported bandgap values[9–11] and our measurement results for ΔE_V at the Al_2O_3/InAlN and InAlN/GaN interfaces.[8,12] The E_{CNL} position is also indicated in Fig. 4, which clarifies that the interface states that increased steeply toward E_C should have produced the negative charge to block the shift of E_{Fsurf} toward E_C, in accordance with the positive bias. Consequently, the contribution of the acceptor-like interface states was added to the bias-independent components of V_{FB} including the fixed charges. Thus, V_{FB} should also be decreased by the process optimization for reducing the interface states near the conduction band. Since a similar explanation can be applied to the C-V curve for the capless-annealed MOS diode, the high-density acceptor-like interface states should have existed deep inside the band gap above E_{CNL} to pin E_{Fsurf}.

In conclusion, the ALD-Al_2O_3/InAlN interface formed on a sufficiently thick doped InAlN layer was investigated electrically to evaluate D_{it} near the conduction band. Since the behavior of the interface was dependent on the interface formation process, further process optimization should improve the properties of the ALD-Al_2O_3/InAlN interface. It should be stressed that the interface should be formed carefully, even though InAlN is chemically and thermally stable in nature.

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