Analog Integrated Circuits for the Lotka–Volterra Competitive Neural Networks

Tetsuya Asai, Masashiro Ohtani, and Hiroo Yonezu

***Abstract*— A subthreshold MOS integrated circuit (IC) is designed and fabricated for implementing a competitive neural network of the Lotka–Volterra (LV) type which is derived from conventional membrane dynamics of neurons and is used for the selection of external inputs. The steady-state solutions to the LV equation can be classified into three types, each of which represents qualitatively different selection behavior. Among the solutions, the winners-share-all (WSA) solution in which a certain number of neurons remain activated in steady states is particularly useful owing to robustness in the selection of inputs from a noisy environment. The measured results of the fabricated LV IC's agree well with the theoretical prediction as long as the influence of device mismatches is small. Furthermore, results of extensive circuit simulations prove that the large-scale LV circuit producing the WSA solution does exhibit a reliable selection compared with winner-take-all circuits, in the possible presence of device mismatches.**

***Index Terms*— Analog integrated circuits, neural-network hardware, winner-take-all, winners-share-all.**

I. Introduction

BIOLOGICAL nervous systems are energy efficient and compact. They can efficiently perform flexible information processing in which modern digital computers falter. In recent years, remarkable advances in silicon integrated circuit (IC) fabrication technology have led to the development of very large-scale circuit systems. Using such integration technology, Mead and his colleagues have been developing a neuromorphic hardware which emulates the organization and the function of the nervous systems and tries to reveal the functions of the biological systems [1]–[3]. An analog very large-scale integration (VLSI) is a key technology for implementing such neuromorphic systems since a large number of transistors can be integrated on a small area of a chip, as in biological systems.

In neural networks with mutual inhibition, only significant activities can survive the competition among neurons. For instance in sensory information processing, this implies that salient features in stimuli can be detected by these networks. And according to [4] and [5], such competitive behavior seems to provide a functional basis for neural information processing by the brain, such as decision-making and sequential selection of motor commands. For this potential importance of the activity selection, many competitive neural networks have been discussed in the literature [6]–[11]. Network models, which possess simple organizations and well-understood dynamic behaviors, are attractive from an engineering standpoint. In particular, understanding their behavior is essential for choosing effective values of the parameters which control the system's functions. In this paper, we show experimental results of fabricated IC's for a Lotka–Volterra (LV) neural network which has been fully studied and shown to give three types of steady-state solutions [12]. The LV circuits have been shown to be implemented with a small number of metal-oxide semiconductor (MOS) transistors and were thoroughly inspected using a Simulation Program with Integrated Circuit Emphasis (SPICE) [13].

The three types of solutions in steady states, that is, the winner-take-all (WTA), winners-share-all (WSA), and variant winner-take-all (VWTA) solutions are classified according to the number of active neurons that we call winners, and the dependence of actual winners on initial conditions of neuronal activities. Transitions among the three types are controlled by a single parameter, that is, the ratio of the strength of lateral inhibition to that of self-inhibition. The WTA solution is characterized by the fact that the neuron receiving the largest external input is the only winner. Thus the WTA solution describes the selection of a maximal input. In the WSA solution, at least two neurons remain active as winners in the order of external input strength. The number of winners systematically changes with the strength ratio of the different forms of inhibition. So in both cases, an important feature of the competitive behavior is that the solutions do not depend on initial conditions of neuronal activities. In other words, internal states of the network evolve toward a static representation of the hierarchy in magnitudes of external inputs. On the other hand, in the VWTA solution, which allows a single neuron to remain active, the actual winner changes as the initial conditions change. The behavior of the K-winners-take-all network [7] can be regarded to correspond to the behavior of the LV network in the VWTA solution.

The initial-condition-independent behavior of the network as in the WTA and WSA solutions seems to be particularly useful for applications, since this network can be used to distinguish a particular signal (or a set of signals) from others by estimating scalar values conveyed by the signals. For example, a decision-making process is thought to be the

Manuscript received May 27, 1997; revised December 1, 1998 and June 7, 1999.

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Publisher Item Identifier S 1045-9227(99)07233-1.

selection of one from many possible choices based on the evaluation of each choice with a certain criterion. In this sense, we think that the LV network has a wider applicability than the K-winners-take-all network, which exhibits only the initial-condition-dependent selection among inhomogeneous external inputs [9].

In the LV circuit, MOS transistors operating in their subthreshold regions were used for obtaining an exponential transfer characteristic [14]. The subthreshold MOS operation offers several advantages for implementing neural networks: a possibility of high integration density, low power dissipation, and availability of parasitic bipolar devices. Owing to $O(N)$ complexity of synaptic connections and the use of the subthreshold regions, the LV network is expected to be implemented on a small area of a chip.

On the other hand, according to [15] and [16], we often encounter imperfection of analog integrated circuits due to device mismatches which can be observed among physical parameters of a group of equally designed devices. Although several WTA analog circuits have been proposed in the literature [15], [17]–[21], it is still difficult to select a correct winner since a neuron which should not become the winner can be accidentally activated by the device mismatch. In this paper, we show that the WSA solution can be used to overcome the above difficulties if a high integration density is attained in fabricating the device owing to robustness in the selection of inputs.

This paper is organized as follows. In Section II, after introducing the LV neural network, we summarize equilibrium properties of the LV network. In Section III, we introduce subthreshold MOS circuits for the LV network producing the WTA and WSA solutions. The circuit for the VWTA solution will not be discussed in this paper since we consider it less useful than the circuit for the WTA and WSA solutions. In Section IV, we show the measured results of the fabricated LV IC's. Then in Section V, we show performances of large-scale LV circuits including practical device mismatches using SPICE. Section VI is devoted to summary.

II. The Lotka–Volterra Competitive Neural Network

The LV equation, which describes the competitive behavior among N identical neurons, is given as [12]

$$\tau\frac{dz_i}{dt} = z_i\left(\gamma + W_i - z_i - \lambda\sum_{j\neq i} z_j\right) + \varepsilon \qquad i = 1,\cdots,N \tag{1}$$

where z_i is the activity of the ith neuron, γ represents an input which is nonspecific to each neuron, W_i represents neuron-dependent inputs and ε is a small positive constant (≈ 0). The ε term prevents any z_i from being zero so that losers and winners can interchange if the magnitudes of $\{W_i\}$ are changed occasionally. Each neuron has a self-inhibitory connection of the strength normalized to unity, and λ is the relative strength of all-to-all lateral inhibitory connections among different neurons. The LV equation was derived from the conventional membrane dynamics of neurons with a sigmoid response function and its dynamic properties were analytically studied and shown to give three types of steady-state solutions [12].

Let the external inputs obey

$$W_1 \geq W_2 \geq W_3 \geq \cdots \geq W_{N-1} \geq W_N \geq 0 \tag{2}$$

and $\varepsilon = 0$ for the time being. The qualitative feature of equilibrium solutions is significantly changed with the strength of the lateral inhibition relative to that of the self-inhibition, and the critical strength at which the network behavior changes is roughly given by $\lambda = 1$.

A. WSA Case

The WSA solution of the LV neural network appears when

$$\lambda < \lambda_- \equiv \frac{\gamma + W_1}{\gamma + 2W_1 - W_2}. \tag{3}$$

The number d of winners, which have nonzero activities in steady states, is in general more than one. And the winners are the neurons which receive d largest external inputs among all. The steady-state solution is given by

$$z_i = \frac{1}{\alpha} + \frac{W_i}{1-\lambda} + \frac{\lambda d}{(\lambda-1)\alpha}\langle W\rangle_{\mathcal{D}}$$
$$\alpha \equiv d\lambda + 1 - \lambda, \quad \langle W\rangle_{\mathcal{D}} \equiv \frac{1}{d}\sum_{j=1}^{d} W_j \tag{4}$$

independent of initial values of z_i, in terms of the external inputs $\langle W\rangle_{\mathcal{D}}$ averaged over the winners. The actual number of winners can be determined from

$$\gamma + W_d > \frac{\lambda d}{1-\lambda}(\langle W\rangle_{\mathcal{D}} - W_d). \tag{5}$$

The right side of (5) is an increasing function of d while the left side is a decreasing function of d. Thus there exists an upper bound for d above which condition (5) is not satisfied. This upper bound gives the number of winners.

The condition (5) indicates that the number of winners decreases as the relative strength λ of the lateral inhibition approaches unity. On the other hand, all the neurons remain active for λ less than $\lambda_L \equiv (\gamma+W_N)/(\gamma+W_N+\Sigma_{j=1}^{N} W_j - NW_N)$, which means that no neural selection occurs for $0<\lambda<\lambda_L$. Note that $0<\lambda_L<\lambda_-<1$.

B. WTA Case

The WTA solution is obtained for

$$\lambda_- < \lambda < \lambda_+ \equiv \frac{\gamma + W_1}{\gamma + W_2} \tag{6}$$

with a single neuron allowed to exhibit a nonvanishing activity. The winner is always the neuron which receives the largest external input and is independent of initial conditions. Thus

$$z_1 = \gamma + W_1,$$
$$z_i = 0, \qquad i = 2,\cdots,N \tag{7}$$

in the steady states. The stability of the WTA solution against perturbations from the ε term was extensively studied [22]. Note that $\lambda_+ > 1$ and the WTA behavior occurs only for $\lambda \approx 1$.

C. VWTA Case

When values of the parameter λ are in the range

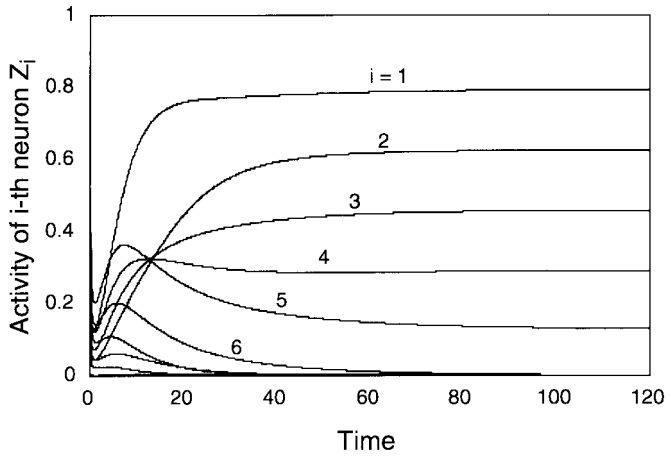
$$\lambda > \lambda_+ \tag{8}$$

the LV network allows only one winner, which is not necessarily the neuron receiving the largest input. In fact, any neuron a can be the winner if the input W_a to the neuron satisfies

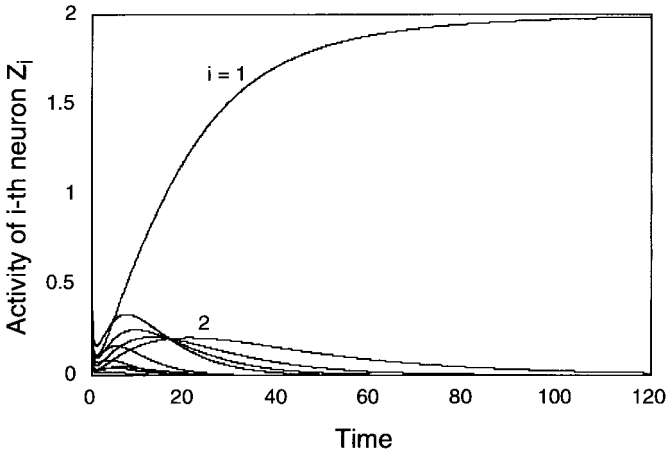
$$\lambda(\gamma + W_a) > (\gamma + W_1). \tag{9}$$

This implies that the actual winner selected by the network depends on initial conditions of neuronal activities. The basin of an attractor is expected to be larger for a neuron receiving a larger external input.

Fig. 1 shows time courses of the LV network with $N = 30, \tau = 1.0$, $\varepsilon = 0.0$, and $\gamma = 1.0$ for $\lambda = 1.0$ (WTA) and 0.8 (WSA) obtained by numerical simulations. The afferent input to the ith neuron is given by $|W_i| \sim N - i$ $(i = 1, \cdots, N)$. Initial states at $t = 0$ were randomly selected in the interval [0, 1]. In Fig. 1(a), it is observed that five neurons $(z_1, z_2, \cdots, z_5)$ remain activated in steady states, which represents the WSA solution. While in Fig. 1(b) it is observed that the neuron receiving the largest input becomes the single winner, that is the WTA solution.



(a)



(b)

Fig. 1. The dynamic behavior of the LV neural network producing the (a) WSA and (b) WTA solutions with $N = 30, \tau = 1.0$, $\varepsilon = 0.0$, and $\gamma = 1.0$ obtained by numerical simulations. Several cells including winners are numbered according to the magnitudes of the external inputs which they receive.

III. Analog Circuits for the Lotka–Volterra Neural Network

By introducing new variables $y_i = \ln z_i$, the LV system described by (1) can be transformed into

$$\begin{aligned}\tau \dot{y}_i &= \gamma' + W_i - \exp(y_i) - \lambda \sum_{j=1, \neq i}^{N} \exp(y_j) \\ &= \gamma' + W_i - (1-\lambda)\exp(y_i) - \lambda \sum_{j=1}^{N} \exp(y_j)\end{aligned} \tag{10}$$

where γ' represents $\gamma + \epsilon \exp(-y_i)$. Note that γ' can be regarded as a fixed input since $\epsilon \approx 0$. Let us introduce the following variable and physical parameters:

$$\begin{aligned} V_i &\equiv \frac{V_T}{\kappa} y_i, \quad \gamma' + W_i \equiv \frac{\exp(-\kappa V_i^{(\mathrm{e})}/V_T)}{1+\beta} \\ \tau &\equiv \frac{C V_T}{I_0 \kappa (1+\beta)}, \quad \lambda \equiv \frac{\beta}{1+\beta} \end{aligned} \tag{11}$$

where V_i represents a transformed variable possessing the dimension of a voltage, $V_T = kT/q$ (k is the Boltzmann's constant, T the temperature, and q the charge of an electron), κ measures the effectiveness of the gate potential, $V_i^{(\mathrm{e})}$ is an external input voltage, C represents a capacitance, I_0 is a MOS fabrication parameter, and β represents a gain constant which is discussed below. We can obtain the following equation from (10) and (11):

$$\begin{aligned} C\dot{V}_i &= I_0 \exp(-\kappa V_i^{(\mathrm{e})}/V_T) \\ &\quad - I_0 \exp(\kappa V_i/V_T) - \beta I_0 \sum_{j=1}^{N} \exp(\kappa V_j/V_T). \end{aligned} \tag{12}$$

It should be noticed that the left side of (12) represents the current of the capacitor, while the right side of the equation is given by the linear combination of saturation currents of MOS transistors operating in the subthreshold region [14]. This implies that the LV network can easily be developed by current-mode subthreshold MOS circuits [15].

In the original LV equation (1), the amount of the lateral inhibition is different among all neurons since the ith neuron is omitted in the lateral inhibition term, that is $-\lambda \sum_{j \neq i}^{N} z_j$. This implies that the complexity of the connection between N neurons is $O(N^2)$. On the other hand, in the transformed equation (12), the lateral inhibition term, that is $-\beta I_0 \sum_{j=1}^{N} \exp(\kappa V_j/V_T)$, is identical with all neurons. Thus, the complexity of the connection becomes $O(N)$. In this way, a large-scale LV network can be implemented on a small area of a chip owing to the $O(N)$ complexity of connections among them. Fig. 2 shows the transformed LV network with $O(N)$ complexity. An inhibitory cell (H cell) receives excitatory signals from excitatory cells (E cells), while

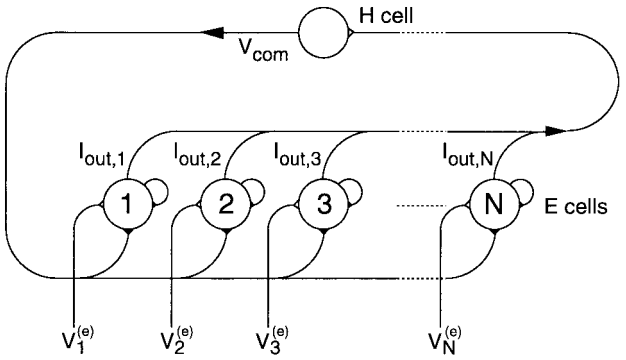


Fig. 2. Network structure of the N-dimensional LV circuit with $O(N)$ complexity. The LV circuit consists of single H-cell circuit and N E-cell circuits, as shown in Figs. 3 and 4.

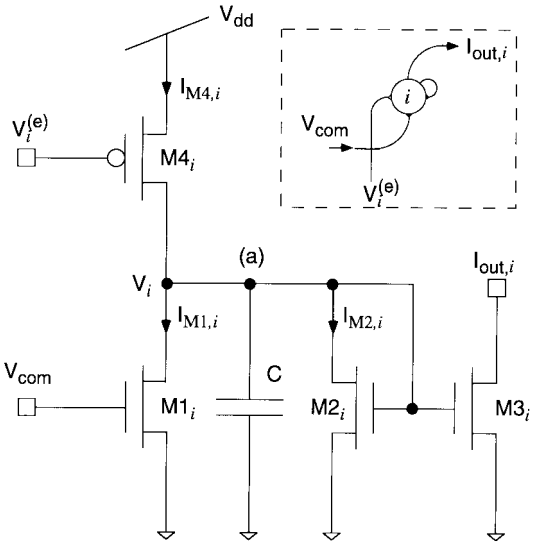


Fig. 3. An excitatory neuron (E cell) circuit composed of four MOS transistors. An external input is given to the circuit through the gate voltage $V_i^{(e)}$ of $M4_i$. The E-cell circuits are connected with the H-cell circuit, shown in Fig. 4, according to the network structure (Fig. 2).

each E cell receives an afferent input, a self-inhibition, and a lateral-inhibition from the H cell.

Fig. 3 represents the ith E-cell circuit and Fig. 4 represents the H-cell circuit. Both circuits were developed by a small number of MOS transistors. In the ith E-cell circuit, the current of $M4_i$, which we denote as $I_{M4,i}$, acts as an excitatory current which increases the membrane potential V_i, while the currents of $M1_i$ and $M2_i$, which we denote as $I_{M1,i}$ and $I_{M2,i}$, respectively, act as lateral- and self-inhibitory currents which decrease the membrane potential. On the other hand, in the H-cell circuit, the input current $I_{\mathbf{in}}$ acts as an excitatory current which increases the output voltage V_{com}.

In the ith E-cell circuit shown in Fig. 3, the node equation around (a) is equivalent to (12). The current of the capacitor corresponds to the left side of (12), while the current of $M4_i$, $M2_i$, and $M1_i$ correspond to the first, second, and third terms of the right side of (12), respectively. It should be noted that the current of $M1_i$ is produced by the H-cell circuit.

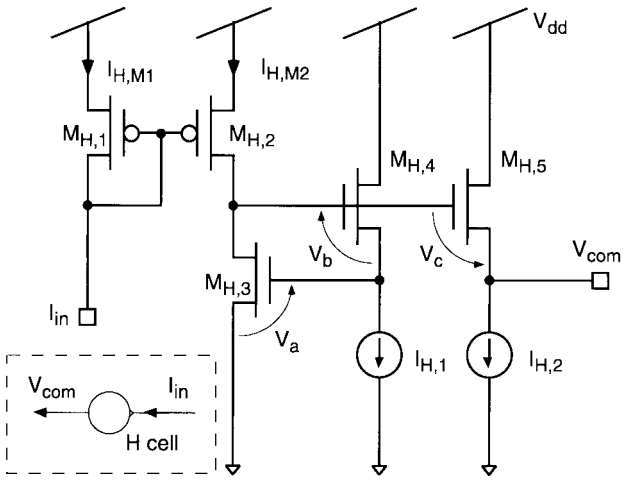


Fig. 4. An inhibitory neuron (H cell) circuit composed of five MOS transistors and two current sources.

The H-cell circuit consists of a translinear circuit that performs a normal product computation [15], as shown in Fig. 4. The input current to the H-cell circuit $I_{\mathbf{in}}$ is mirrored to $I_{\mathrm{M1},i}$ in the ith E-cell circuit with a gain constant β through the common output voltage V_{com}. The gain constant β is given by the ratio of $I_{\mathrm{H},1}$ to $I_{\mathrm{H},2}$ which determines the strength of the lateral inhibition. The strength of the inhibition is externally modifiable by replacing current sources $I_{\mathrm{H},1}$ and $I_{\mathrm{H},2}$ with nMOS transistors. A detailed description of the E-cell circuit and H-cell circuit is given in the Appendix.

In the original LV equation (1), the activity of the ith neuron (z_i) is restricted in the range of $[0, \gamma + W_i]$. Due the system variable changing $(y_i = \ln z_i)$, the range of the transformed system becomes $[-\infty, \ln(\gamma' + W_i)]$, which results in $y_i \to -\infty$ when $z_i \to 0$. This divergence to negative infinity, however, never occurs in the proposed circuit. When $V_i \leq 4V_T$ and $\mathrm{M1}_i$ starts to leave the saturation region, the second term of the right side of (12) ceases to be valid. Consequently, the lateral inhibition term represented by $-\beta I_0 \ \Sigma_{j=1}^{N} \ \exp(\kappa V_j / V_T)$ in (12) decreases rapidly to zero, rather than to I_0, as V_i approaches zero in the equation for the losers. This indicates that V_i does not go to negative infinity for the losers because the driving term itself vanishes. Thus the losers acquire a small nonvanishing V_i, giving $z_i > 0$.

Equation (3) predicts that the LV circuit produces the WSA solution when

$$\frac{\beta}{1+\beta} < \frac{I_{\mathrm{M4},1}}{2I_{\mathrm{M4},1} - I_{\mathrm{M4},2}}$$
$$I_{\mathrm{M4},1} \geq I_{\mathrm{M4},2} \geq I_{\mathrm{M4},3} \geq \cdots I_{\mathrm{M4},N-1} \geq I_{\mathrm{M4},N} \geq 0 \ \mathrm{A} \quad (13)$$

where $\beta \equiv I_{\mathrm{H},1}/I_{\mathrm{H},2}$. Equation (13) indicates that the boundary between the WTA and WSA solutions is determined by 1) the ratio of the largest afferent input of the E cell $(I_{\mathrm{M4},1})$ to the second largest $I_{\mathrm{M4},2}$ and 2) the ratio of the current sources in the H-cell circuit (β). Thus, one can choose those parameters so that the LV circuits may produce the WSA or WTA solution.

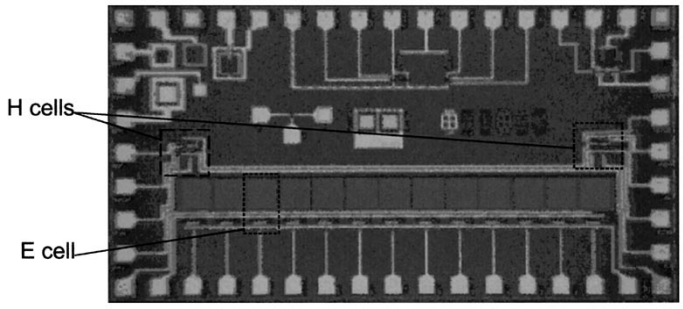
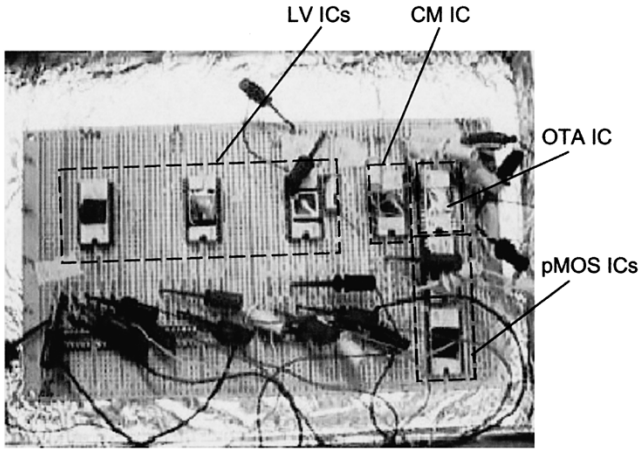
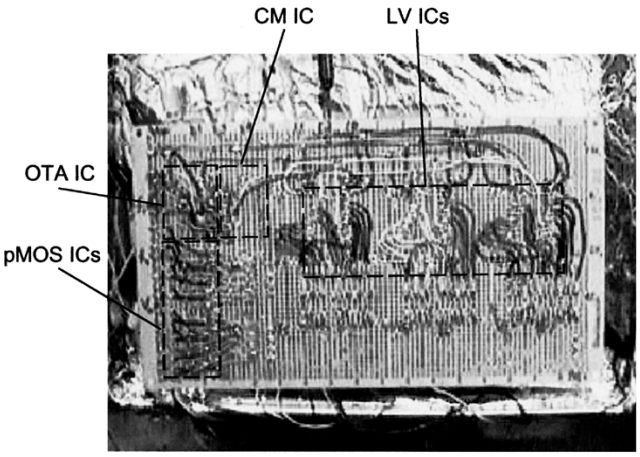


Fig. 5. Chip photograph of the fabricated LV circuit including 13 E-cell circuits and 2 H-cell circuits (chip size: 5.1 mm × 2.8 mm, feature size: 10 μm, nMOS process). The pMOS transistors used in the E-cell and H-cell circuits were not implemented on the chip, but were fabricated in another process.



(a)

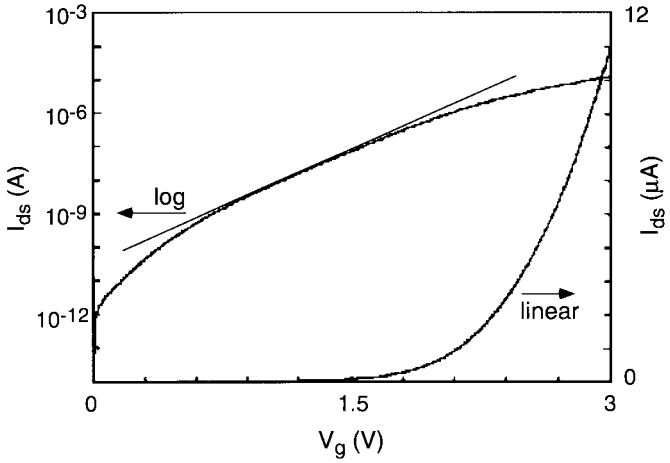


(b)

Fig. 6. (a) Front and (b) back side photographs of the LV circuit implemented on the printed board ($N = 39$). The network consists of three LV IC's, three afferent input IC's including current sources, and a pMOS current mirror.

IV. Experimental Results

We fabricated prototype LV IC's in a 10-μm nMOS process at the Electron Device Research Center in Toyohashi University of Technology. Fig. 5 shows a chip photograph which contains 13 E-cell circuits and 2 H-cell circuits without pMOS transistors. The pMOS transistors used in the E-cell circuits and H-cell circuits were fabricated in another process. Using three LV IC's, we constructed the LV network with $N = 39$, as shown in Fig. 6. It is seen that a connection density among the LV IC's is significantly reduced so that the LV network with very high integration density can be developed on one chip with the proposed circuit.



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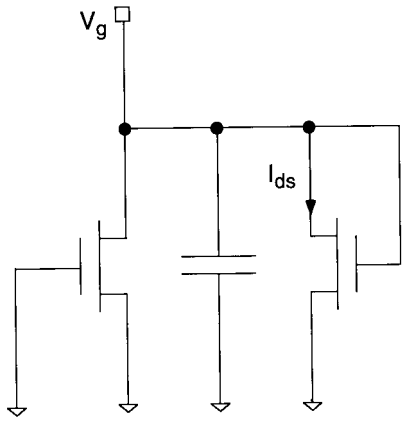
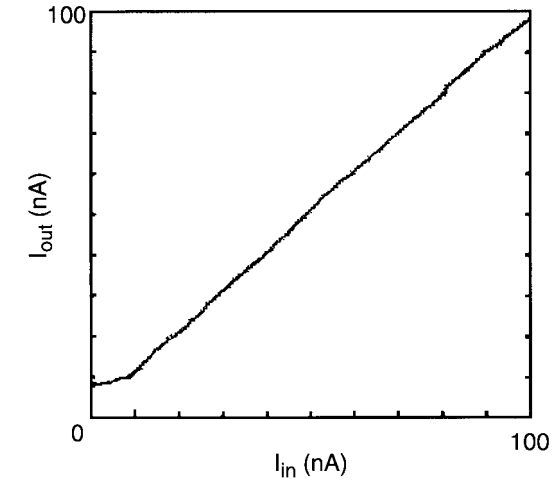


(b)

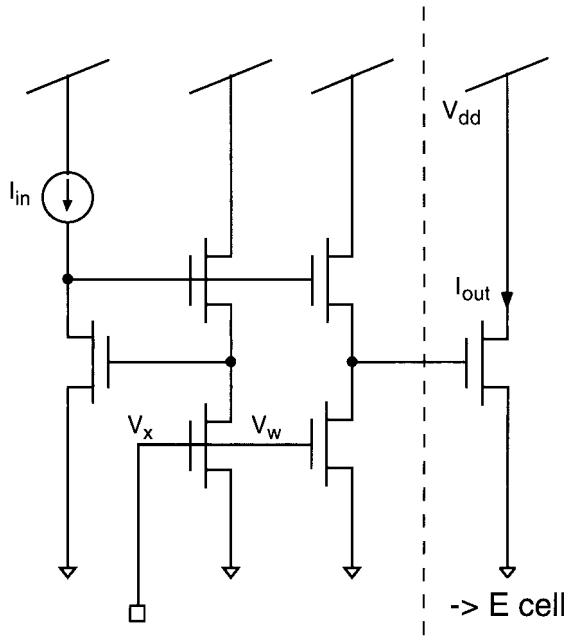
Fig. 7. (a) Drain–source current of the diode-connected nMOS transistor in the E-cell circuit. (b) Measured circuit.

Fig. 7(a) and (b) shows the drain-source current of the diode-connected nMOS transistor used in the E-cell circuit and its measured circuit, respectively. The exponential region of the nMOS transistor was approximately obtained as $0.8\ \text{V} < V_g < 1.8\ \text{V}$, while the nominal "threshold" voltage of the transistor was approximately obtained as 2.0 V. Due to the gate-oxide thickness of fabricated MOS transistors in our CMOS process ($T_{\text{ox}} \geq 1000$ Å), the S factor became 0.4 V/decade, which results in rather a long time reaching to the equilibrium state, as compared with LV circuits fabricated in the standard CMOS process. However, such large S factor does not influence the qualitative behavior of the LV circuit since the factor influences only I_0 and κ with respect to the time constant τ in (11).

The input–output characteristic of the H-cell circuit and its measured circuit are shown in Fig. 8(a) and (b), respectively.



(a)



(b)

Fig. 8. (a) Measured input–output characteristic of the H-cell circuit. (b) Measured circuit.

In the experiment, V_x was set at 2.0 V and V_w was set at 2.0 V. It was shown that the output current was widely proportional to the input current. The gain constant β obtained from Fig. 8(a) was approximately unity, as expected.

Fig. 9 shows measured equilibrium voltages $V_{1,2,3,4}|_{t\to\infty}$ of the LV circuit with $N = 39$ as a function of the afferent input current $I_{\mathrm{M4},1} = 1$ nA to 200 nA. The rest input currents $I_{\mathrm{M4},2}, I_{\mathrm{M4},3}, I_{\mathrm{M4},4}$, and $I_{\mathrm{M4},(5,6,\cdots,39)}$ were set at 20, 40, 60 nA, and 0 A, respectively. The semiconductor parameter analyzer 4145B (Hewlett Packard, Inc.) was used for producing those afferent currents instead of the pMOS transistors in the E-cell circuits. In the experiment, the gain constant β was fixed at unity ($\lambda = 0.5$). It should be noticed that the LV circuit with those parameters produces the WSA solution since the parameters satisfy (13).

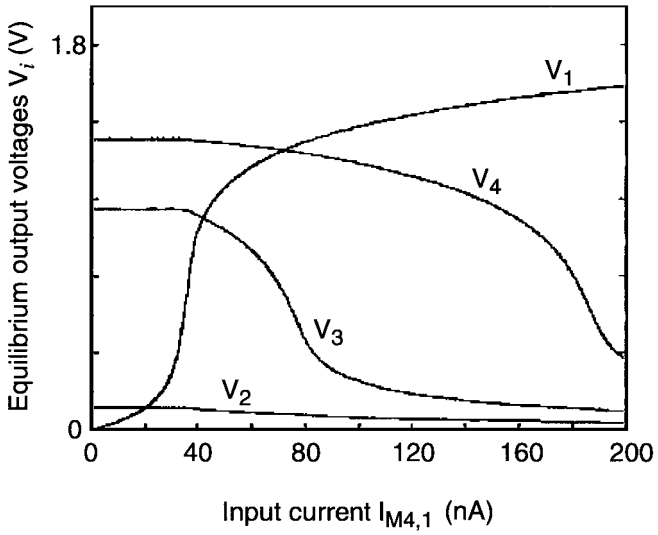


Fig. 9. The distribution of equilibrium voltages for the input currents $(I_{\mathrm{M4},1}, I_{\mathrm{M4},2}, I_{\mathrm{M4},3}, I_{\mathrm{M4},4}, I_{\mathrm{M4},(5,\cdots,39)}) = (1 \sim 200,$ 20, 40, 60, 0) nA, $V_x = V_w = 2.0$ V ($\beta = 1.0$), and $V_{\mathrm{dd}} = 9$ V. The horizontal and vertical axes represent $I_{\mathrm{M4},1}$ and $V_{1,2,3,4}$, respectively. Other equilibrium voltages ($V_{5,\cdots,39} \approx 0$ V) are independent of $I_{\mathrm{M4},1}$.

When $I_{\mathrm{M4},1} < 20$ nA, the equilibrium voltages of the E-cell circuits satisfied the inequality $V_1 < V_2 < V_3 < V_4$ and $V_{5,6,\cdots,39} \approx 0$ V since $I_{\mathrm{M4},1} < I_{\mathrm{M4},2} < I_{\mathrm{M4},3} < I_{\mathrm{M4},4}$ and $I_{\mathrm{M4},(5,6,\cdots,39)} = 0$ A. When $I_{\mathrm{M4},1} = 20$ nA, V_1 agreed with V_2, as expected. If 20 nA $< I_{\mathrm{M4},1} < 40$ nA, the equilibrium voltages became $V_2 < V_1 < V_3 < V_4$ since $I_{\mathrm{M4},2} < I_{\mathrm{M4},1}$. When $I_{\mathrm{M4},1} = 40$ nA, V_1 must be equal to V_3, however, V_1 did not coincide with V_3 but they coincided when $I_{\mathrm{M4},1} = I_{\mathrm{M4},3} + \Delta I \approx 43$ nA ($\Delta I \approx 3$ nA) because of the device mismatches of the MOS transistors. When 43 nA $< I_{\mathrm{M4},1} < 60$ nA, the equilibrium voltages became $V_2 < V_3 < V_1 < V_4$ and V_1 coincided with V_4 when $I_{\mathrm{M4},1} \approx 72$ nA ($\Delta I = 12$ nA) due to the mismatches. When $I_{\mathrm{M4},1} > 72$ nA, the equilibrium voltages satisfied $V_2 < V_3 < V_4 < V_1$, as expected.

The winner will not be influenced by the device mismatch in the H-cell circuit since the mismatch influences only the gain constant β which determines the type of the solution (WSA or WTA) according to (13). On the other hand, the mismatch of $\mathrm{M1}_i$ in the ith E-cell circuit directly influences the strength of the lateral inhibition of the E-cell circuit, while that of $\mathrm{M4}_i$ does the afferent input current. The measured results reveal that the fabricated circuit requires a current difference of at least $O(10$ nA) between the afferent input currents in order to determine the correct winners among the E-cell circuits.

The time course of the membrane voltages $V_{1,2,3,4}$ of the E-cell circuits for $\beta = 1.0$ is shown in Fig. 10. In the experiment, the afferent input currents $I_{\mathrm{M4},(1,2,3,4)}$ to the E-cell circuits are given by off-chip pMOS transistors. The rest of the input currents $I_{\mathrm{M4},(5,6,\cdots,39)}$ were set at 0 A. The result shown in Fig. 10 is consistent with the prediction obtained from the theory and the computer simulations. It should be noticed that the difference between equilibrium currents of the E-cell circuits $(I_{\mathrm{M2},(1,2,3,4)})$ becomes more conspicuous compared with the equilibrium voltages $V_{1,2,3,4}$ because of

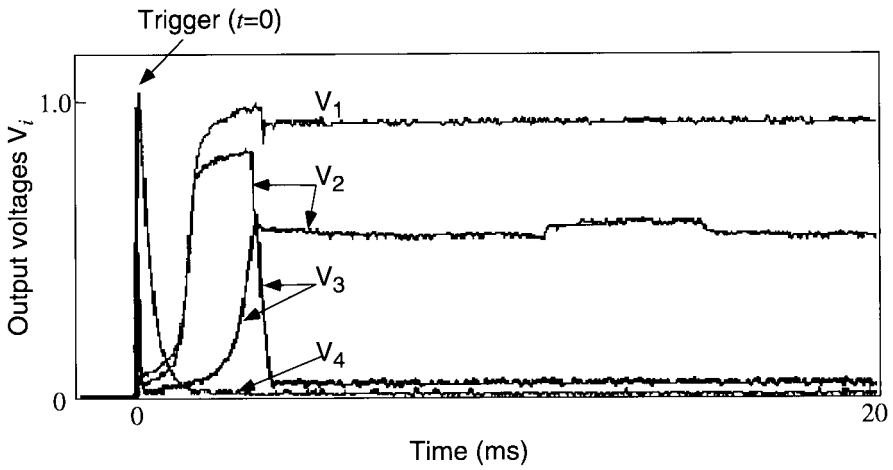


Fig. 10. Transient responses of the LV circuit with $N = 39$, $V_1^{(e)} < V_2^{(e)} < V_3^{(e)} < V_4^{(e)}$, $V_x = V_w = 2.0$ V ($\beta = 1.0$) and $V_{dd} = 9$ V. The vertical axis represents the membrane voltages of E-cell circuits ($V_{1,2,3,4}$) receiving external inputs.

the logarithmic relation between the original LV equation (1) and the transformed equation (12).

As we mentioned in Section I, selecting a single winner with WTA circuits is quite difficult under a noisy environment. The above results indicated that the practical device mismatches could be a conclusive drawback for determining the correct winner. In the following section, we show that the WSA solution produced by the LV circuit can be used effectively to overcome the above problem on the basis of a collective neural processing.

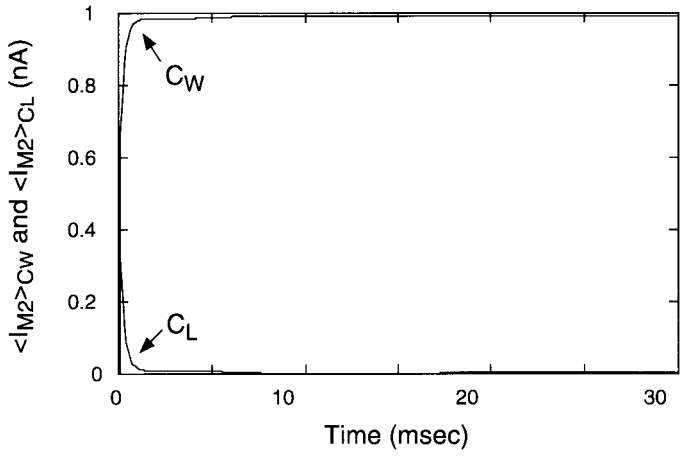
V. An Expansion to a Large-Scale Network: Is Collective Operation Necessary for a Correct Information Processing?

In the preceding section, we confirmed that the fabricated LV circuit with small N could select multiple winners according to the magnitude of the afferent inputs as long as the minimum difference between the inputs was within $O(10$ nA$)$. Our next interest is the behavior of large-scale LV circuits which can be used to overcome the possible problem of device mismatches. Since the prototype LV chip includes only 13 E-cell circuits, it is rather difficult to construct a large-scale network with them. Therefore, we conducted SPICE simulations of the large-scale LV network using device mismatches obtained from our fabricated LV IC's.

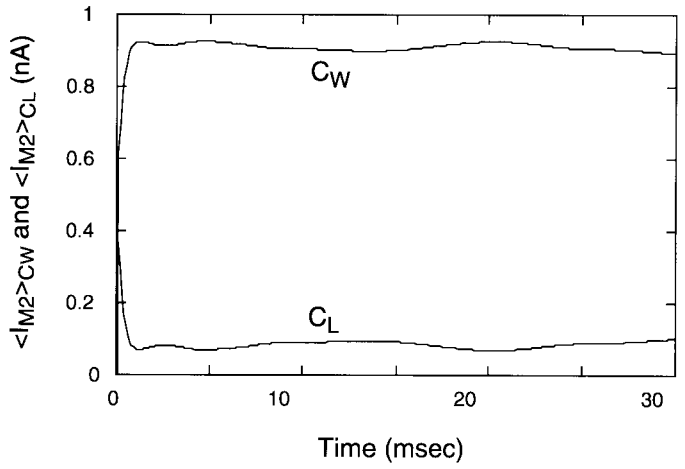
In order to overcome the influences of the device mismatch, we assume the following conditions: 1) the LV circuit with large N produces the WSA solution; 2) the network is split into several clusters; 3) each cluster consists of several E-cell circuits; 4) E-cell circuits within the same cluster receive the same magnitude of an afferent input current; and 5) the output of each cluster is represented by the average of the output current of the E-cell circuits in the cluster. The cluster receiving the largest input among the clusters, which we denote as cluster C_W, will become a winning cluster when the mismatch parameters are not given to the circuit. On the other hand, in the presence of the mismatches, several E-cell circuits in the cluster C_W will become losers, while some E-cell circuits in the rest clusters C_L will become winners. If the size of the cluster is sufficiently large, those singular losers and winners will not influence the output of the clusters according to "the decision by majority" resulting from condition v). It should be noticed that such collective decision of the winner is certainly owing to the existence of multiple winners produced by the LV circuits with the WSA solution. In the following simulation, we confirm whether this approach is valid or not for practical device mismatches.

In the simulation, N is set at 200 and β is set at 1.0 with respect to condition 1). For conditions 2) to 4), the cluster size M is set at 100 and two different magnitudes of the input currents are given to the clusters. The high input currents (100 nA) are given to a cluster C_W consisting of M E-cell circuits, while the rest cluster C_L consisting of M E-cell circuits receives slightly low input currents compared with the input current of the cluster C_W. In the following simulations, we denote the differential current between the input currents of C_W and C_L as ΔI_{WL}. The mismatch parameters and variations used in the simulation are dimensions of MOS transistors (± 0.1 μm), V_T (± 0.05 V), C (± 0.2 pF), and κ (± 0.02). Those variations were obtained from the fabricated LV circuits in our CMOS process.

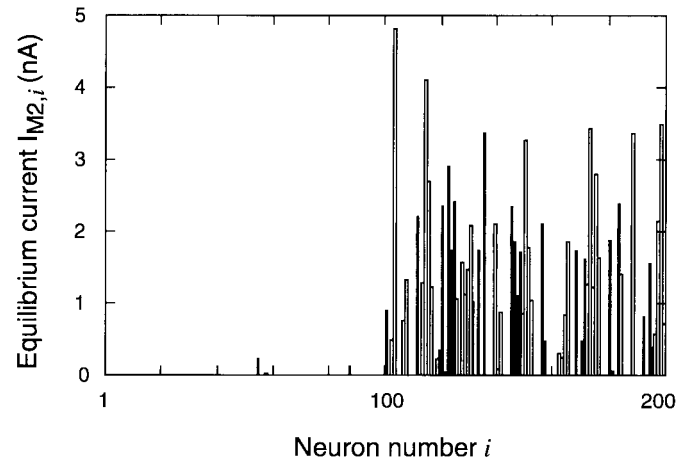
Fig. 11 shows transient responses and an equilibrium distribution of output currents of the clusters C_W and C_L, which we denote as $\langle I_{\mathrm{M2}} \rangle_{C_W}$ and $\langle I_{\mathrm{M2}} \rangle_{C_L}$, respectively. When the cluster C_L received the input current of 97 nA ($\Delta I_{\mathrm{WL}} = 3$ nA), the cluster C_W became the winner at the equilibrium, as shown in Fig. 11(a). The differential output current between $\langle I_{\mathrm{M2}} \rangle_{C_W}$ and $\langle I_{\mathrm{M2}} \rangle_{C_L}$ was sufficiently large for determining the single winning cluster (C_W). In this case, E-cell circuits in the cluster C_W were activated with high probabilities, while E-cell circuits in the cluster C_L were nearly dead at the equilibrium, as shown in Fig. 11(c). On the other hand, when the cluster C_L received the input current of 98 nA ($\Delta I_{\mathrm{WL}} = 2$ nA), $\langle I_{\mathrm{M2}} \rangle_{C_W}$ and $\langle I_{\mathrm{M2}} \rangle_{C_L}$ showed oscillatory behavior, as shown in Fig. 11(b). Oscillation of winning status will be observed when the input to the cluster C_W are very close to the input to the cluster C_L.



(a)



(b)



(c)

Fig. 11. Transient responses of $\langle I_{\rm M2}\rangle_{C_W}$ and $\langle I_{\rm M2}\rangle_{C_L}$ when the input currents of the cluster C_L was set at 97 nA (a) and 98 nA (b). The cluster size, input currents of the cluster C_W. and β were fixed at 100, 100 nA, and 1.0, respectively. (c) Output-current distribution of the E-cell circuits at the equilibrium state.

These results indicate that $\Delta I_{\rm WL}$ must be larger than 3 nA in order to avoid the oscillation of winning status and determine the correct winning cluster when $M = 100$ and $\beta = 1.0$.

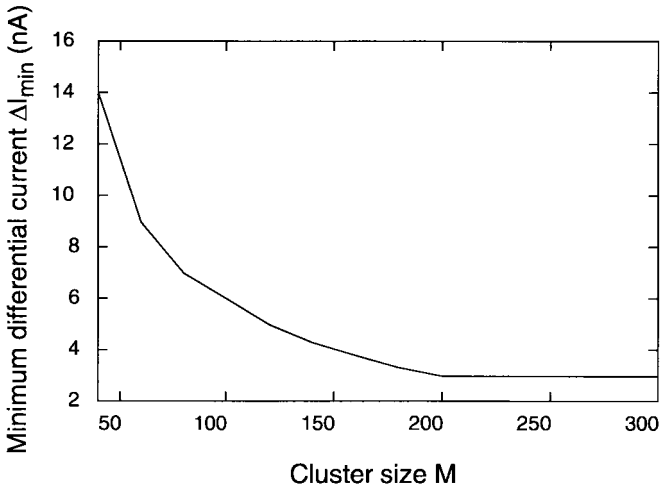


Fig. 12. Dependence of the minimum differential current $\Delta I_{\rm min}$ on the cluster size M.

We denote the minimum value of $\Delta I_{\rm WL}$ as $\Delta I_{\rm min}$. Fig. 12 shows the dependence of $\Delta I_{\rm min}$ on the cluster size M. In the simulations, we assume that the clustered LV circuit shows the WTA behavior when

$$D \equiv \frac{\langle I_{\rm M2}\rangle_{C_W}}{\langle I_{\rm M2}\rangle_{C_W} + \langle I_{\rm M2}\rangle_{C_L}} \geq 0.99. \tag{14}$$

When $M \leq 60, \Delta I_{\rm min}$ was $O(10$ nA). As $M \rightarrow \infty$, $\Delta I_{\rm min}$ asymptotically approached to 3 nA.

These results indicate that the values of the required difference between afferent input currents for selecting the correct winning cluster is $O(1$ nA) when $M > 60$. Namely, it was shown that reliability of the selection could be considerably improved by using the clustered LV circuit, as compared with the conventional WTA circuits and individual LV circuit shown in section IV. Thus, "the decision by majority" approach, which is certainly owing to the WSA solution of the proposed LV circuit, seems to be valid in the analog circuits with practical device mismatches.

VI. Summary

We fabricated analog MOS integrated circuits for a LV competitive neural network and showed their characteristics and performances.

The present LV circuit has several merits in applications. First, the underlying mechanism for the selection is both qualitatively and quantitatively known for WTA and WSA cases. This makes it easier to design a neural circuit suitable for a particular application. Second, the competitive behaviors occur independently of initial conditions. This dynamic property is useful for constructing an appropriate internal representation of the hierarchy in the magnitudes of external inputs which may vary in time. Third, by introducing an inhibitory cell, the complexity of connections is easily reduced to $O(N)$. Fourth, adopting exponential transfer characteristics for a neuron unit removes the quadratic interaction terms from the original LV neural network. This makes the circuit organization extremely simple. Fifth, the electric power dissipation from the circuit is

expected to be very small since the MOS transistors are used in their subthreshold regions of operation.

The experimental results showed that the fabricated LV circuit could produce a WSA solution and select multiple winners according to the magnitude of afferent input currents as long as the minimum difference between the input currents was within $O(10\,\mathrm{nA})$. Large-scale SPICE simulations were also conducted to show that the proposed circuit could overcome influences of device mismatches by the WSA solutions. Introducing clusters of neural circuits, it was shown that the values of the required difference between afferent input currents for selecting the correct wining cluster was within $O(1\ \mathrm{nA})$ when the cluster size was larger than 60.

APPENDIX

Here, we will show that the proposed LV circuit is equivalent to (12) when the E-cell circuits and H-cell circuit are arranged according to the network structure shown in Fig. 2.

Applying Kirchhoff's current law (KCL) at node (a) in Fig. 3, we can obtain the equation

$$C\dot{V}_i = I_{\mathrm{M4},i} - I_{\mathrm{M1},i} - I_{\mathrm{M2},i} \tag{A.1}$$

where $I_{\mathrm{M}a,i}$ stands for the current of transistor Ma_i of the ith E-cell circuit. In the subthreshold region of operation, $I_{\mathrm{M2},i}$ is ideally given by

$$I_{\mathrm{M2},i} = I_0 \exp(\kappa V_i/V_T) \tag{A.2}$$

where I_0, V_T, and κ are the physical parameters described in Section III. Similarly, $I_{\mathrm{M1},i}$ is given as

$$I_{\mathrm{M1},i} = I_0 \exp(\kappa V_{\mathrm{com}}/V_T) \tag{A.3}$$

in terms of the gate–source voltage V_{com} of M1$_i$, as long as it operates in the saturation region $(V_i \geq 4V_T)$. The current mirror consisting of M2$_i$ and M3$_i$ implies that the output current of the ith E-cell circuit $I_{\mathrm{M3},i}$ is equal to $I_{\mathrm{M2},i}$. Applying KCL at the input terminal of the H-cell circuit, we obtain the current $I_{\mathrm{H,M1}}$ of $\mathrm{M}_{\mathrm{H},1}$ in the H-cell circuit as

$$I_{\mathrm{H,M1}} = I_0 \sum_{j=1}^{N} \exp(\kappa V_j/V_T) \tag{A.4}$$

which is equal to $I_{\mathrm{H,M2}}$ due to the current mirror structure of $\mathrm{M}_{\mathrm{H},1}$ and $\mathrm{M}_{\mathrm{H},2}$.

The current $I_{\mathrm{H,M2}}$ needs to be mirrored to $I_{\mathrm{M1},i}$ in the ith E-cell circuit with an externally modifiable ratio. To this end, the transistors $\mathrm{M}_{\mathrm{H},3}$, $\mathrm{M}_{\mathrm{H},4}$, and $\mathrm{M}_{\mathrm{H},5}$ in the H-cell circuit and M1$_i$ $(i = 1, 2 \cdots N)$ in the E-cell circuits are employed as a translinear multiplier/divider [15]. Then the conservation of energy imposes the following relation on the voltages in the H-cell circuit:

$$V_a + V_b + V_c + V_{\mathrm{com}} = 0 \tag{A.5}$$

where V_a, V_b, and V_c stand for the gate-source voltages of transistors $\mathrm{M}_{\mathrm{H},3}$, $\mathrm{M}_{\mathrm{H},4}$, and $\mathrm{M}_{\mathrm{H},5}$, respectively. Representing the gate-source voltages with their respective drain-source subthreshold currents, and assuming that all devices have identical values for κ and I_0, we obtain

$$\frac{V_T}{\kappa}\ln\left(\frac{I_{\mathrm{H,M1}}}{I_0}\right) + \frac{V_T}{\kappa}\ln\left(\frac{I_{\mathrm{H},1}}{I_0}\right) - \frac{V_T}{\kappa}\ln\left(\frac{I_{\mathrm{H},2}}{I_0}\right) - \frac{V_T}{\kappa}\ln\left(\frac{I_{\mathrm{M1},i}}{I_0}\right) = 0. \tag{A.6}$$

From (A.4) and (A.6), we can easily derive

$$I_{\mathrm{M1},i} = \frac{I_{\mathrm{H},1}}{I_{\mathrm{H},2}} I_{\mathrm{H,M1}} = \beta I_0 \sum_{j=1}^{N} \exp(\kappa V_j/V_T) \tag{A.7}$$

where β represents the ratio of $I_{\mathrm{H},1}$ to $I_{\mathrm{H},2}$. By replacing the current sources for $I_{\mathrm{H},1}$ and $I_{\mathrm{H},2}$ with nMOS transistors, β is rendered externally modifiable through the gate voltages of those transistors.

The afferent input to each E-cell circuit is given by an input current to transistor M4$_i$. Therefore, the strength of the afferent input can be externally controlled by changing the gate voltage $V_i^{(\mathrm{e})}$ of M4$_i$ through

$$I_{\mathrm{M4},i} = I_0 \exp(-\kappa V_i^{(\mathrm{e})}/V_T). \tag{A.8}$$

Here $V_i^{(\mathrm{e})}$ must be in the range which ensures the operation of M4$_i$ in the subthreshold region.

By substituting (A.2), (A.7), and (A.8) into (A.1), we obtain

$$C\dot{V}_i = I_0 \exp(-\kappa V_i^{(\mathrm{e})}/V_T) - I_0 \exp(\kappa V_i/V_T) - \beta I_0 \sum_{j=1}^{N} \exp(\kappa V_j/V_T), \tag{A.9}$$

which corresponds to (12) discussed in Section III.

ACKNOWLEDGMENT

The authors thank Prof. T. Fukai of Tokai University and Dr. S. Tanaka of the Institute of Physical and Chemical Research (RIKEN) for their fruitful discussion. They also thank H. Ikeda, D. Sudo, T. Sugiura, and colleagues of Toyohashi University of Technology, for their cooperation as they were indispensable for completing the present research.

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