Fabrication of one-dimensional GaAs channel-coupled InAs quantum dot memory device by selective-area metal-organic vapor phase epitaxy

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There has been growing interest in quantum dot information storage devices using quantum dots (QDs) as storage media. The operation of a quantum dot memory (QDM) device depends on the discrete emission and capture of electrons, and not on the average behavior of hundreds of thousands of electrons, as is the case in today’s flash memory devices. In general, the QDM devices mainly consist of a quantum dot layer to store electrons and a channel in close vicinity to sense them.1–5 The storing and releasing of electrons into and from the QD energy levels is solely determined by the voltage of a control gate. While many studies of silicon QDM devices have addressed various key features, such as fabrication, room-temperature operation, the single electron charging effect, etc.,1,2 only a few have addressed InAs QDM devices and most of them comprising several electrons to operate.3–5

Since storing information in an economic way requires high packaging density and low power consumption, the number of QDs must be reduced, and, consequently, the sensing channel should also be sufficiently reduced to enable sensing of a small potential change in the QDs caused by charging and discharging effects.Selective-area metalorganic vapor phase epitaxy (SA-MOVPE) growth is a key technology in fabricating various kinds of semiconductor nanostructures and their integrated circuits in high density.6 We have, therefore, attempted to fabricate an InAs QDM device using SA-MOVPE. The self-limited growth mechanism associated with SA-MOVPE grown GaAs wafers on masked GaAs (001) substrates naturally reduces the top width.6,7 We utilized this natural width reduction mechanism to define narrow channels and then grew a few InAs QDs on the top to complete a memory structure requiring few electrons to operate.

We first defined a narrow wirelike opening with a length of 4 μm in the [−110] direction and a width of 600 nm in the [110] direction on SiO2-masked GaAs (001) substrates by electron-beam lithography and wet chemical etching. Using a low-pressure MOVPE system operating at 76 Torr, we grew a GaAs double-hetero-high-electron mobility transistor (DH-HEMT) channel8 in this opened area, followed by InAs QDs to complete the memory structure. The growth sequence of the channel and the related thicknesses were a 250 nm GaAs buffer layer, a 50 nm Al0.3Ga0.7As layer, an 18 nm GaAs well layer, a 10 nm Al0.3Ga0.7As spacer layer, a 25 nm Si-doped Al0.3Ga0.7As layer, and a 10 nm GaAs capping layer. The growth temperature was 700 °C. After fabrication of the channel, the growth temperature was reduced to 440 °C in 5 min, and then InAs QDs were grown in Stranski-Krastanow growth mode. A 20-nm-thick GaAs capping layer was grown at the same temperature without interruption to cover the dots, then the temperature was increased to 600 °C for a further growth of 50-nm-thick GaAs as a second capping layer. Two similar structures were also grown for comparative and quantum dot analysis, in which one sample had no QDs layer and the other had no top capping layer. The source materials used for this growth were trimethylgallium (TMG), trimethylaluminum (TMA), trimethylindium (TMI), and 20% arsine in purified hydrogen. The partial pressures of the TMG and TMA were 3.4 × 10−6 and 6.8 × 10−7 atm, respectively. The partial pressure of the arsine was 1.1 × 10−4 atm for the GaAs well layer and 5.3 × 10−4 atm for the AlGaAs layer. The partial pressures of the TMI and arsine for the InAs QD layer were 4.2 × 10−7 and 5.3 × 10−7 atm, respectively. After the completion of growth, Ge/Au/Ni/Au metals were deposited and annealed at 450 °C for 5 min as an Ohmic contact, and then Cr/Au metals were deposited as gate electrodes. Electron-beam lithography and photolithography, together with the standard lift-off process, were used to define the electrodes. The carrier density and mobility of two-dimensional electron gas (2DEG) on a planar reference sample at 77 K were 1.0 × 1012 cm−2 and 5.3700 cm2/V s, respectively.

Figures 1(a) and 1(b) show a scanning electron microscope (SEM) image of the SA-MOVPE grown device structure and a schematic representation of the memory device and its equivalent circuit. Because of the self-limited growth
mechanism, the top width of the wire was reduced to 200 nm, as shown in Fig. 1(a). Figures 1(c) and 1(d) show the growth layer details and the corresponding schematic conduction-band profile. To determine the number of buried QDs and the size distribution, we conducted the SEM and atomic force microscope (AFM) analyses on uncapped samples, grown separately but under similar growth conditions. The SEM analysis on an uncapped wire pattern showed InAs QDs with a size distribution of 10–30 nm and with an average density of 25 dots/0.1 μm². Ex situ AFM investigations on uncapped planar samples showed that the QDs had a height of less than or equal to 8 nm. The mechanism of InAs dot formation on GaAs (001) substrate is reported elsewhere. Details of the InAs dot formation on top of the GaAs wires by SA-MOVPE are reported elsewhere.

The memory characteristics of our device, mounted on a cryohead where the temperature could be varied from 20 to 300 K, were measured using a semiconductor parameter analyzer. Figure 2(a) shows the measured hysteresis behavior of our device at 20 K. The drain current was measured, in the dark, for a fixed source drain voltage (V_DS) of 100 mV by scanning the gate voltage (V_G) from −0.4 to 1.0 V and back. The reverse scanning resulted in a positive voltage shift in the drain current, showing a clockwise hysteresis with a ∆V_{th} of 165 mV. A similar measurement on a sample with no QDs showed no hysteresis effect. Therefore, the positive shift in our sample with QDs can be attributed to electron capturing at QD energy levels.

The scanning in our sample was started from −0.4 V, in steps of 0.1 V, up to a positive maximum gate voltage V_{G_{max}}, at which the QDs would be fully charged. Figure 3(a) shows that there was a clear shift in ∆V_{th} depending on the gate voltage scanning range. As the number of electrons involved in the charging process increased with the gate voltage, an increasing shift in ∆V_{th} was obtained. For the present device, ∆V_{th} increased linearly (the linear nature was due to the size distribution of the QDs) up to 1.0 V and then saturated, as shown in the insert of Fig. 3(a). This means that scanning between −0.4 and 1.0 V and back corresponds to a fully charged state.

The charging and discharging process in our device works as follows. In the forward scanning, the QD energy levels are lowered below the Fermi level, so electrons are transferred from the channel to the QD energy levels, leading to a decrease in the channel carrier concentration. During the reverse scanning, because the stored electrons are not released immediately, the magnitude of the current flowing through the channel is less, resulting in clockwise hysteresis. However, when the reverse scanning reaches −0.4 V, the QD energy levels are shifted above the Fermi level, so the stored electrons are completely transferred to the channel. The charging and discharging operation of our device is thus completely electrically controllable and does not require any light illumination, which is in contrast with the recent experiment by Koike et al. 12,13 in which light illumination was required for discharge because of thick high barrier material between the channel and the InAs QD layer. When we increased the gate voltage scan range up to 1.2 V, a reverse loop was obtained, as shown in the inset of Fig. 2(a) and it was similar to the one observed by Yusa and Sakaki. 5 The magnitude of the reverse current within the reverse loop was higher than the forward current, and the reason for this higher magnitude could be due to the charging and immediate discharging of electrons from the excited states, probably from the d levels of the InAs QDs.

We investigated the temperature dependency of our device by scanning the gate voltage forth and back at different temperatures. Figure 3(b) shows the temperature dependence on ∆V_{th}. There was a downward trend from an initial ∆V_{th} of 165 mV at 20 K to zero at 200 K. Thermal-energy-assisted excitation and removal of trapped electrons 10 are the reasons for this downward trend. Recently, Balacco et al. 11 have noticed room-temperature memory operation in a similar device and attributed the same to deep levels associated with InAs QDs. In our case, absence of such high-temperature operation is an indication that there are no deep levels in our device. Similar kind of InAs QD devices, free from deep levels have been prepared and reported elsewhere. 12,13 Figure 3(b) also shows the position of the discharged state (V_{D_{th}})
the channel under the gate, \( d_1 \) is the distance from the gate to the dot, and \( d_2 \) is the distance from the dot to the channel. Therefore, to estimate the total capacitance of our device, the number of dots buried under the gate (50 dots as observed from SEM analysis of uncapped wire samples), the channel dimension and top capping thickness (70 nm) should be known. In the present device structure, the top wire dimension under the gate (200 x 1000 nm) was considered as the channel dimension. Further, assuming that the number of electrons in each QD is equal to six, two \( s \) and four \( p \) shell electrons of an InAs QD, we calculate the total capacitance of our device as

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\Delta V_{\text{th}} = 147 \text{ mV}
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The calculated value is comparable to the experimentally obtained value of 165 mV at 20 K, indicating that around 300 electrons were responsible for memory operation at this temperature. A similar calculation at 180 K resulted in a value of 24 mV, with a single electron per QD, and this was also comparable with the experimental variance of 29 mV. We therefore attribute this high-temperature \( \Delta V_{\text{th}} \) value to the single electron charging effect.

In conclusion, we have successfully fabricated a one-dimensional GaAs channel-coupled InAs quantum dot memory device by SA-MOVPE and demonstrated the existence of memory up to 180 K. We used a natural width reduction mechanism associated with the self-limited growth mechanism of SA-MOVPE to define narrow channels and then grew a few InAs QDs on the top of the channel to realize a memory device involving few electrons (around 300 at 20 and 180 K, respectively). Further investigation is now underway to fabricate an InAs quantum dot memory device with even more reduced dimensions to realize single dot single electron memory that can operate at room temperature.

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