

## PAPER

# Low-Power Dynamic MIMO Detection for a $4 \times 4$ MIMO-OFDM Receiver

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**SUMMARY** This paper describes low-power dynamic multiple-input and multiple-output (MIMO) detection for a  $4 \times 4$  MIMO-orthogonal frequency-division multiplexing (MIMO-OFDM) receiver. MIMO-OFDM systems achieve high-speed and large capacity communications. However, they impose high computational cost in MIMO detection when separating spatially multiplexed signals and they consume vast amounts of power. We propose low-power dynamic MIMO detection that controls detection speed according to wireless environments. The power consumption is reduced by dynamic voltage and frequency scaling (DVFS) that controls the operating voltage and clock frequency in the MIMO detector. We implemented dynamic MIMO detection in a pipelined minimum mean square error (MMSE) MIMO detector that we developed in our previous work. A power saving of 92% was achieved under lowest clock frequency mode conditions.

**key words:** wireless communications, MIMO detection, low power, DVFS

## 1. Introduction

Orthogonal frequency division multiplexing with multiple-input and multiple-output (MIMO-OFDM) is a powerful tool in enhancing communication capacities or reliance and has widely been adopted in current wireless communication systems. The standardization group of IEEE802.11 wireless LAN groups has released the IEEE 802.11n specifications [1] that are based on MIMO-OFDM technology.

MIMO detection is important in MIMO-OFDM systems and needs to calculate the weight matrix in each OFDM subcarrier from the estimates of MIMO channels. This process needs numerous matrix multiplications and inverse matrix calculations, which increase the processing time, circuit area, and power consumption. The algorithms for MIMO detection are divided into linear [2], [3] and non-linear detection, such as ordered successive interference cancellations (OSIC)[4], [5] and maximum-likelihood (ML) detection [6], [7]. There are trade-offs between MIMO detection and computational complexity.

Since OFDM detects MIMO channel properties on the basis of each subcarrier, its computational cost is proportional to the number of subcarriers. A MIMO-OFDM receiver requires considerable throughput even for linear de-

tection. We focused on a hardware implementation of linear detection. We previously presented a complete pipeline MMSE MIMO detector based on Strassen's matrix inversion [8]. This detector can make use of concurrent and pipeline processing and has systematic matrix computation suitable for hardware implementation. The processing time of the complete pipeline detector is 150 times faster than that of other detectors [2], [3] for 512 subcarriers [8]. However, it consumes large amounts of power where the power consumption is 701.2 mW at a 160-MHz clock frequency.

We propose low-power dynamic MIMO detection that controls the detection speed according to wireless environments. Our investigations indicated that the detection speed could be controlled by maintaining communication by using Doppler frequency information. Dynamic MIMO detection adaptively changes the computational time in MIMO detection. Power consumption is reduced by lowering the operating clock frequency and voltage, which is a technique that is known as dynamic voltage and frequency scaling (DVFS) [9], [10]. We found that dynamic MIMO detection provided communication quality equivalent to fixed MIMO detection and reduced power by applying low-speed detection modes. A DVFS FFT/IFFT processor that operates at adequate voltage/frequency under different MIMO configurations has been presented [11] as a DVFS technique in MIMO-OFDM system communications. This DVFS technique only treats the change in MIMO configurations and does not assume variations in wireless environments.

The paper is organized as follows: Sect. 2 explains an algorithm for MIMO detection in MIMO-OFDM systems. Section 3 reviews the designs of MMSE MIMO detectors, which revisits our previous work. The dynamic MIMO detection we propose that covers both the algorithm and circuit structure is presented in Sect. 4. The results obtained from evaluating communication quality and power consumption are presented in Sect. 5. Section 6 summarizes the paper.

## 2. MIMO Detection Algorithm

A MIMO system that uses multiple antennas on both transmitter and receiver sides can increase communication capacity by multiplexing and separating signals. A received signal vector in a MIMO-OFDM system (i.e., multi-carrier OFDM transmission) is described by

$$\mathbf{y}[k, t] = \mathbf{H}[k]s[k, t] + \mathbf{n}[k, t], \quad (1)$$

where  $k$  indicates a subcarrier index,  $t$  indicates a data sym-

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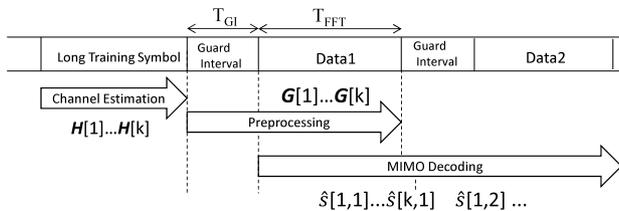


Fig. 1 Timing chart for MIMO detection.

bol index, and  $s[k, t]$  denotes a transmitted signal vector at the  $t$ -th symbol. Here,  $\mathbf{n}$  stands for a white Gaussian noise vector and  $\mathbf{H}[k]$  with an  $M_R \times M_T$  matrix indicates a MIMO channel where  $M_R$  and  $M_T$  are the numbers of receiving and transmitting antennas. Weight matrix  $\mathbf{G}[k]$  by using the minimum mean square error (MMSE) criterion is computed as

$$\mathbf{G}[k] = (\mathbf{H}[k]^H \mathbf{H}[k] + \sigma^2 \mathbf{I})^{-1} \mathbf{H}[k]^H \quad (2)$$

where  $(\cdot)^H$  denotes the complex conjugate transpose and  $\sigma^2$  indicates noise variance. The computation in Eq. (2) is called “preprocessing”. A decoded signal vector,  $\hat{\mathbf{s}}[k, t]$ , is given by multiplying the weight matrix with the received signal vector as

$$\hat{\mathbf{s}}[k, t] = \mathbf{G}[k] \mathbf{y}[k, t]. \quad (3)$$

There is a timing chart for MIMO detection in Fig. 1. A MIMO detector starts computing MIMO channel matrices for all subcarriers when it receives the last training symbol. Preprocessing can be executed after each MIMO channel matrix is computed. Since the data symbols follow the training symbols in packet mode OFDM, the detector should complete preprocessing before it receives the data symbols. Otherwise, the detector leads to unacceptable processing delay. We consider acceptable latency time to be the sum of FFT duration  $T_{\text{FFT}}$  and GI length  $T_{\text{GI}}$  as a measure of real-time processing. For instance, the IEEE802.11n PHY frame has parameters of  $N=108$ ,  $T_{\text{FFT}}=3.2 \mu\text{s}$ , and  $T_{\text{GI}}=0.8 \mu\text{s}$ , where  $N$  is the number of data subcarriers. The acceptable latency time for preprocessing becomes  $4 \mu\text{s}$ .

### 3. Design of MMSE MIMO Detector

The circuit structure for the pipeline MMSE MIMO detector presented in Yoshizawa et al. [8] is briefly explained here. The pipeline MIMO detector is based on Strassen’s matrix inversion [12]. Strassen’s algorithm for matrix inversion divides a square matrix into four block matrices. It is divided into  $2 \times 2$  block matrices for a  $4 \times 4$  matrix  $\mathbf{\Omega}$  as

$$\mathbf{\Omega} = \begin{pmatrix} \mathbf{A} & \mathbf{B} \\ \mathbf{C} & \mathbf{D} \end{pmatrix}, \quad (4)$$

where  $\mathbf{A}$ ,  $\mathbf{B}$ ,  $\mathbf{C}$ , and  $\mathbf{D}$  are the  $2 \times 2$  matrices.  $\mathbf{\Omega}^{-1}$  is calculated with Strassen’s algorithm:

$$\mathbf{\Omega}^{-1} = \begin{pmatrix} \mathbf{F} & -\mathbf{A}^{-1} \mathbf{B} \mathbf{E}^{-1} \\ -\mathbf{E}^{-1} \mathbf{C} \mathbf{A}^{-1} & \mathbf{E}^{-1} \end{pmatrix}$$

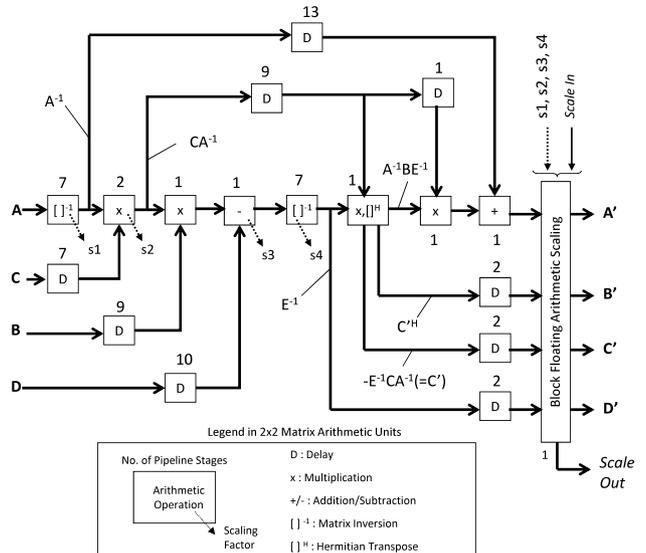


Fig. 2 Circuit structure for 4×4 matrix inversion.

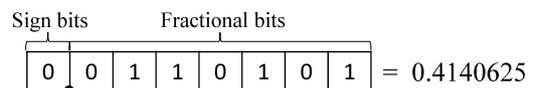


Fig. 3 Fixed point format.

$$= \begin{pmatrix} \mathbf{A}' & \mathbf{B}' \\ \mathbf{C}' & \mathbf{D}' \end{pmatrix} \quad (5)$$

$$\mathbf{F} = \mathbf{A}^{-1} + \mathbf{A}^{-1} \mathbf{B} \mathbf{E}^{-1} \mathbf{C} \mathbf{A}^{-1} \quad (6)$$

$$\mathbf{E} = \mathbf{D} - \mathbf{C} \mathbf{A}^{-1} \mathbf{B}. \quad (7)$$

This algorithm reduces computational complexity by reusing the intermediate results of  $\mathbf{E}^{-1}$ ,  $\mathbf{A}^{-1}$ , and  $\mathbf{C} \mathbf{A}^{-1}$ . Since the MMSE criterion in Eq. (2) gives  $\mathbf{\Omega} = \mathbf{H}^H \mathbf{H} + \sigma^2 \mathbf{I}$ , it becomes a Hermitian matrix composed of  $\mathbf{C} = \mathbf{B}^H$  and  $\mathbf{B}' = \mathbf{C}^H$ . This property gives the relation of  $\mathbf{A}^{-1} \mathbf{B} = (\mathbf{C} \mathbf{A}^{-1})^H$  and further reduces complexity by reusing these intermediate results.

The circuit structure of  $4 \times 4$  matrix inversion is outlined in Fig. 2. The main stages (from  $\mathbf{A}$  to  $\mathbf{A}'$ ) are used to compute the submatrices of  $\mathbf{E}^{-1}$  and  $\mathbf{F}$  and produce the other submatrices of  $\mathbf{A}^{-1}$ ,  $\mathbf{C} \mathbf{A}^{-1}$ , and  $\mathbf{E}^{-1} \mathbf{C} \mathbf{A}^{-1}$ . The  $2 \times 2$  matrix arithmetic units with internal pipeline stages have been implemented in fixed point arithmetic. The fixed point format in Fig. 3 consists of a sign bit and fractional bits without integer bits. This representation can avoid overflows in addition and subtraction if the absolute values of arithmetic inputs are not more than  $1/2$ . Moreover, the absolute values of arithmetic inputs need to be close to  $1/2$  to decrease rounding errors in the fractional bits. The block floating adjusts a maximum value for  $2 \times 2$  matrix  $\mathbf{\Omega}$  to satisfy  $1/4 \leq \max |\Omega_{ij}| < 1/2$ . The block floating scaling factors of  $s_1$ ,  $s_2$ ,  $s_3$ , and  $s_4$  are introduced in the  $2 \times 2$  matrix multiplication and inversion units. We apply direct computation to  $2 \times 2$  matrix inversion in the submatrices using

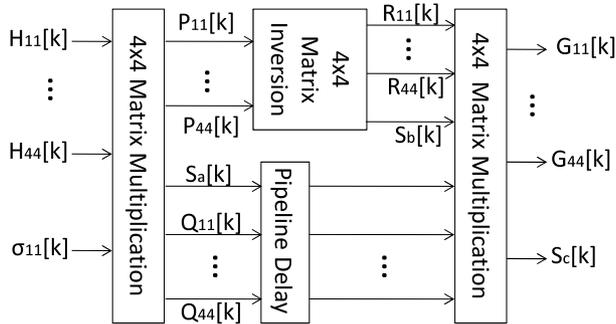


Fig. 4 Structure of circuit for pipeline MMSE MIMO detector.

Table 1 Performance of circuit for pipeline MMSE MIMO detector.

Operation Frequency	160 MHz
Logic Gate Count	2,203,300
Pipeline Latency	187.5 ns
Power Consumption	701.2 mW

$$\omega^{-1} = \begin{pmatrix} a & b \\ c & d \end{pmatrix}^{-1} = \frac{1}{ad - bc} \begin{pmatrix} d & -b \\ -c & a \end{pmatrix}. \quad (8)$$

The circuit structure of the pipeline MMSE MIMO detector is outlined in Fig. 4. The inputs of  $H_{11}[k]$  to  $H_{44}[k]$  are elements of channel matrix  $\mathbf{H}[k]$ , and  $\sigma^2$  is variance in the noise vector. The outputs of each block are computed by

$$\mathbf{P}[k] = \mathbf{H}[k]^* \mathbf{H}[k]^T + \sigma^2 \mathbf{I} \quad (9)$$

$$\mathbf{Q}[k] = \mathbf{H}[k]^* \quad (10)$$

$$\mathbf{R}[k] = \mathbf{P}^{-1}[k] \quad (11)$$

$$\mathbf{G}[k] = \mathbf{R}[k] \mathbf{Q}[k], \quad (12)$$

where  $S_a[k]$ ,  $S_b[k]$ , and  $S_c[k]$  are scaling factors to avoid an overflow. The pipeline delay unit adjusts computation timings for  $\mathbf{H}[k]$  to meet data of  $\mathbf{R}[k]$ .

The performance of the circuit for the pipeline MMSE MIMO detector is summarized in Table 1. The MIMO detector was implemented by using a 90-nm CMOS standard library. The power consumption value was measured under conditions of a 1.0-V voltage supply and a 160-MHz clock speed. The implemented results indicated a satisfactory pipeline latency of 187.5 ns, which is less than the acceptable latency time of 4  $\mu$ s (mentioned in Sect. 2). It required a large amount of power of 701.2 mW. Since the MIMO detector used about 40% of the power consumption in the 4 $\times$ 4 MIMO-OFDM receiver circuit according to our previous work [13], the low-power technique of MIMO detection has a strong impact on the hardware implementation of MIMO-OFDM systems.

## 4. Dynamic MIMO Detection

### 4.1 MIMO Channel Variations

The timing chart in Fig. 1 indicates severe processing latency for real-time processing in a MIMO detector. The pipeline MMSE MIMO detector has been designed to meet

Table 2 Simulation parameters.

Modulation Type	16QAM
Signal Bandwidth	40 MHz
FFT Size	128
No. of Data Subcarriers	108
FFT Length	3.2 $\mu$ s
Guard Interval Duration	0.8 $\mu$ s
Packet Length	500 Bytes
Channel Model	Multipath Rayleigh Fading
MIMO Spatial Correlation	i.i.d.
Symbol Timing	Ideal
Channel Estimation	Calculation at Training Symbols
Maximum Doppler Frequency	2, 6, 10, 14, 18 Hz
Error Correcting	Convolution Coding (R=3/4) Soft-Decision Viterbi Decoding

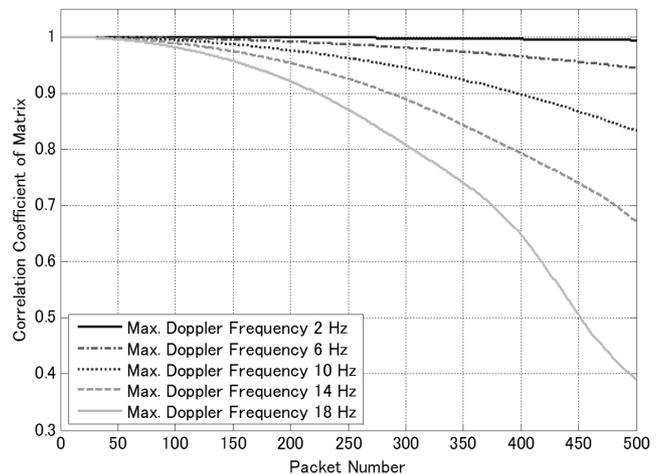


Fig. 5 Snapshot example of channel variations under maximum Doppler frequency conditions from 2 to 18 Hz.

latency requirements that assume that a MIMO detector operates under the worst conditions when wireless channel propagation characteristics vary for all MIMO-OFDM packets, i.e., fast fading environments. However, the other conditions (i.e., better conditions in slow fading environments) could be considered in actual wireless systems.

We investigated time variations in MIMO channel coefficients by measuring the two-dimensional correlation coefficients of the MIMO channel matrices in first and other packets under various conditions with maximum Doppler frequencies. The simulation parameters are enumerated in Table 2, which assumes a packet based MIMO-OFDM system in the IEEE 802.11n standard. There is a snapshot example of the correlation coefficients in Fig. 5. The horizontal axis represents the number of packets. The low Doppler frequency condition of 2 Hz maintains almost the same correlation coefficients across several hundreds of packets. This phenomenon indicates that the channel matrix does not change across several hundreds of packets under slow fading conditions.

The MIMO channel variations are also considered in the frequency domain for MIMO-OFDM systems. The frequency-domain linear interpolation of MIMO channels as a mean of minimizing the computational complexity of ma-

trix inversion has been presented [14]. However, the method of interpolation needs the channel environment to be flat fading to considerably reduce complexity. Low Doppler frequency conditions would be more acceptable than flat fading conditions for wireless LAN systems.

4.2 Proposed Method

Slow fading conditions do not impose severe timing constraints on computing Eq. (2) because the channel matrix of  $\mathbf{H}$  changes slowly. The latency requirement in Fig. 1 could be loosened under slow fading conditions. We discuss dynamic MIMO detection that adaptively changes the computation time of Eq. (2) and the time intervals to update the weight matrix of  $\mathbf{G}$ . There is a timing chart for static MIMO detection treated as a conventional detector in Fig. 6. Static MIMO detection computes the period of  $T_{FFT}+T_{GI}$  for each packet. The weight matrix of  $\mathbf{G}^q$  ( $q$  is an updated index) is updated within the same packet. The dynamic MIMO detection we propose has two types of detection modes, i.e., short and long detection delay modes, whose timing charts are in Figs. 7(a) and 7(b). The short detection delay mode extends the computation time to  $T_P$ .  $T_P$  denotes the packet length consisting of training symbols and data symbols. This extension means that the weight matrix is updated when the next packet is received. The number of waiting packets  $N_w$  controls the frequency with which the weight matrix is updated. As the number of  $N_w$  increases, the number of computations of the weight matrix is decreased. The long detection delay mode further extends the computation time by  $N_w \cdot T_P$ . The timing to update the weight matrix is delayed

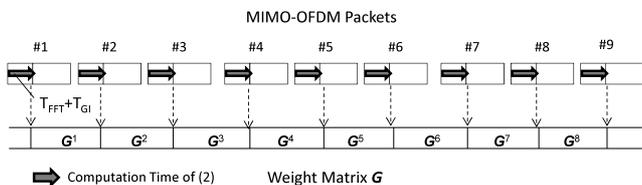


Fig. 6 Static MIMO detection.

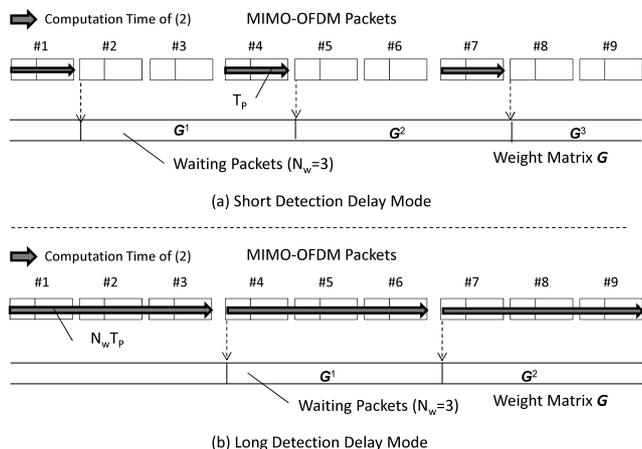
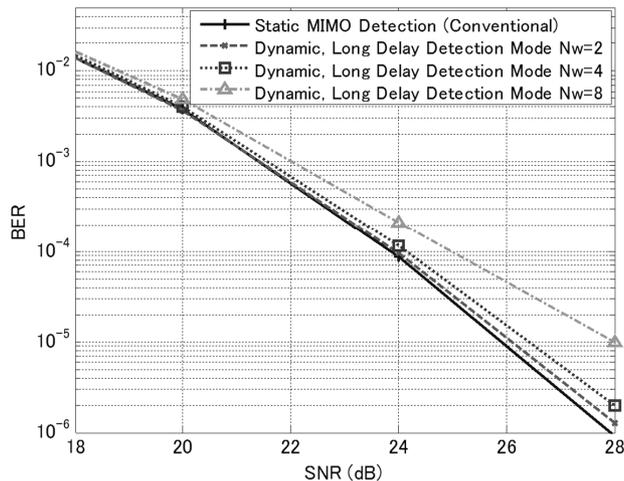


Fig. 7 Proposed dynamic MIMO detection.

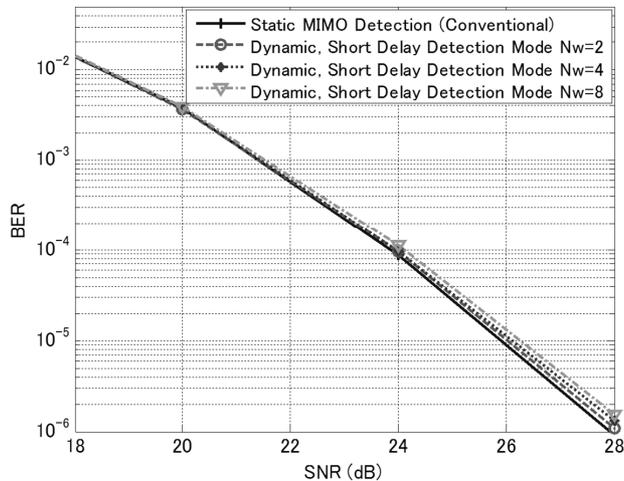
by  $N_w - 1$  packets overall, compared with the short detection delay mode. The long detection delay mode is more sensitive to channel variations in fading environments due to this delay.

Dynamic MIMO detection was evaluated by using bit error rate (BER) to assess performance. The graph in Fig. 8 compares static MIMO detection with the proposed method when applying the numbers of waiting packets  $N_w$ . We used the same simulation parameters as those in Table 2 and a maximum Doppler frequency of 10 Hz. When the acceptable degradation was set to less than 1 dB in SNR for BER of  $10^{-4}$ , the conditions of  $N_w=2, 4$ , and 8 provided enough performance in communication in the short detection delay mode. The long delay detection mode limited the numbers of  $N_w$  to 2 and 4.

We applied the least squares (LS) method that extracts the channel matrix by adding and subtracting the long training symbols to estimating the MIMO channels. The long training symbols were defined by orthogonal space-time patterns. LS channel estimation is used in IEEE802.11n



(a) Static MIMO detection vs dynamic MIMO detection with long delay mode.



(b) Static MIMO detection vs dynamic MIMO detection with short delay mode.

Fig. 8 BER at maximum Doppler frequency of 10 Hz.

MIMO-OFDM systems [15]. The channels are estimated only once to update the weight matrix. The performance of BER would be improved by using appropriate extrapolation based on past channel matrices, especially in the long delay detection mode. The power increase in this case by introducing channel matrix extrapolation and the decrease by increasing the number of waiting packets  $N_w$  should be compared.

### 4.3 Circuit Structure

The circuit structure for dynamic MIMO detection is in Fig. 9. A phase locked loop (PLL) supplies a clock and a DC/DC converter supplies an operating voltage. Their speed and magnitude are changed by information from the DVFS control unit. The DVFS control unit adjusts the MIMO detection speed associated with the number of waiting packets  $N_w$ . When the MIMO detection speed is decreased, the MIMO detector operates at a low clock frequency and under low operating voltage conditions, which is based on the DVFS technique [9]. The power consumption model in CMOS circuits can be expressed as

$$Power = C_L V_{DD}^2 f + (A - 1) I_0 e^{\frac{-V_T}{\alpha V_{th}}} V_{DD}, \quad (13)$$

where  $C_L$  is capacitance,  $V_{DD}$  is the operating voltage, and  $f$  is the operating frequency. Here,  $A$  is the number of gates,  $I_0$  is the leakage current,  $V_T$  is the threshold voltage, and  $\alpha$  is a parameter of subthreshold swing. The first term indicates dynamic power. The second term is leakage power caused by leakage current. From Eq. (13), dynamic power is proportional to the square of the operating voltage, and leakage power is proportional to the operating voltage. The power consumed in CMOS circuits by both dynamic and leakage power is reduced by decreasing the power voltage. It is clear that a lower supply voltage can significantly reduce power consumption. However, lowering the supply voltage imposes a penalty of increasing circuit delay expressed by

$$\gamma = C_L \frac{V_{dd}}{K_d (V_{dd} - V_T)^\delta}, \quad (14)$$

where  $K_d$  is a drivability factor and  $\delta$  is an empirical constant value depending on CMOS technology [16]. This delay is associated with a decrease in clock frequency given by  $1/\gamma$ .

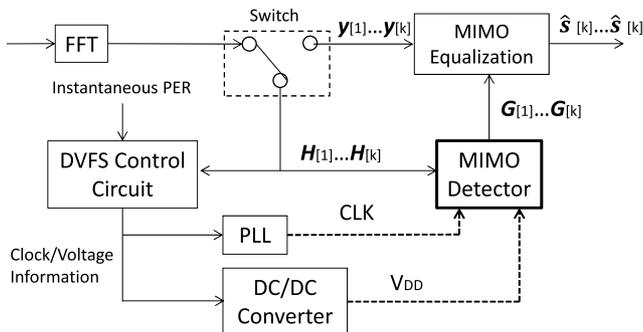


Fig. 9 Circuit structure for dynamic MIMO detection.

Therefore, DVFS has a trade-off between power reduction and clock speed in the MIMO detector.

## 5. Evaluation

We treated a simplified example on the length of  $T_P$  and the number of waiting packets  $N_w$  to evaluate power reduction with the dynamic MIMO detection we propose. We assume  $T_P = 5(T_{FFT} + T_{GI})$ , i.e.,  $20 \mu s$ , which indicates that the packet length is given by four training symbols and one data symbol. As the number of data symbols in a packet decreases, the timing constraints for MIMO detection are more severe. We have summarized the results for selected numbers in our simulation in Table 3 for the parameters of  $N_w$ . The results indicate that the long detection mode requires a smaller value for  $N_w$  due to the delay in updating the weight matrix of  $G^q$ .

The power consumption results for static (conventional) and dynamic (proposed) MIMO detection are listed in Table 4. Each acceptable clock period in dynamic MIMO detection can be calculated by scaling the computation time in static MIMO detection. Since delay  $\gamma$  in Eq. (14) corresponds to the clock period, the value of  $V_{dd}$  can be determined. The dynamic and leakage power are computed from Eq. (13). The results for power and energy consumption for the number of waiting packets  $N_w$  and the short and long detection delay modes are summarized in Table 5. Compared with static MIMO detection, the long detection delay mode achieved a power saving of 92% under the condition of  $N_w = 16$ . The long delay detection mode provided lower power consumption than that of the short delay detection mode by decreasing the operating voltage. The short delay detection mode, on the other hand, was superior to the long delay detection mode in terms of total energy consumption. Note that leakage power became dominant under lower operating frequency conditions because leakage power was not proportional to the magnitude of clock frequency. The longer computation time in the long delay detection mode would increase energy consumption due to leakage power.

Table 3 Numbers of waiting packets under maximum Doppler frequency conditions.

Number of Waiting Packets ( $N_w$ )	Maximum Doppler Frequency (Hz)			
	2	10	20	40
Short Detection Delay Mode	16	16	4	1
Long Detection Delay Mode	16	4	1	1

Table 4 Power consumption by static and dynamic MIMO detectors.

MIMO Detection Type	Computation Time	Clock Frequency (MHz)	Operating Voltage (V)	Power Consumption (mW)		
				Dynamic	Leakage	Total
Static	$T_{FFT} + T_{GI}$	40	1	123.57	38.41	161.98
Dynamic (Proposed)	$T_P$	8	0.58	8.40	22.28	30.68
	$4T_P$	2	0.37	0.86	14.21	15.07
	$16T_P$	0.5	0.33	0.17	12.68	12.85

**Table 5** Summary of power and energy consumption results.

MIMO Detection Type	Number of Waiting Packets ( $N_w$ )	Computation Time	Total Computation Time for 1000 Packets ( $\mu s$ )	Power (mW)	Total Energy ( $\mu J$ )
Static	0	$T_{FFT}+T_{GI}$	$1000 \cdot (T_{FFT}+T_{GI})$	161.98	647.9
Dynamic Short Detection Delay Mode	1	$T_p$	$1000 \cdot T_p$	30.68	613.6
	4		$1000/4 \cdot T_p$		153.4
	16		$1000/16 \cdot T_p$		38.4
Dynamic Long Detection Delay Mode	1	$T_p$	$1000 \cdot T_p$	30.68	613.6
	4	$4T_p$	$1000/4 \cdot 4T_p$	14.21	301.4
	16	$16T_p$	$1000/16 \cdot 16T_p$	12.68	257.0

## 6. Conclusion

We presented dynamic MIMO detection to reduce power consumption in a  $4 \times 4$  MIMO-OFDM receiver. Dynamic MIMO detection controlled computation time in MIMO detection according to time-varying conditions of Doppler frequency. Power consumption was reduced with the DVFS technique, which dynamically changed the clock frequency and operating voltage. Dynamic MIMO detection reduced power consumption to 1/14 and energy consumption to 1/17 in our evaluations.

The dynamic MIMO detection we proposed assumes that the value for Doppler frequency is known. However, estimating low Doppler frequencies as dozens of hertz required long-term observations of several seconds for received signals. It was not practical to directly estimate Doppler frequency in terms of real-time processing. A scheme of adaptive control to determine appropriate numbers of waiting packets  $N_w$  would be more effective for time-varying wireless environments and will be discussed in future work.

## References

- [1] "IEEE P802.11n/D4.00: Draft amendment to wireless LAN media access control (MAC) and physical layer (PHY) specifications: Enhancements for higher throughput," March 2008.
- [2] A. Burg, S. Haene, D. Perels, P. Luethi, N. Felber, and W. Fichtner, "Algorithm and VLSI architecture for linear MMSE detection in MIMO-OFDM systems," IEEE International Symposium on Circuits and Systems (ISCAS), pp.4102–4105, May 2006.
- [3] J. Eilert, D. Wu, and D. Liu, "Efficient complex matrix inversion for MIMO software defined radio," IEEE International Symposium on Circuits and Systems (ISCAS), pp.2610–2613, May 2007.
- [4] Z. Khan, T. Arslan, J.S. Thompson, and A.T. Erdogan, "Area and power efficient VLSI architecture for computing pseudo inverse of channel matrix in a MIMO wireless system," Proc. 19th International Conference on VLSI Design (VLSID), pp.734–737, Jan. 2006.
- [5] D. Perels, S. Haene, P. Luethi, A. Burg, N. Felber, W. Fichtner, and H. Bolcskei, "ASIC implementation of a MIMO-OFDM transceiver for 192 Mbps WLANs," 31st European Solid-State Circuits Conference (ESSCIRC), pp.2152–218, Sept. 2005.
- [6] S. Chen, T. Zhang, and M. Goel, "Relaxed tree search MIMO signal detection algorithm design and VLSI implementation," IEEE International Symposium on Circuits and Systems (ISCAS), pp.1147–1150, May 2006.

- [7] B. Mennenga, E. Matus, and G. Fettweis, "Vectorization of the sphere detection algorithm," IEEE International Symposium on Circuits and Systems (ISCAS), pp.2806–2809, May 2009.
- [8] S. Yoshizawa, Y. Yamauchi, and Y. Miyanaga, "VLSI implementation of a complete pipeline MMSE detector for a  $4 \times 4$  MIMO-OFDM receiver," IEICE Trans. Fundamentals, vol.E91-A no.7, pp.1757–1762, July 2008.
- [9] A.P. Chandrakasan, V. Gutnik, and T. Xanthopoulos, "Data driven signal processing: An approach for energy efficient computing," International Symposium on Low Power Electronics and Design (ISLPED), pp.347–352, Aug. 1996.
- [10] W.W. Shi, C.S. Choy, J.P. Guo, C.F. Chan, K.N. Leung, and K.P. Pun, "A 90 nm RFID tag's baseband processor with novel PIE decoder and uplink clock generator," IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), pp.644–647, Aug. 2010.
- [11] Y. Chen, Y.-W. Lin, Y.-C. Tsao, and C.-Y. Lee, "A 2.4-Gsample/s DVFS FFT processor for MIMO OFDM communication systems," IEEE J. Solid-State Circuits, vol.43, no.5, pp.1260–1273, May 2008.
- [12] S.M. Balle and P.C. Hansen, "A Strassen type matrix inversion algorithm," IOS Press, Advances in Parallel Algorithms, pp.22–30, 1994.
- [13] S. Yoshizawa and Y. Miyanaga, "VLSI implementation of a  $4 \times 4$  MIMO-OFDM transceiver with an 80-MHz channel bandwidth," IEEE International Symposium on Circuits and Systems (ISCAS), pp.1743–1746, May 2009.
- [14] J. Wang and B. Daneshrad, "Performance of linear interpolation-based MIMO detection for MIMO-OFDM systems," Wireless Communications and Networking Conference (WCNC), vol.2, pp.981–986, March 2004.
- [15] R.V. Nee, V.K. Jones, G. Awater, A.V. Zelst, J. Gardner, and G. Steele, "The 802.11n MIMO-OFDM standard for wireless LAN and beyond," Wireless Pers. Commun., vol.37, pp.445–453, 2006.
- [16] D. Sengupta and R. Saleh, "Power-delay metrics revisited for 90 nm CMOS technology," IEEE International Symposium on Quality of Electronic Design (ISQED), pp.291–296, March 2005.



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