A Single Electron Binary-Decision-Diagram Quantum Logic Circuit Based on Schottky Wrap Gate Control of a GaAs Nanowire Hexagon

Seiya Kasai and Hideki Hasegawa, *Member, IEEE*

***Abstract*—A novel hexagonal binary-decision-diagram (BDD) quantum logic circuit approach for III-V quantum large scale integrated circuits is proposed and its basic feasibility is demonstrated. In this approach, a III-V hexagonal nanowire network is controlled by Schottky wrap gates (WPGs) to implement BDD logic architecture by path switching. A novel single electron BDD OR logic circuit is successfully fabricated on a GaAs nanowire hexagon and correct circuit operation has been confirmed from 1.5 K to 120 K, showing that the WPG BDD circuit can operate over a wide temperature range by trading off between the power-delay product and the operation temperature.**

***Index Terms*—Binary decision diagram (BDD), GaAs, logic circuit, Schottky wrap gate (WPG), single electron.**

I. Introduction

QUANTUM nanodevices may play important roles in future information technology and multidisciplinary nanotechnology. This is because nanoscale dissipative quantum switches such as single electron transistors provide opportunities to realize Boolean logic circuits at smallest possible power-delay product (PDP) values near the quantum limit [1] with high circuit densities beyond limits of silicon roadmap devices [2]. In the far future, nanotechnology may even realize nondissipative quantum circuits such as in [3] where quantum coherence, extending over entire circuit operation, realizes massively parallel and highly sophisticated quantum computation/processing.

In reality, however, there exists, at present, no realistic approach even for dissipative quantum circuits. This is because quantum devices are weak and sensitive and not suited to conventional Boolean logic gate architectures which require robust devices. For example, GaAs single electron (SE) logic inverter circuits we demonstrated [4], were poor in transfer gain (max 1.3), current drivability, threshold voltage control and output/input voltage matching.

To overcome this difficulty, this Letter proposes a novel hexagonal binary-decision-diagram (BDD) quantum logic circuit approach for III-V quantum large-scale integrated circuits and demonstrates its feasibility through fabrication of a simple SE integrated circuit based on Schottky wrap gate control of a GaAs etched nanowire hexagon.

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The authors are with the Research Center for Integrated Quantum Electronics (RCIQE) and Graduate School of Electronics and Information Engineering, Hokkaido University, Sapporo 060-8628, Japan (e-mail: kasai@rciqe.hokudai.ac.jp).

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II. Concept of Hexagonal BDD Quantum Logic Circuits

The BDD logic architecture was originally proposed by Akers [5]. Its hardware implementation in Si CMOS LSIs was investigated by Yano *et al.* [6]. Single electron BDD circuits were simulated on computer by Asahi *et al.* [7]. Recently, we have successfully fabricated a GaAs SE BDD node device [8] and suggested use of hexagonal nanowire networks [9], [10].

As shown in Fig. 1(a), the novel hexagonal BDD circuit consists of a wired array of gated quantum BDD node devices formed on a hexagonal closely packed planar nanowire network. Ungated portions of the network serve as interconnects and thus unnecessary branches are cut out. Each node device has one entry- and two exit-branches. Depending on gate input x_i, it selects, through gate control of quantum transport, one of exit-branches for the incoming information messenger which is either a single electron or a few electrons. The value of the logic function, r_i, is determined by checking whether the root terminal, r_i, is connected to terminal-1 or to terminal-0.

Any combinational logic function can be implemented as BDD circuits [6]. As basic examples, hexagonal BDD implementations of AND, OR, and XOR logic functions are shown in Fig. 1(b). Full adders, multipliers and other standard circuit blocks can be formed using multihexagon layouts. For a large logic system including feedback, the system is divided into fairly large BDD combinational logic blocks. Then, root outputs of each block are put into a buffer register circuit consisting of quantum wire transistors, MESFETs, HEMTs or HBTs for 0,1 detection, possible amplification, voltage level shifting and timing control. Then, outputs of the register are put into gates of another BDD block and so on. This allows a logic system design at register transfer level using a suitable BDD logic partition theory.

Since this approach requires no direct output-to-input cascade connection, none of large voltage gain, precise input-output voltage matching, large fan-in and fan-out numbers and large current drivability are required. A hexagonal structure promises high-density integration. Smaller device counts in BDD circuits than in logic gate circuits [6] also help dense integration. Furthermore, node devices are interconnected by nanowires without source/drain contacts and this avoids the serious contact problem in ULSIs. Absence

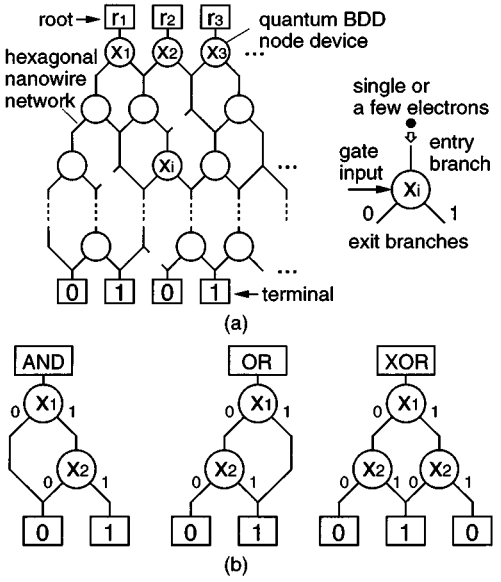

Fig. 1. (a) Hexagonal BDD quantum circuits integrating node devices in the inset. (b) Hexagonal BDD layouts of AND, OR, and XOR logic functions.

of output-to-input cascade interconnections, use of ungated nanowires as interconnects as well as regular circuit layouts reduce numbers of interconnection metallization levels and average interconnection lengths.

III. Fabrication and Characterization of Single Electron BDD Circuits

For SE transport, a pair of tunneling barriers attached to a quantum dot (QD) is required. As shown in Fig. 2(a), two types of SE BDD node devices using Schottky wrap gates (WPGs) were fabricated on AlGaAs/GaAs etched nanowires with electron beam lithography. In the node-switch type device, the gate on the entry-branch and the gate on the exit-branch selected for SE transport form a pair of tunneling barriers with a QD at the node and the gate on the other exit-branch is biased to block SE transport. In the branch-switch type device, switching of SE transport takes place by a pair of gates formed on each exit-branch. In both devices, the WPG voltage, V_g, not only controls tunneling barrier profiles, but also the dot potential. Our WPGs [4], [8] produce much sharper potential profiles than previous split gates [11] due to field lines coming from top and sides. An example of conductance oscillation from a branch-switch is shown in Fig. 2(b). The behavior is similar to Si MOS SETs [12]. Unlike metal SETs, semiconductor SE devices are truly quantum devices with artificial atom features [13] due to long Fermi wavelengths. Indeed, analysis of temperature dependences of heights and widths of conductance peaks confirmed SE transport through lateral resonant tunneling [14]. Both node devices showed sharp path switching by applying complementary gate inputs, as reported elsewhere [8].

To investigate integration feasibility, a two-variable-input BDD OR logic circuit was fabricated on an etched GaAs hexagon shown in Fig. 3(a) with its graph. Here, a node-switch device at node x_1 and a branch-switch at x_2 are integrated to realize OR function. 0-branch at x_2 and terminal-0 were omitted, since one terminal suffices for logic value determination. Another branch switch on 1-branch at x_1 is a dummy used for circuit test.

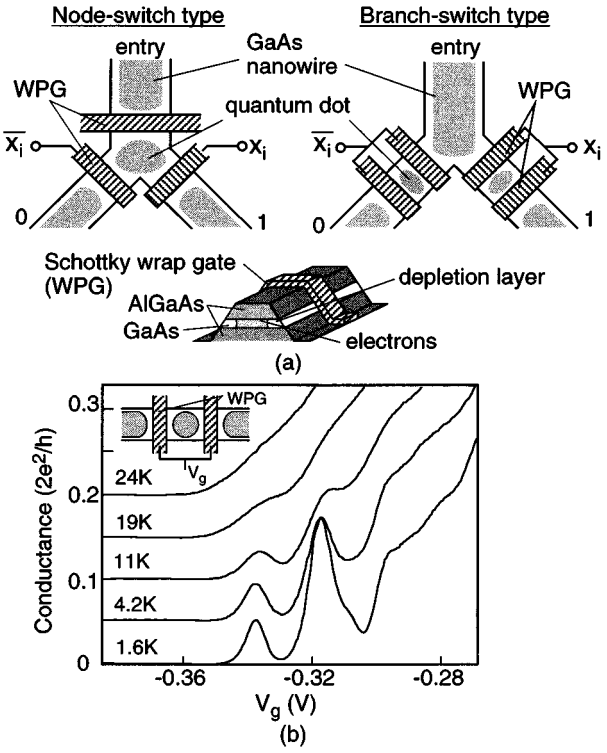

Fig. 2. (a) Two types of WPG single electron BDD node devices: a node-switch type (left) and a branch-switch type (right) and a basic structure of the WPG (bottom). (b) Conductance oscillation characteristics in a branch-switch type single electron device having 30 nm Cr/Au WPGs.

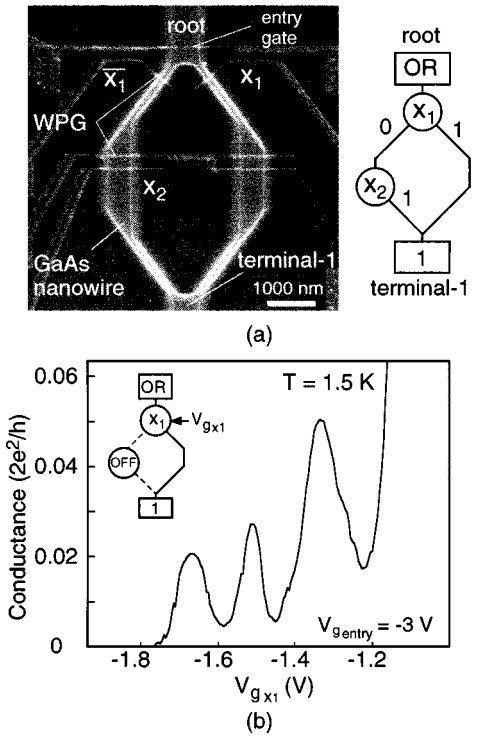

Fig. 3. (a) SEM image of a single electron BDD OR logic circuit on a GaAs hexagon and (b) conductance oscillation waveform from a branch of the WPG BDD node device.

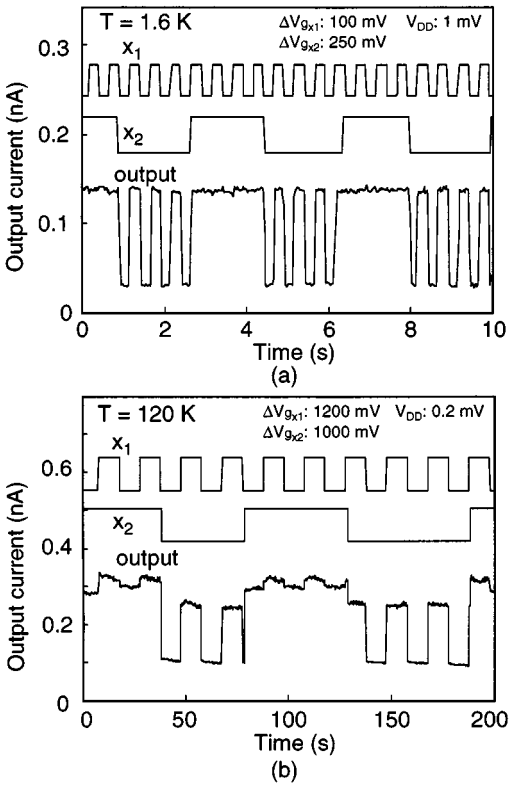

Fig. 4. Input/output waveforms of the WPG BDD OR logic circuit at (a) 1.6 K and (b) 120 K.

The fabricated circuit showed proper SE transport behavior as shown in Fig. 3(b). Its logic operation was investigated by carefully adjusting dc bias for two devices to cause path switching at the first conductance peak. The input-output waveforms by low-frequency logic test at 1.6 K are shown in Fig. 4(a). Correct OR logic operation was obtained in the SE regime. This is the first demonstration of a SE BDD circuit.

The circuit gave correct outputs at least up to 120 K by bias adjustments and gate swing increase as shown in Fig. 4(b). This is because operation changes with temperature from the SE quantum regime, to a few electron quantum regime and finally to the many electron classical regime. Thus, BDD circuits operate over a wide temperature range by trading off between PDP and temperature.

IV. Prospects of Speed-Power Performance and High Density Integration

Direct circuit speed measurements were difficult because pulse measuring equipments available today have too large input capacitances for measuring the high-speed operation of single-electron circuits with minute capacitances. A simple estimate was made as follows. The total capacitance C was 70 aF from the charging energy (2.3 meV) determined by Coulomb diamonds. The ratio, A, of tunneling conductance to the quantum conductance $G_0(=2e^2/h)$ was 0.01. According to [1], delay time τ and power P of a SET switch can be roughly estimated by $\tau = C/(AG_0)$ and $P = e^2/(2C\tau)$, which gave $\tau = 1$ ns and $P = 2 \times 10^{-13}$ W at 1.5 K. The resultant PDP of 2×10^{-22} J is near to the quantum limit [1]. In the future, if quantum-limit operation is realized at room temperature, PDP value is increased to about 10^{-20} J due to thermal energy limitation [1]. These two values are much smaller than those of advanced Si devices at 300 K. For example, 100 nm Si CMOS transistors typically give PDP values in the range of 10^{-16} J. Latest 20 nm/30 nm Si CMOS transistors gave record PDP values in the range of 10^{-17} J [15].

To realize dense SE circuits operating at room temperature, dense hexagonal networks of nanowires with wire widths below 10 nm are required. We are making intensive efforts to realize such III-V networks using selective MBE [16]. The present approach is also applicable to silicon-on-insulator (SOI) structures and to molecular nanowire networks including carbon nanotubes where dense hexagonal arrays were recently formed [17].

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