Growth Dynamics and Applications of Selectively–Grown InGaAs Nanowires

（有機金属気相選択成長法による InGaAs ナノワイヤの
成長ダイナミクスと素子応用に関する研究）

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by

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Dedicated to my parents,

Etsuko KOHASHI and Hiromichi KOHASHI

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Chapter 1

Background and Motivation

1.1 General Introduction

The field for semiconductor nanotechnology represents an exciting and rapidly expanding research area including the physical, material, life, and engineering science. Among them, the electronics based on the scaling in silicon complementary–metal–oxide–semiconductor (Si–CMOS) technology has been successfully progressed and has offered today's fast information processing, developments of science, and expanding business field. The progress in such technology continues to overcome a lot of difficulties of the resolution limits and improve the integration level which is usually expressed as Moore's Law (that is, the number of components per chip of integrated circuit (IC) doubles roughly every 24 months) [1].

Meanwhile, some issues simultaneously arise. First one is a material or physical issue. Cost of the use of silicon (Si) is relatively low and the quality of single crystal Si is extremely high (purity is ~99.999999999%). However, their mobility of electrons and holes is relatively low (electron mobility: 1400 $cm^2V^{-1}s^{-1}$, hole mobility: 450 $cm^2V^{-1}s^{-1}$ [2] at room temperature) as compared to those of the other materials, such as III–V compound semiconductors (e.g., electron mobility of InAs: 40000 $cm^2V^{-1}s^{-1}$, hole mobility of InSb: 850 $cm^2V^{-1}s^{-1}$ [2]) and so on. In addition, Si has an indirect band gap, and this fact hinder the light emission from Si.

Second one is scientific issue regarding the optical wavelength of lithography and/or process–induced structural damages. Third one is the scaling issue. Scaled MOS field–effect transistors (FETs) have serious issues originated from the short–channel effects, and these issues result in some problems, such as the increase of the power consumption and calorific power.

For overcoming the first issue described above, the other materials having high carrier mobility and/or direct band gap are really required, such as the germanium (Ge), carbon (C), gallium arsenide (GaAs), indium phosphide (InP), zinc oxide (ZnO), and so on. Among them, III–V compound semiconductors (e.g., GaAs, InP, InAs…) have superior material properties for electric and photonic applications, and we study on this kind of semiconductors.

To overcome the second and third issues, self–assembled nanostructures are now intensively investigating. In general, there are two philosophically distinct approaches for creating small structures, which can be characterized as top–down and bottom–up. In the top–down approach, small structures are made from bulk materials by a combination of lithography and etching techniques. Current Si–CMOS technology is one of the top–down approaches in nanotechnology, however, such approaches have some issues as we mentioned above.

On the other hand, the bottom–up approach, in which functional structures are assembled from chemically synthesized, well–defined nano–scale building blocks, and represents a powerful alternative approach to conventional top–down methods. Compared to etching–based top–down methods for fabrication, the bottom–up method based on crystal growth is a counter approach to fabricating nanostructures without any concern for damages during the fabrication. The bottom–up approach has the potential to go far beyond of the limits of top–down technology, and will enable entirely new device concepts and functional systems, and thereby create technologies that we have not yet imaged. For instance, FETs using semiconductor nanowires, which is one of the self–assembled nanostructures [3][4], can suppress the short channel effects and are expected that it contribute to further development of electronics.

This thesis gives the details of research on the synthesis of III–V compound semiconductor nanowires and their device applications. In particular, those of indium gallium arsenide (InGaAs) nanowires were intensively investigated. In this chapter, we describe the general introduction of this study. Specifically, the overviews of the III–V compound semiconductors nanowires (III–V compounds, InGaAs, semiconductor nanowires) are briefly described. Finally, we explain the motivation and outline of the research described in this thesis.

1.2 III–V Compound Semiconductor Nanowires

1.2.1 III–V Compound Semiconductors

For long periods, silicon (Si, group–IV element shown in **Figure 1–1**) has been the dominant material, mainly due to the high quality silicon dioxide (SiO_2), which is very good insulator that can be thermally formed on Si. In addition, Si in the form of silica and silicates is the most abundant minerals in the earth's crust, which makes Si very cheap in comparison to the other alternatives. However, many compound semiconductors that consist of two or more elements, such as III–V materials (e.g., GaAs, InGaN) and II–VI materials (e.g. ZnO), have unique electrical and optical properties that are absent in Si.

Among them, this thesis focuses on and deals with the III–V compound semiconductors. The III–V compound semiconductors, such as GaAs, AlAs, InAs, InP, their ternary, and quaternary alloys, are composed of group–III and group–V elements shown in **Figure 1–1**. Firstly formed artificial crystal of III–V compound semiconductor is InP in 1910. After that, toward 1950, formation of various kinds of III–V materials, such as InSb, GaSb, GaAs, GaP, AlAs, AlP, and AlN, and their physical properties has been reported. Then, in the wake of that H. Welker *et al*. pointed out the importance of these materials in 1952 [6], III–V compound semiconductors has come to be noted as promising semiconducting material for electrical and optical device applications [7]–[9].

II	III	IV	V	VI
	Boron 5 B	Carbon 6 C	Nitrogen 7 N	Oxygen 8 O
	Aluminum 13 Al	Silicon 14 Si	Phosphorus 15 P	Sulfur 16 S
Zinc 30 Zn	Gallium 31 Ga	Germanium 32 Ge	Arsenic 33 As	Selenium 34 Se
Cadmium 48 Cd	Indium 49 In	Tin 50 Sn	Antimony 51 Sb	Tellurium 52 Te

Figure 1–1

A part of the periodic table. Gray regions represent the set of III and V elements.

Group	Material	Crystal Structure	Lattice Constant (Å)		Linear Thermal Expansion Coefficient (10^{-6}/K)	Carrier Mobility ($cm^2V^{-1}s^{-1}$)	
			a	c		Electron	Hole
IV	Si	D	5.4309	–	2.4	1400	450
	Ge	D	5.6575	–	5.5	3900	1900
III–V	GaAs	ZB	5.6533	–	6.0	8500	400
	InAs	ZB	6.0583	–	5.19	40000	500
	AlAs	ZB	5.6611	–	5.20	180	
	GaP	ZB	5.4495	–	5.3 ~ 5.81	250	150
	InP	ZB	5.8687	–	4.5	5400	200
	AlP	ZB	5.4625	–		80	
	GaN	WZ	3.189	5.186	5.59 (a), 3.17 (c)	1000	200
	InN	WZ	3.533	5.693			
	AlN	WZ	3.112	4.982	4.03 ~ 6.09	300	14
	GaSb	ZB	6.094	–	6.7	3000	1000
	InSb	ZB	6.478	–	5.04	77000	850
	AlSb	ZB	6.136	–	4.88	200	420
II–VI	CdTe	ZB	4.681	–		1200	100
		WZ	4.57	7.47			

Table 1–1

Physical properties of IV, III–V, and II–VI semiconductors at 300 K. “D”, “ZB”, and “WZ” represent the crystal structure of diamond, zincblende, and wurtzite, respectively. “a” and “c” for lattice constant represent a–axis and c–axis, respectively. The values of lattice constant, linear thermal expansion coefficient and carrier mobility are quoted from Refs. [2] and [5].

Table 1–1 shows physical properties of III–V compounds. It is known that almost III–V materials exhibit zincblende (ZB) crystal structure in bulk, except for some group–III nitrides (e.g., GaN). In general, these III–V compounds are chemically synthesized as epitaxial thin films on planar crystal substrate (e.g, GaAs and InP) by the crystal growth techniques, such as metal–organic vapor–phase epitaxy [10] (MOVPE, details are described in **Chapter 3**). In such techniques, the difference in lattice constant, thermal expansion coefficient, and polarity between grown crystal and substrate is important for obtaining high quality single crystals. For example, the growth of InAs or GaAs thin films on InP and/or Si substrate is very difficult.

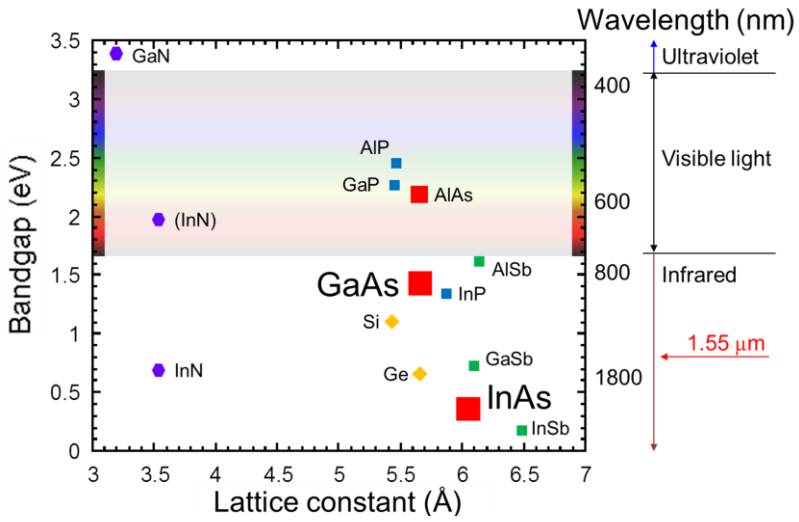

Figure 1–2

Band gaps of the group IV and III–V binary semiconductors plotted as function of the lattice constant. Closed diamonds, closed square, and closed hexagons represent the crystal structure of each material, that is, diamond, zincblende, and wurtzite, respectively. [2][5]

Unique electrical and optical properties of III–V compounds absented in Si have been generating much research interests. Some III–V compounds have higher carrier mobility than that of Si, which make it promising material for application to high–speed and high–frequency electronics. For instance, in InGaAs or InAs, the electron mobility is more than 10 times higher than that in Si as shown in **Table 1–1**. In recent years, III–V compounds have been considered as a leading candidate to replace the Si channel in MOSFETs. Their future role has recently been recognized in the "International Technology Roadmap for Semiconductors (ITRS)" [1].

As for the optical properties, many III–V materials, including GaAs, InAs, and InP, have direct band gap. This means that electrons and holes can directly combine while conserving momentum, and such process results in the emission of photons. In addition, the values of their band gap cover the wide range of light wavelength (**Figure 1–2**) including ultraviolet, visible, and infrared light. Moreover, these III–V materials can form their ternary and quaternary alloys, such as $In_{1-x}Ga_xAs$, $In_{1-x}Ga_xN$, $In_{1-x}Ga_xAs_yP_{1-y}$, and the physical properties, such as band gap and lattice constant, can continuously be changed depending on their alloy composition, x and/or y. These unique features of III–V compounds make these

materials interesting for optical applications, such as lasers, light–emitting diodes (LEDs) and also photo detectors. For instance, InGaAsP–related materials and group–III nitrides cover the infrared optical–communication band (wavelength: $\lambda \approx 1.3$ μm [11], and 1.55 μm [12]) and/or visible range, and their properties and applications have intensively been investigated [13]–[17].

Another notable feature of III–V compounds is that they can form various kinds of heterostructures (**Figure 1–3**), such as GaAs/AlGaAs and (In)GaN/AlGaN [13]–[22]. By using such structures with doping techniques, high–mobility and high–efficiency electrical/optical devices can be achieved due to the two–dimensional (2D) electron gas and carrier confinement.

Aforementioned unique features of III–V compounds have driven the studies on their synthesis and applications. Among the III–V materials, we focus on InGaAs (indium gallium arsenide) in this thesis, and more detailed informations about it are described in next section.

1.2.2 Indium Gallium Arsenide

Indium gallium arsenide (InGaAs) is the ternary alloy and is consisted of two group–III elements (gallium, Ga and indium, In) and one group–V element (arsenic, As). The physical properties of GaAs, InAs, and $In_{1-x}Ga_xAs$ in bulk are shown in **Table 1–2**. The properties of $In_{0.53}Ga_{0.47}As$ are also shown, because the $In_{0.53}Ga_{0.47}As$ lattice–matches with InP, and their properties have intensively been studied [23]–[26]. Their crystal structure is zincblende (ZB) and these have direct band gap. In addition, the physical properties of $In_{1-x}Ga_xAs$ represent intermediate properties between GaAs and InAs, and continuously vary with changing their

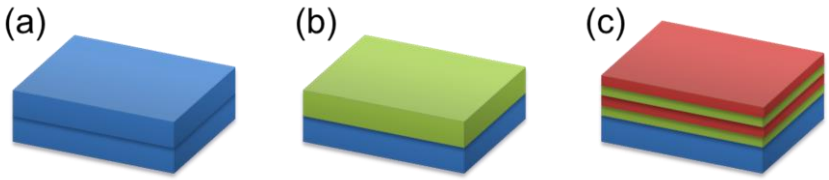

Figure 1–3
Various kinds of heterojunctions. (a) Homojunction, (b) Heterojunction, (c) Multi–heterojunction. Different color regions represent different materials (e.g., Blue: InP, Green: InGaAsP, and Red: InGaAs)

alloy composition, x (**Table 1–2**). For instance, the lattice constant of $In_{1-x}Ga_xAs$ is simply given by "$5.6533x + 6.0583(1-x)$" (Vegard's law). The other physical properties, such as the band gap, effective masses, and dielectric constant, can also be modulated by composition engineering, and we can choice its appropriate value, except for the thin film growth in large lattice–mismatched systems (e.g., $In_{0.53}Ga_{0.47}As$ does not grow on GaAs with high crystal quality).

	GaAs	**InAs**	**$In_{0.53}Ga_{0.47}As$**	**$In_{1-x}Ga_xAs$**
Crystal Structure	ZB	ZB	ZB	ZB
Lattice Constant (Å)	5.6533	6.0583	5.8687	$5.6533x + 6.0583(1-x)$
Band Gap (eV)	1.424	0.354	0.74	$0.35 + 0.60\,x + 0.475x^2$
Band Structure	Direct	Direct	Direct	Direct
Dielectric Constant (static)	12.9	15.15	13.9	$15.1 - 2.87x + 0.67x^2$
Dielectric Constant (high frequency)	10.89	12.3	11.6	$12.3 - 1.4x$
Infrared Refractive Index, n	3.3	3.51	3.43	$3.51 - 0.16x$
Effective Electron Mass, m_e	$0.063\,m_0$	$0.023\,m_0$	$0.041\,m_0$	$(0.023 + 0.037x + 0.003x^2)\,m_0$
Effective Hole Masses, m_h	$0.51\,m_0$	$0.41\,m_0$	$0.45\,m_0$	$(0.41 + 0.1x)\,m_0$
Effective Hole Masses, m_{lp}	$0.082\,m_0$	$0.026\,m_0$	$0.052\,m_0$	$(0.026 + 0.056x)\,m_0$
Electron Mobility ($cm^2\,V^{-1}s^{-1}$)	8500	40000	12000	
Hole Mobility ($cm^2\,V^{-1}s^{-1}$)	400	500	300	
Breakdown Field (V/cm)	$\approx 4 \times 10^5$	$\approx 4 \times 10^4$	$\approx 2 \times 10^5$	
Melting Point (˚C)	1238	942		~ 1000

Table 1–2

Physical properties of GaAs, InAs, and $In_{1-x}Ga_xAs$ at 300 K. "ZB" represent the crystal structure of zincblende. "Direct" means direct transition. The datas are quoted from Refs. [2], [5], and [27].

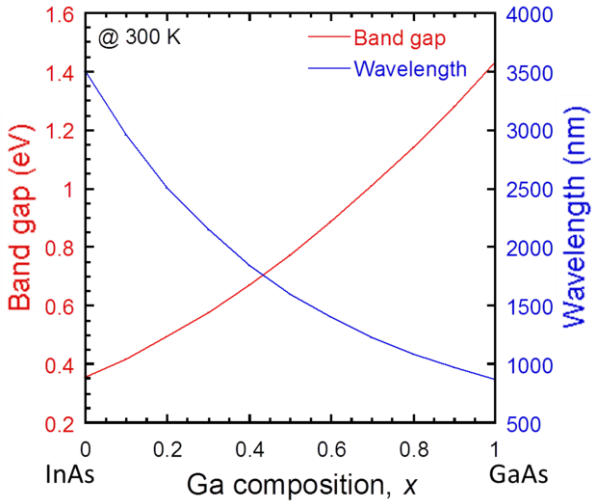

Figure 1–4

Band gap and corresponding emission/absorption wavelength versus gallium composition, x, of $In_{1-x}Ga_xAs$ [27]. (x = 1: GaAs, x = 0: InAs)

More specifically, for instance, the composition–dependent band gap of $In_{1-x}Ga_xAs$ and corresponding light wavelength can be plotted as shown in **Figure 1–4** [27]. The band gap of $In_{1-x}Ga_xAs$ varies from 1.42 eV (GaAs) to 0.35 eV (InAs) while remaining direct band gap, and it covers optical–fiber communication bands (e.g., Original–band (O–band): 1260–1360 nm, and Conventional–band (C–band): 1530–1565 nm). In addition, the strong absorption lines of many molecules are located in this wavelength range. Specifically, carbon dioxide (CO_2), nitrous oxide (N_2O), and carbon monoxide (CO) have absorption lines at wavelengths around 2.05, 2.13, and 2.33 μm, respectively [28]. Moreover, InGaAs has larger band gap than that of InAs, and higher electron mobility than that of GaAs. Importance of InGaAs–related materials and their heterostructures can be seen from its variety of applications utilizing their unique properties. For example, $In_{1-x}Ga_xAs$ can be applied to field–effect transistors (FETs) [29][30], lasers for optical–fiber communication [13][15] or for molecular spectroscopy and trace–gas sensing [28][31][32], infrared photo detectors including avalanche photo diodes (APDs) [33]–[35], and multi–junction solar cells [36][37]. Among them, we focused on the FET application of InGaAs in this thesis as described in **Chapter 8**, and we thus give more detailed information about application of InGaAs to FETs, and would like to clarify the significance of our research.

InGaAs–Based Planar Field–Effect Transistors

Metal–insulator–semiconductor field–effect transistors (MISFETs) have been widely used as important components in large scale integration (LSI) systems. They have many attractive advantages, i.e., self–isolation, low power consumption, and normally–off mode. However, current LSI technology based on silicon (Si) faces critical issues as we described in **Section 1.1**. One of the approaches for realizing high–speed MISFETs is use of the other material which has a high mobility, such as III–V compound semiconductors.

The III–V compound semiconductor channel MISFETs have firstly been reported by H. Becke *et al*. in 1965, where they demonstrated *n*–channel depletion–type GaAs MISFETs with chemically deposited SiO_2 or Si_3N_4 films, which exhibited a power gain up to 10dB at 100 MHz [38]. After that, however, the III–V MISFETs having inversion–type channel have not been realized for a decade. This seems attributable to high density of surface states and high density of bulk traps. In 1974, T. Ito and Y. Sakai have reported the inversion–type GaAs MISFETs by improving fabrication process of MISFETs [39], where the stability of MIS structures was remarkably improved by using the chemically vapor deposited double layer films of Al_2O_3 and SiO_2. This structure had relatively low density of interface states and FETs exhibited an effective mobility of 2240 $cm^2V^{-1}s^{-1}$.

More recently, $In_{1-x}Ga_xAs$ has attracted much attentions as an alternative fast channel to replace Si for future *n*–type MISFETs, because its electron mobility is higher than that of bulk Si and GaAs [40]. Various kinds of insulators, such as Al_2O_3 and HfO_2, have been attempted for gate–dielectric of InGaAs MISFETs [41][42].

The advantage of InGaAs as a transistor channel is originated not only from its high electron mobility, but also from its band gap and interface properties. Although the electron mobility of InAs is much higher than that of InGaAs, the band gap of InGaAs is twice larger than that of InAs (**Table 1–2**). Since the band gap of InAs is only 0.35 eV, both thermal generation and band–to–band tunneling can be major sources of leakage current in FETs [43]. On the other hand, InGaAs has a larger band gap, which may reduce the leakage current and allow higher temperature operation.

In addition, the Schottky barrier height at the insulator–InGaAs interface can be adjusted by changing their alloy composition as shown in **Figure 1–5(a)** [44][45]. This feature gives MISFETs the efficient gate controllability. For example, the performance of $In_{0.65}Ga_{0.35}As$ MISFETs, such as the drain current and transconductance, is better than that of $In_{0.53}Ga_{0.47}As$ MISFETs and much better than that of $In_{0.20}Ga_{0.80}As$ MISFETs [46]. These results can be explained as follows. Presumably every interface has donor–type and acceptor–type interface traps [47]. A convenient notation is to interpret the sum of these by the distribution of interface trapping state density, D_{it}, with an energy level called charge neutrality level, E_{CNL}. If Fermi–level, E_F, is above E_{CNL}, the states are of acceptor–type and negatively charged if the states are occupied. If E_F is below E_{CNL}, the states are of donor–type and positively charged if the states

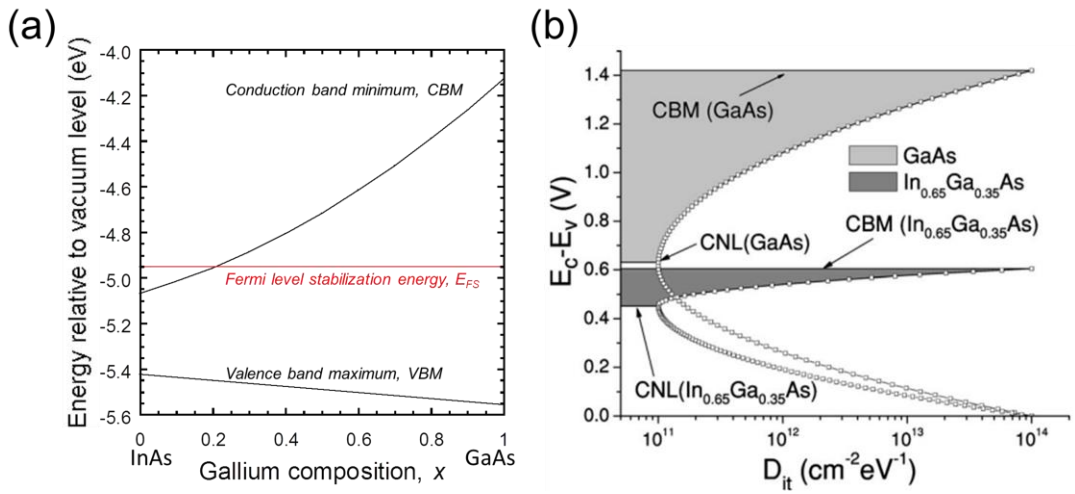

Figure 1–5

(a) Conduction band, valence band, and Fermi level stabilization energy, relative to vacuum level, as a function of composition in $In_{1-x}Ga_xAs$ alloys [44][45]. The composition dependence of the fundamental band gap at room temperature is taken from Ref. [27]. (b) Schematic for the parabolic interface trapping state density, D_{it}, distribution within energy band of GaAs and $In_{0.65}Ga_{0.35}As$ [46]. The charge neutrality level (CNL) is aligned 0.8 eV below conduction band minimum (CBM) for GaAs and 0.15 eV below CBM for $In_{0.65}Ga_{0.35}As$. The shadow area shows the built–up negative charges in interface traps after Fermi–level moves from CNL to CBM. The model is extremely simplified to highlight the fundamental point by assuming D_{it} distribution is parabolic in logarithm scale and D_{it} value at CBM and valence band maximum is fixed at 10^{14} $cm^{-2}eV^{-1}$. E_C–E_V represents the band gap.

are occupied. Assuming that Fermi–level stabilization energy, E_{FS}, shown in **Figure 1–5(a)** is located at E_{CNL} and the strong electron inversion occurs when E_F reaches conduction band minimum (CBM), the farther the E_{CNL} locates from CBM, the more negative trapped charges are built in when the E_F sweeps to CBM, the more difficult it is to realize a large amount of inversion charges to participate the transport. The traps not only reduce the mobile inversion charges, but also prevent further surface potential bending due to the Coulomb repulsion. The amount of acceptor–type interface traps from CNL to CBM should be less for $In_{0.65}Ga_{0.35}As$ than $In_{0.53}Ga_{0.47}As$, and much less for $In_{0.20}Ga_{0.80}As$ or GaAs, as illustrated in **Figure 1–5(b)**, and this results in the higher performance of $In_{1-x}Ga_xAs$ MISFETs when the value of x is relatively low.

InGaAs–based FETs have exhibited further development in recent years. For instance, $In_{0.7}Ga_{0.3}As$ MISFETs with maximum effective channel mobility of 4402 $cm^2V^{-1}s^{-1}$ using InP barrier layer [48], the inversion–type enhancement–mode $In_{0.65}Ga_{0.35}As$ MISFETs with maximum drain current exceeding 1 A/mm [29], inversion–type $In_{0.53}Ga_{0.47}As$ MIS high–electron–mobility transistors (HEMTs) on Si substrate with maximum drain current exceeding 2 A/mm [49], and enhancement–mode $In_{0.7}Ga_{0.3}As$ pseudomorphic HEMTs (PHEMTs) with maximum oscillation frequency, f_{max}, in excess of 1 THz [30], have been reported.

We also focus on the superior properties of InGaAs suitable for FET applications [50][51], and studied the fabrication of InGaAs nanowire–based MISFETs as described in **Chapter 8**. The semiconductor nanowires (NWs) have distinctive electrical and optical properties originated from their unique geometry and synthetic process. In next section, we briefly introduce the NWs from the point of view of the wide range of nanotechnology.

1.2.3 Semiconductor Nanowires

This thesis describes the synthesis and device applications of III–V semiconductor nanowires (NWs), in particular, those of indium gallium arsenide (InGaAs) NWs are intensively studied. The detailed informations of NW–synthesize, its history, and advantages and applications of NWs are given in **Chapter 2**. Thus, we describe the general introduction of the NWs as a nanostructure in the wide range of nanoscience and nanotechnology in this section.

Nanostructures

Intrinsic physical properties of bulk materials (e.g., **Table 1–1**) are certainly the key factors for realizing various kinds of devices. However, their "size" and "geometry" are also significantly important factors not only for achieving high–performance devices, but also for creating novel properties, principles, and functional devices, and these should be noted. It has been understood that the sufficient reduction of the number of atoms in a structure can have dramatic implications for its properties. The reduction in size of crystalline structures will ultimately mean that the characteristic properties of individual atoms, normally negligible in bulk, begin to increase in importance. Size effects become important when at least one dimensional of a crystal is reduced to the order of hundreds of atoms the length scale of nanometers (**Figure 1–6(b)**). The unique properties of nanostructures can be roughly divided into two primary categories surface–related effects and quantum confinement effects.

Surface–Related Effects

Bonding structure of surface atoms of a material is different from that of atoms below the surface, and atoms at the material surface may have a different chemical environment of oxide or hydrogen termination forms. These atoms will thus behave somewhat differently from other atoms in a crystal. In bulk materials, the proportion of surface atoms to bulk atoms is entirely negligible, and processes that take place at the surface of a material are usually of little consequence to the behavior of the material as a whole. However, the surface–to–volume ratio of a nanoscale structure is considerably high enough that surface effects often cannot be ignored. As well, the structure of the solid state can change somewhat to accommodate the high proportion of surface atoms, ultimately decreasing the stability of the crystal.

Quantum Confinement Effects

Quantum effects occur when the wavelength of an electron in a material is of the same order as a dimension of the material. This limits the motion of an electron in the material, which becomes quantized in than confining dimension.

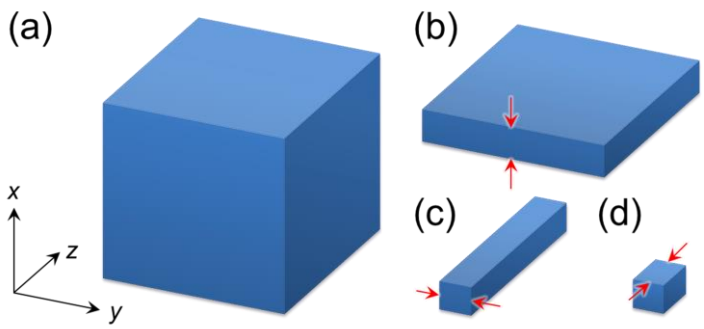

Figure 1–6

Schematic illustrations of (a) bulk, (b) quantum well, (c) quantum wire, (d) quantum dot.

Low–Dimensional Structures

The density of states of the electrons is determined by the number of dimensions in with electrons are quantized. Individual molecules and quantum dots (QDs), which can be classified as zero–dimensional (0D) structures (**Figure 1–6(d)**), are attractive building blocks for bottom–up assembly of nanoscale electronics. These 0D structures have been intensively investigated over the past decade [52], since they represent the smallest building blocks with corresponding high potential for integration [53][54]. However, as for the use of such 0D structures integrated systems, it has been difficult to develop and demonstrate realistic schemes for integration of 0D devices into functional architectures.

One–Dimensional Structures

One–dimensional (1D) structures (**Figure 1–6(c)**) have also been the focus of extensive studies worldwide due to their unique physical properties, and potential to revolutionize broad areas of nanotechnology. Two classes of materials, carbon nanotubes (CNTs) [55] and semiconductor nanowires (NWs) [62], have shown as 1D nanostructures.

CNTs can exhibit either metallic or semiconducting behavior depending on diameter and helicity [56]. The unique electronic properties of CNTs open up the possibility of creating number of different devices that could have potential in nanoelectronics. For instance, single–

walled CNTs have been used to fabricate field–effect transistors (FETs) [57], diodes [58], and logic circuits [59]. However, it is difficult to make well controlled whether semiconducting or metallic CNTs for specific device functions. Hence, we should make efforts for addressing a serious issue for CNT–based approach to be practical for highly integrated electronics systems.

Semiconductor Nanowires

Semiconductor nanowires (NWs) represent important and broad class of nanoscale wire–like structure, and have become the focus of intensive research in recent years owing to their unique applications in mesoscopic physics and devices [3][4]. NWs are defined as the structures with two dimensions in the range of tens of nanometers (nm), and the third is much longer and typically in the range of micrometers (μm). Such structures are particularly interesting for electrical and optical device applications. For instance, for electrical applications, they exhibit quantum confinement in two dimensions while the third is relatively unrestricted, which contributes to the increase of carrier mobility [60]. Furthermore, field–effect transistors using NWs can suppress the short channel effects and are expected that it contribute to further development of electronics [61].

In comparison with zero–dimensional (0D) structures, such as semiconductor quantum dots, the advancement of nanowires (1D) has been slow until very recently [62][63], as hindered by the difficulties associated with the synthesis and fabrication of these nanostructures with well–controlled dimensions, morphology, phase purity, and chemical composition. In contrast to

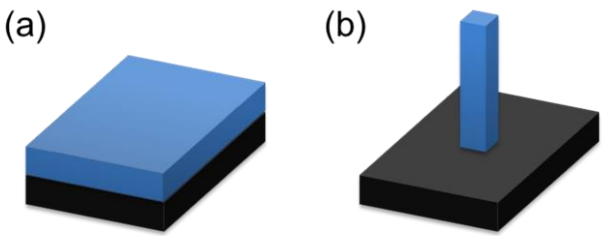

Figure 1–7
Schematic illustrations of epitaxially grown (a) planar semiconductors, and (b) semiconductor nanowires.

CNTs, nanowires can be rationally and predictably synthesized in single crystal form with all key parameters controlled during growth; chemical composition, diameter, length, conduction type, and conductivity. Therefore, nanowires represent one of the best–defined and controlled elements nanoscale building blocks, which correspondingly have enabled a wide range of devices and integration strategies. For example, nanowire applications have been demonstrated, such as nanoscale FETs [64], lasers [65], and logic circuits [66].

1.2.4 III–V Compound Semiconductor Nanowires

Various kinds of semiconductor materials have been formed as the nanowires (NWs), such as group–IV materials (e.g., Si, Ge), III–V materials (e.g., GaAs, InP, GaN, InGaAs), and II–V materials (e.g., ZnO). In particular, epitaxially grown III–V compound semiconductor NWs have recently attracted much research interest, because the III–V NWs have unique features originated from both intrinsic physical properties of III–V compounds (**Section 1.2.1**) and size/geometrical effects of NWs (**Section 1.2.3**). Consequently, III–V NWs (**Figure 1–7(b)**) have great potential to achieve high–performance devices and novel technologies, which are not possible with the conventional planar semiconductors (**Figure 1–7(a)**).

Understanding and development of synthesis techniques of ternary alloy are essentially important issues for realizing future applications based on III–V compound semiconductor NWs. As for the InGaAs NWs, several groups have investigated their growth properties in various kinds of growth techniques [67]–[73]. However, the sufficient understanding and controllability of growth of InGaAs NWs have not been achieved and remained as an active subject of debate, because the growth processes in the synthesis of ternary alloys are generally more complex than that of binaries. Thus, further investigations of InGaAs NW growth is required for obtaining precise controllability of their size, and alloy composition, as well as for the comprehensive understanding of growth dynamics of III–V ternary alloys.

1.3 Motivation

Realization of novel functional and developed devices builds upon many fundamental studies from material science to device mounting. As the knowledge of the unique properties of nanostructures increases, the transition from promising science to practical technology requires further understanding of the function and effects of nanoscale structures. Since the properties and functions of nanostructures are strongly dependent on their size, geometry, and chemical composition, the controllability of their properties are very important for crystal growth.

This thesis deals with the epitaxial growth, characterizations, and applications of III–V compound semiconductor nanowires (NWs) fabricated by selective–area metal–organic vapor–phase epitaxy (SA–MOVPE). In particular, those of InGaAs NWs were intensively investigated.

SA–MOVPE is one of the bottom–up techniques for crystal growth applying the selective–growth technique using partly masked substrate. History, advantages, and procedures of SA–MOVPE are described in **Chapter 2** and **Chapter 3**. Our group has continuously been studying the selective–area growth of III–V compound semiconductor nanowires by using MOVPE since late 1990s. Various kinds of materials, including binary and ternary, and vertical/lateral heterostrctures have been fabricated to characterize crystal structures, atomic composition profiles, and photoluminescence properties with quantum size effects. As for the InGaAs NWs formed by SA–MOVPE, our group has already been reported the growth properties and structural/optical characterizations [69]–[73].

To make efficient use of InGaAs NWs, simultaneous control of NW size (i.e., their height and diameter) and alloy composition is essentially required, because the mole fraction of group–III elements and NW size strongly affect the physical properties of NWs as well as the performance of devices. Simultaneously, for achieving precise control of NW size and alloy composition, deep understanding of their growth dynamics and mechanisms is significantly important. On the other hand, it is known that the growth dynamics of GaAs and InAs NWs formed by SA–MOVPE exhibit some dissimilarity [74][75] in terms of the effects of growth temperature and V/III ratio (**Chapter 4**). This fact suggests that the growth dynamics of In_{1-}

$_x$Ga$_x$As NWs should be dependent on their alloy composition, x. However, the composition–dependent growth dynamics of selectively–grown InGaAs NWs has not been reported.

The core motivation of this thesis is the achievement of simultaneous control of size and alloy composition of InGaAs NWs by clarifying the origin of composition–dependent growth dynamics, and demonstration of NW–based device using InGaAs NWs. We thus firstly investigated the composition–dependent growth dynamics of InGaAs NWs. More specifically, we grew the $In_{1-x}Ga_xAs$ NWs having alloy composition of gallium–rich ($x > 0.5$) and indium–rich ($x < 0.5$), and compared their growth dynamics, in terms of the effects of growth temperature and V/III ratio (**Chapter 5** and **Chapter 6**).

To realize NW–based device applications, such as FETs and single–photon sources, the reduction of NW diameter is particularly important to avoid introducing misfit dislocations in lattice–mismatched systems. In addition, it is necessary to freely control the position of NWs depending on the application. However, previously reported InGaAs NW arrays in SA–MOVPE were limited to NW diameters of larger than 50 nm, and further reduction of the NW diameter is required. Therefore, we investigated the reduction of the diameter of InGaAs NWs to close to 30 nm and control of their pitch in SA–MOVPE (**Chapter 7**).

For understanding the physical properties of NWs, fabrication of the electrical devices is important, because the electronic properties, such as current–voltage (*I–V*), capacitance–voltage (*C–V*), and photo current characteristics offer some informations of material regarding contact resistance, conductivity, surface/interface state density, quantum efficiency, and so on, as well as the device performance. In addition, metal–insulator–semiconductor (MIS) structure is particularly required for field–effect transistor (FET) application to suppress the leakage current for low power consumption. Also, it is worth investigating the interface properties between insulator (I) and semiconductor (S). Our group has already reported the fabrication and characterization of the Schottky–gate metal–semiconductor (MES) FETs using single InGaAs NW [50]. However, the MISFETs have not been demonstrated. Thus, we fabricated and characterized the MISFETs using single InGaAs NWs and improvement of their fabrication process. In particular, we proposed two kinds of fabrication process for FET fabrication, and investigated the effects of these fabrication processes on their electrical properties (**Chapter 8**).

1.4 Outline of This Thesis

This thesis describes a series of experiments aimed at understanding and controlling the growth of $In_{1-x}Ga_xAs$ nanowires (NWs) having any alloy composition ($0<x<1$), and at achieving the high–performance device applications using InGaAs NWs formed by selective–area metal–organic vapor–phase epitaxy (SA–MOVPE). More specifically, composition–dependent growth dynamics, that is, the composition–dependent effects of growth temperature and V/III ratio, of InGaAs NWs in SA–MOVPE were investigated and we proposed two–step growth method for reducing NW diameter to 30–nm–diameter based on the knowledge of composition–dependent growth dynamics. Furthermore, for achieving the high–performance device applications, we fabricated lateral metal–insulator–semiconductor field–effect transistors (MISFETs) and characterized their electrical properties.

This thesis divided into 9 chapters as follows.

Chapter 2 serves as an overview of the research of NW growth and their applications.

In **Chapter 3**, detailed fabrication and characterization techniques of semiconductor NWs are described. First, we describe overview of MOVPE growth including comparison of other growth techniques, MOVPE system, and principle of MOVPE growth process. Second, principles of SA–MOVPE growth are explained. Next, the explanations of ordinary sample preparation for the NW growth in SA–MOVPE are described. Finally, we explain about the characterization techniques that used for observing and imaging of structural information and investigation of optical properties of NWs.

In **Chapter 4**, we review the features of the growth of GaAs, InAs, and InGaAs NWs in SA–MOVPE. First, we describe about the growth of GaAs and InAs NWs. This thesis explains composition–dependent growth dynamics of InGaAs NWs in SA–MOVPE (**Chapter 5** and **Chapter 6**). Because InGaAs is an alloy between GaAs and InAs, the knowledge on the growth properties of selectively–grown GaAs and InAs NWs is especially important to understand the growth dynamics of InGaAs NWs in SA–MOVPE. In particular, effects of

growth temperature and V/III ratio in selective–area growth of GaAs and InAs NWs exhibited some dissimilarity, which is thought to be due to the inherent difference between GaAs and InAs in binding energy, lattice constant, and so on. Finally, we review the growth of InGaAs NWs based on our previous reports. Knowledge obtained from these reports is to be the basis of discussion of this thesis.

In **Chapter 5** and **Chapter 6**, we describe about composition–dependent growth dynamics of selectively–grown InGaAs NWs, and discuss the experimental results in detail. We grew the $In_{1-x}Ga_xAs$ NWs having alloy composition of gallium–rich ($x > 0.5$) and indium–rich ($x < 0.5$), and compared their growth dynamics. As a result, it was found that the dependence on the growth temperature and V/III ratio of NW diameter, NW height, and alloy composition was significantly changed depending on alloy composition of InGaAs. We believe that the knowledge on composition–dependent growth dynamics offers the important guidelines for realizing simultaneous and precise control of NW size and alloy composition.

In **Chapter 7**, we describe the proposed growth method for realizing thin InGaAs NWs independently of the geometry of the mask used for SA–MOVPE. It was found that the nucleation and growth of NWs are strongly dependent on the geometry of the mask for SA–MOVPE, as well as V/III ratio. We discuss the origin of these growth behaviors and clarify the procedure for growing 30–nm–diameter InGaAs NWs independently of the mask pitch (spacing between neighboring NWs).

In **Chapter 8**, we describe about the fabrication and characterization of lateral MISFETs using selectively–grown single InGaAs NWs and improvement of their fabrication process. In particular, we proposed two kinds of fabrication process for NW–MISFET fabrication, and investigated the effects of these fabrication processes on their electrical properties. As a result, we obtained good electrical characteristics and this result indicates that the NW–based FET application is very promising for the building blocks of future nano electronics and photonics.

Summary and conclusions of the present work are shown, and outlook for NW fabrication and their applications are discussed in **Chapter 9**.

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Chapter 2

Semiconductor Nanowires

2.1 Introduction

Research on the synthesis of semiconductor nanowires (NWs) has been begun from over half a century ago, and has become intensive since a quarter–century ago. And now, the synthesis of semiconductor NWs has actively been studied for wide spectrum of materials. Moreover, such low–dimensional nanostructures are not only interesting for fundamental research due to their unique structural and physical properties relative to their bulk counterparts, but also offer great potential for application to future electronic/photonic devices. We review the background of the research on semiconductor NWs, regarding the synthesis, structural and physical properties, and device application of NWs in this section.

2.1.1 Progress in Nanowire Research

In the early 1960s, first demonstration of epitaxial growth of free–standing crystals has been reported by R.S. Wagner and W.C. Ellis [1]. These free–standing NW–like structures were denoted as "Whiskers" at that time. In that work, Wagner and Ellis demonstrated the vapor–liquid–solid (VLS) growth of silicon (Si) whiskers using gold (Au) as a catalyst. A small piece of Au is placed on a Si substrate, and heated up. The Au forms small droplets under injection of $SiCl_4$ and H_2, and they catalyze the growth of Si NW–like structures. Wagner and Ellis explained this phenomenon through the fact that the liquid droplet is a preferred site for deposition from the vapor, which causes the liquid to become supersaturated with Si. The whisker diameter is comparable to the catalyst size. Because nanostructures can be fabricated by using VLS without the lithography techniques, the VLS has become to be popular for those who are interested in growth mechanism, nanostructure physics, and novel functional devices.

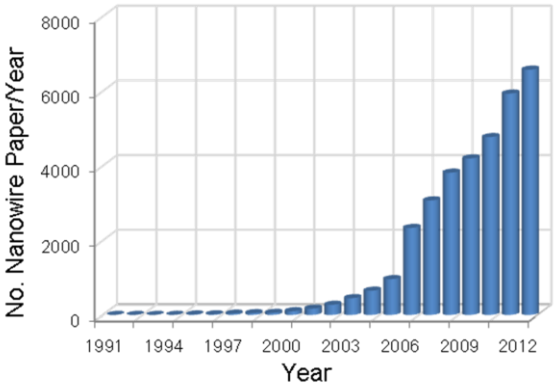

Figure 2–1

Increase in the number of publications on nanowire–related topics from year 1991–2012 (Source, ISI; keyword, nanowires).

In the early 1990s, the growth of III–V nanowhiskers, such as GaAs [2] and InAs [3], using VLS mechanism has been reported by research group of Hitachi, as well as the first demonstration of the *pn* junctions based on heterostructured NWs [4]. Since then, the VLS became exceedingly common as the NW growth method, because this method could synthesize almost all kinds of NWs even oxides and metals with a small size and high quality via a simple procedure. For instance, Harvard University (USA, C.M. Lieber group) [5]–[10], University of California, Berkley (USA, P. Yang group) [11], and Lund University (Sweden, L. Samuelson group) [12][13] showed impactful progresses in the research on VLS–grown NWs around 2000.

On the other hand, Hokkaido University (Japan, T. Fukui group) has been reported an alternative "catalyst–free" NW growth method applying selective–area growth (SAG) technique since late 1990s. Interest in this method has been growing continuously because size– and position–controlled NWs can be grown by SAG without any assists of catalyst. History, advantages, and procedures of SAG of NWs are described in **Section 2.2.2** and **Chapter 3**.

These early works on nanowhiskers were popularized as NWs in the following decade, and become one of the most active research areas within the nanoscience. This can be seen from the vast number of publications on NWs over the past two decade, which has exponentially increased as shown in **Figure 2–1**. Particularly the III–V NWs to be discussed in this thesis have drawn much attention since 2000 with most of the activity and development in the last ten years.

2.1.2 Advantages of Semiconductor Nanowires and their Arrays

Nanowires (NWs) are elongated nanostructures with quite small diameters (several tens to hundreds nanometers (nm)) and relatively long height (it is usually μm–scale). In the other words, they have three–dimensional geometry with high aspect ratio (**Figure 2–2(a)**). Among them, epitaxially grown NWs have unique features and advantages absented in planar semiconductors for achieving novel or developed device applications. Furthermore, NWs can be grown as an array as shown in **Figure 2–2(b)**, and thereby NWs provide additional advantages, which is also key feature of NW technology particularly for the optical device applications. In this section, we describe the features and advantages of semiconductor NWs and their arrays.

2.1.2.1 Advantages of Nanowires

High Aspect Ratio with Small Diameter

The small diameter of NWs allows lateral confinement of carriers that can be used to get electrical and optical properties different from that of the bulk, such as the ballistic transport property in "quantum" wire. Such feature contributes to the increase of carrier mobility, for instance, it was estimated to be 10^6 $cm^2V^{-1}s^{-1}$ for a properly–designed GaAs quantum wire at low temperature [14], and it is suitable for the electronic device applications, such as the field–effect transistors (FETs). For FET applications, another possible benefit of NWs is the vertical geometry, which enables the gate length of vertical transistors (**Figure 2–3(a)**) can be shortened with high precision through the deposit or anisotropic etching of gate–metals. In addition, when the surrounding–gate– electrodes are applied for vertical transistors, it can be suppressed the

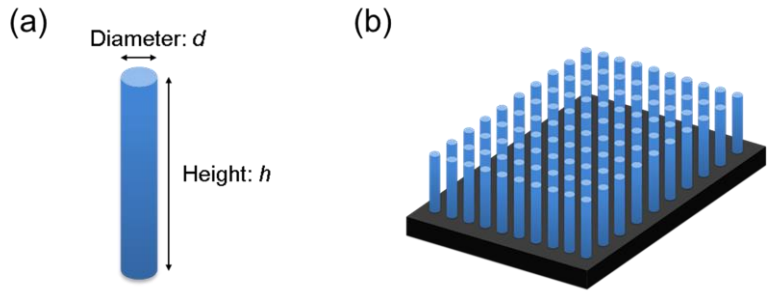

Figure 2–2
Schematic illustrations of (a) nanowire and (b) nanowire array.

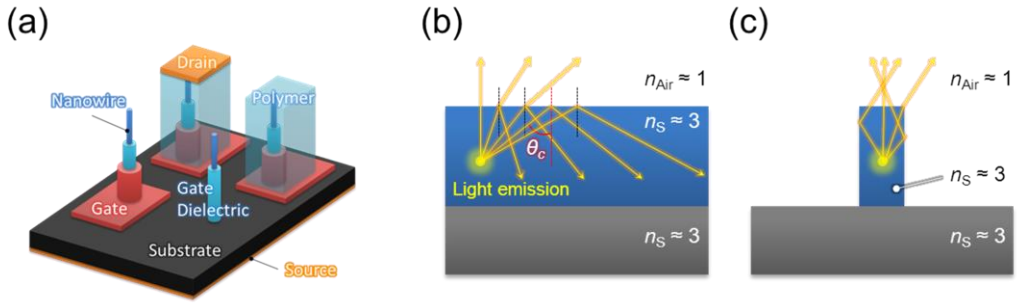

Figure 2–3

(a) Schematic illustration of vertical–surrounding–gate (VSG) transistors. (b) and (c) show schematic illustrations of refraction and reflection behavior of the light emitted from typical III–V semiconductors to the air for (b) planar semiconductor and (c) semiconductor nanowire, respectively. n_{Air} and n_s represent the infrared refractive index of air and semiconductor, respectively. θ_c represent the critical angle for the total reflection. Gray and blue regions in (b) and (c) represent the substrate and epitaxially grown layer, respectively.

short channel effects, which is one of the critical issues of scaled transistors, because the electric–field from drain or source is terminated to the surrounding gate electrode. Furthermore, drain or source electrodes are fabricated relatively easier than those in zero–dimensional (0D) structure systems. This feature is also adapted to the optical applications.

Additionally, such unique NW geometry also offers the high–performance light emitting devices with high light extraction efficiency. **Figure 2–3(b)** and **Figure 2–3(c)** show the schematic illustrations of the refraction and reflection behavior of the light emitted from typical III–V semiconductors for planar semiconductor (**Figure 2–3(b)**) and for semiconductor NWs (**Figure 2–3(c)**), respectively. In those cases, the critical angle of the light emitted from semiconductors for total reflection, θ_c, is given by Snell's law and is described as follows.

$$\theta_c = \sin^{-1}\left(\frac{n_{\mathrm{Air}}}{n_s}\right)$$

where n_{Air} and n_s ($n_s > n_{Air}$) are refractive index of air and semiconductors, respectively. Here, the infrared refractive index of typical III–V semiconductors is about 3 (e.g. GaAs: 3.3, InP: 3.1, InAs: 3.51, $In_{0.53}Ga_{0.47}As$: 3.43 [15]). When n_{Air} and n_s are set to be 1 and 3, the θ_c can be

estimated to be 19.5°. Consequently, the emitted light from III–V semiconductors with larger incident angle than 19.5° cannot be extracted to the air due to the total reflection as shown in **Figure 2–3(b)**, resulting in the low light extraction efficiency. On the other hand, NW geometry can extract the light more efficiently, utilizing the total reflection nature (**Figure 2–3(c**). This feature is suitable for light emitting devices, such as light–emitting diodes, lasers, and single–photon sources (SPSs) [15][17].

Large Surface/Volume ratio

Very small diameters of NWs with achieve larger surface more than 10 times that of planar surface. Because of these properties, NWs are promising building block for future applications in sensors and solar cells. For instance, NW sensing device is possible to overcome the sensitivity limitations of previous planar FET sensors and increases sensitivity to the point that single–molecule detection might be possible [18].

Axial and Radial *pn*/Hetero–Structures

Epitaxially grown NWs can grow including various *pn*/hetero–structures during a series of crystal growth. Type of *pn*/hetero–structures can roughly be divided into following two kinds of *pn*/hetero–structures, that is, axial (vertical) *pn*/hetero–structure and radial (lateral) *pn*/hetero–structure (**Figure 2–4**).

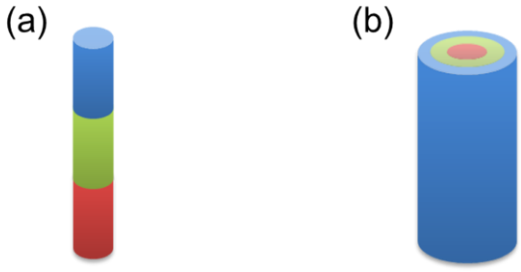

Figure 2–4

Schematic illustrations of two kinds of *pn*/hetero–structure nanowires. (a) Axial (vertical) *pn*/hetero–structure. (b) Radial (lateral) *pn*/hetero–structure.

For the axial *pn*/hetero–structure (**Figure 2–4(a)**), we can form the various *pn*–junctions along longitudinal direction of NWs. Moreover, the quantum wells (QWs) and/or quantum dots (QDs) can be embedded in a size– and position–controlled NW [19]–[23], this feature provides some opportunities for creating novel NW–based devices, such as the single–photon sources (SPSs) [24], QD memories [25], and avalanche photo diodes (APDs) [26].

For SPS applications, furthermore, QDs embedded in NWs (NW–QDs) have an advantage, that is, the fine structure splitting of excitons can be vanished in NW–QDs [27][28]. This is because the typical vertically–aligned III–V NWs grown on (111)–oriented substrate are consisted of six {–110} sidewalls, and has three–fold symmetry. Consequently, there is no intrinsic anisotropy for vertical and parallel polarizations. Such symmetry also leads to an expectation that the shape anisotropy of QDs on (111) surfaces is much smaller than those on (001) surfaces. This feature is important to realize the light source of entangled photon pairs.

On the other hand, the radial *pn*/hetero–structure (**Figure 2–4(b)**) also gives unique advantages to NW–based applications. Such kind of *pn*/hetero–structure is usually called "Core–Shell" structure. It should be noted that the core–shell structure cannot be formed by only the conventional planar and top–down technology.

For electrical devices, core–shell NWs are used for obtaining high electron mobility [29][30]. For instance, the field–effect transistors (FETs) using InAs/InP core–shell NWs exhibited the electron mobility of 11500 $cm^2V^{-1}s^{-1}$ at room temperature, which is substantially higher value than that of other synthesized one–dimensional (1D) nanostructures [29]. As for the optical devices, core–shell NWs are expected to be a promising candidate for high–efficiency light–emitting diodes (LEDs) [31] and solar cells [32][33], because these types of *pn*/hetero–structures have large injection areas. And these potentially achieve a large junction area of more than 10 times that of conventional planar LEDs.

Furthermore, whole surface of NWs can epitaxially be passivated by using the core–shell growth technique. This feature enables us to significantly improve the emission and absorption efficiency [34]–[36]. For instance, GaAs/AlGaAs core–shell NWs grown on Si substrate show dramatically enhancement of photoluminescence (PL) intensity compared to that

of the GaAs NWs on Si, where the value of PL intensity of AlGaAs/GaAs NWs was 490 times larger than that of GaAs NWs [34]. This indicates that the AlGaAs shell layer acted as a passivation layer to reduce the surface non–radiative recombination centers in GaAs NWs. This result suggests that the core–shell technique is important for *in situ* passivation of NWs.

Lattice–Mismatched Growth

Developments in semiconductor device applications have been supported by the progress in heteroepitaxial growth technology. Heteroepitaxial integration, however, remains inaccessible applications, due to the large lattice mismatches between the materials. The lattice mismatches between two materials, ϵ (%), is given as following equation,

$$\epsilon = \frac{a_{epi} - a_{sub}}{a_{sub}} \times 100,$$

where a_{epi} (Å) and a_{sub} (Å) is lattice constant of materials of epitaxial layer and substrate, respectively. For instance, the lattice mismatches with silicon (Si) for GaAs and InAs are 4.1 and 11.6 %, respectively.

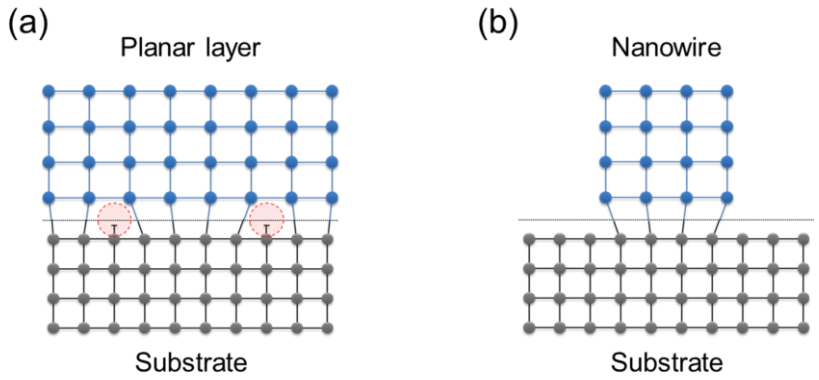

Figure 2–5

Schematic illustrations of lattice–mismatched growth in (a) planar and (b) nanowire growth techniques. The red dotted circles in (b) represent the positions of misfit dislocations. The black dashed lines represent the heterointerface between epitaxial layer and substrate. In a planar layer, misfit dislocations are formed due to lattice mismatch between the epitaxial layer and substrate. In a nanowire, its small diameter can relieve strain by expanding or contracting in the two lateral dimensions, relieving strain without misfit dislocations.

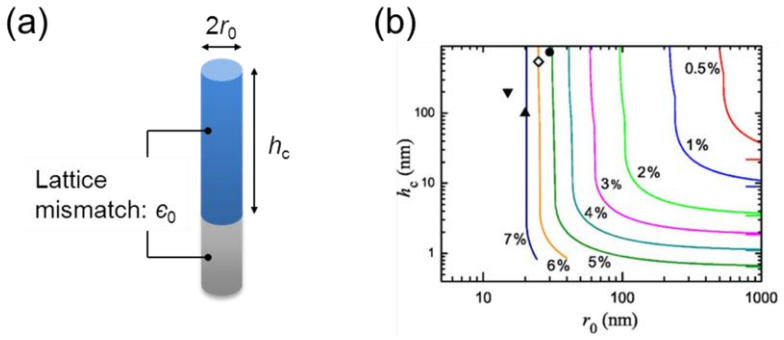

Figure 2–6

(a) Schematic illustration of the nanowire geometry with lattice mismatched heterostructure. (b) Variations of the critical thickness, h_c, of a misfitting layer growing on the top of a nanowire as a function of the radius, r_0, for various values of the lattice mismatch, ϵ_0, given in percent near each curve and a Poisson's ratio of 1/3. [39]

Large lattice mismatch induces poor quality of heterointerfaces with high misfit dislocation density. Such high density dislocation makes planar thin film epitaxial growth difficult. The defects act as preferred sites for impurity atoms, high–diffusivity paths for dopants, and sites for non–radiative recombination, limiting the performances of electrical/optical devices. J.W. Matthews and A.E. Blakeslee introduced a model for the onset of misfit dislocations in thin films, when the thin films are epitaxially grown on single crystal substrates. This model is based on thermodynamic assumptions and represents and elasticity approach. In this model, the epitaxial layers relax with forming defects when the layer is reached a certain critical thickness, which limits the dislocation–free thickness of a strained layer [37].

Figure 2–5(a) shows the schematic illustration of typical result of lattice–mismatched growth when $a_{epi} > a_{sub}$ (e.g. III–V materials on Si, InGaAs on GaAs). Due to the larger lattice constant of the epitaxial layer, the epitaxial material will be compressively strained at first, with respect to its typical equilibrium lattice constant. If thin film growth takes place until a certain critical thickness, the strain between the two materials will end up relaxing *via* misfit dislocations. High strain energies are released to form misfit dislocations, which are detriment for the device performance. On the other hand, the requirement for lattice matching is relaxed in heterostructure NWs, because of their small footprints or growth region. Thus, NWs may

exhibit surface–strain relaxation without the formation of extended defects usually observed highly mismatched materials as shown in **Figure 2–5(b)**. Therefore, NWs are usually single–crystalline and exhibit a high structural quality.

E. Ertekin *et al*. [38] and F. Glas [39] modeled this problem using equilibrium analysis to predict the critical diameters as a function of lattice mismatch. The critical diameter decreases as lattice mismatch increases as shown in **Figure 2–6**. For example, no threading dislocation is formed in 200–nm diameter NWs with as much as 2% lattice mismatched [39]. Therefore, an initially strained NW, in principle, can be grown infinitely long without generating any dislocations, as long as its footprint is smaller than the critical diameter.

This feature enables us to integration of III–V compound semiconductors on Si, as well as for the large lattice–mismatched systems in III–V compounds [34][40][41]. Fabrication technology of III–V materials on Si is the long–time challenge for integrating high performance III–V devices with main stream Si technology. It allows for the ability to select optimal material properties for various regions of a device. In particular, the ability to integrate III–V compound semiconductor materials with Si can realize so–called “Si photonics” as the way for light emitting or absorbing devices integrated directly with Si electronics.

No Process–Induced Damages

We described the many features and advantages of semiconductor NWs in this section. First one is originated from the geometry of NWs. The NW geometry has high aspect ratio with small diameter, which provides some advantages compared to conventional planar geometry, such as the increase of electron mobility and light extraction efficiency, as well as the suppression of short–channel effects in scaled transistors. In addition, high surface/volume ratio of NWs also gives some advantages particularly to the sensor device applications.

Second one is originated from the synthesis of NWs. NWs can be grown including axial and radial *pn*/hetero–structures, and both structures opens the opportunities for realizing novel device applications. Furthermore, NW synthesis enables us to form the single crystal with high structural quality even in large lattice–mismatched systems. For instance, III–V compound

semiconductors can be integrated on Si substrate by utilizing the growth techniques of NWs. These advantages of NWs cannot be achieved by only using conventional synthesis of planar semiconductors and top–down technology.

It should be noted again that such unique features and advantages of NWs are generated from a series of crystal growth technique without using fine top–down processing. In other words, the elongated and relatively complex nanostructures can easily be fabricated without any process–induced structural damages by using NW technology. Because the surface/volume ratio of three–dimensional (3D, stereoscopic) nanostructures like NWs is high, the process–induced structural damages or defects significantly influence and deteriorate the performance of nanoscale semiconductor devices. Therefore, this feature that NWs can be grown without any process–induced damages is very important benefit to realize nanoscaled and/or NW–based future application.

2.1.2.2 Advantages of Nanowire Arrays

Low Reflectance

When the NWs are grown as an array (**Figure 2–2(b)**), some additional advantages particularly for the optical device applications are appeared. For example, the reflectance at the interface between semiconductors and air is low for the array of NWs compared to that for the planar semiconductors, because the NWs are like a Moth–eye structure (**Figure 2–7(a)**).

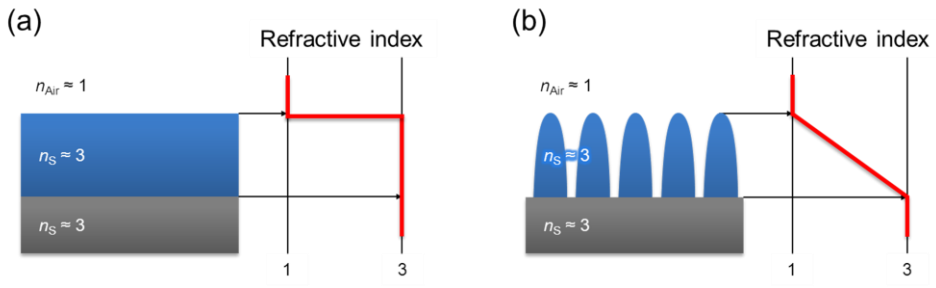

Figure 2–7

Schematics of variation of refractive index. (a) Planar structure. (b) Moth–eye structure. n_{Air} and n_s represent the (infrared) refractive index of air and semiconductor, respectively. Gray and blue regions represent the substrate and epitaxially grown layer, respectively.

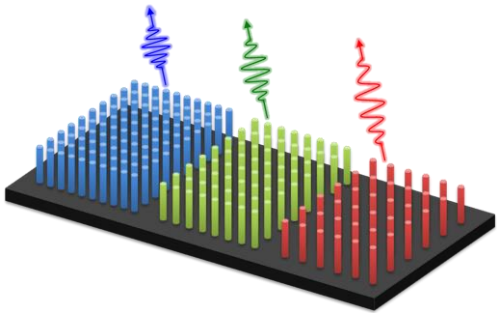

Figure 2–8
Schematic illustration of multi–wavelength–light emission from nanowire array.

Here, the reflectance, *R* (Power), when incident angle is 0° at the semiconductor–air (S–A) interface is given by Fresnel's formula and is described as follows,

$$R = \left(\frac{n_1 - n_2}{n_1 + n_2}\right)^2$$

where n_1 and n_2 is refractive index of certain medias 1 and 2, respectively. When n_1 and n_2 are set to be 1 and 3 (refractive index of air and typical III–V compounds), *R* is estimated to be 25%. In the other words, 25% of the light is lost by reflectance. While in the NW array, the reflectance at the S–A interface is significantly reduced [36][42]–[44], because the refractive index near the S–A interface varies gradually as shown in **Figure 2–7** [45]. This feature is one of the key advantages of NW arrays for optical applications, such as solar cells and LEDs.

Multi–Wavelength–Light Emission

In NW array growth, NWs emitting multi–wavelength–light can be fabricated on same substrate through a series of crystal growth (**Figure 2–8**). For instance, InGaN/GaN multiple–quantum–well (MQW) nanocolumn (NC) arrays formed on a same substrate exhibited visible emission changed from blue to red with increasing NC diameter [46]. This indicates the alloy composition of InGaN/GaN MQW NCs varied with changing its diameter, because the diffusion behavior of indium and gallium precursors is different in the crystal growth. Similarly, the alloy composition of InGaAs NWs varied with changing spacing between neighboring NWs [47]. Such feature of NW array opens new opportunities for developing light emitting applications.

2.2 Growth Techniques for Semiconductor Nanowires

2.2.1 Catalyst–Assisted Vapor–Liquid–Solid Growth

The Vapor–Liquid–Solid (VLS) mechanism has firstly been proposed by Wagner and Ellis in 1964 for forming one–dimensional silicon (Si) crystals, in which the particles act as seeds for the crystal growth [1], and the VLS is one of the major approaches for the nanowire (NW) growth. Origin of its name is the system involving a vapor–phase precursor (in that case, $SiCl_4$), a liquid alloying as the mediating material (AuSi), and a solid crystal (Si).

The schematic illustration of NW growth process by using catalyst–assisted VLS mechanism is shown in **Figure 2–9**. When a gas containing the growth (source) materials flows over the growth substrate, the precursor atoms prefer to deposit on the surface of the droplet and forms an alloy. Continued incorporation of precursor atoms into the liquid droplet leads to a supersaturation of the semiconductor component. As a consequence, crystal growth occurs at the solid–liquid interface and NW growth starts. The NW diameter is determined by the size of the droplet; if the droplet size is on nm–scale, we can control the wire diameter on nm–scale. In most cases, the droplet remains at the tip of the NW, as shown in **Figure 2–9(c)**.

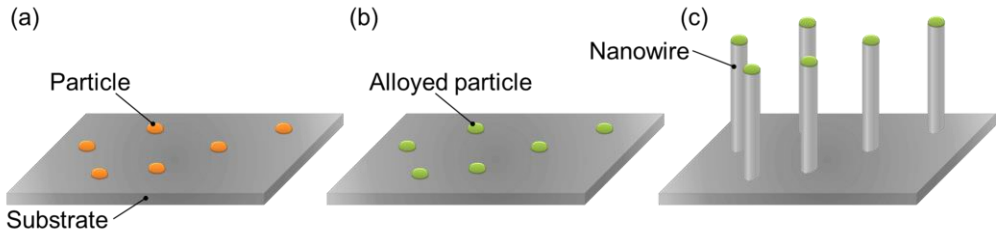

Figure 2–9

Overview of the fabrication procedures of semiconductor nanowires by using catalyst–assisted Vapor–Liquid–Solid (VLS) mechanism. (a) Metal seed particles are formed and/or deposited onto a substrate. (b) The sample is heated to a growth temperature and source materials are introduced. (c) When an appropriate supersaturation of growth materials is achieved, nucleation occurs at the particle–crystal interface. Then, the nanowire growth occurs at the particle–nanowire interface.

However, in this method, the control of NW position and size is hard due to the unintentional positioning of Au droplet made by annealing Au thin films or deposition of Au nano–particles. To overcome this critical issue, position controlled epitaxial NWs have been studied using lithographic positioning of metal seed particles. T. Sato *et al*. reported the site–controlled GaAs NWs by using a SiO_2 masked substrate [48]. In addition, B.J. Oholsson *et al*. developed a technique for the synthesis of size–selected III–V NWs grown on a crystalline substrate [49]. As catalysts, they used size–selected Au aerosol particles and can control the whisker diameter with size of Au particles.

In addition, the possible influence of metal–catalyst to contaminate VLS grown NWs has been a long standing concern. For instance, Au incorporation is known to result in deep–level defects near the mid–gap of Si, which drastically reduces the minority carrier lifetime and generally should be avoided in the context of active devices. In fact, high–angle annular dark–field (HAADF) scanning transmission electron microscopy (STEM) images of Si NWs have indeed shown the existence of Au atoms in Si NWs [50]. Using HAADF–STEM, Au atoms were observed in higher numbers than expected from a simple extrapolation of the bulk solubility to low growth temperature. It should be noted that the incorporation of Au is a problem not only for Si NWs, but also for NWs of any materials including III–V semiconductor.

Alternative method to metal catalyst–assisted VLS has been reported, where NWs can be grown by so–called “self–catalytic” processes without using Au or the other metals as a “catalyst”. Here, one constituent material of the NW forms the catalytic droplet, enabling VLS growth on top of the NW [51][52] and core–shell and axial heterostructure NWs formed using a self–catalyst based on VLS mechanism have been reported [53][54]. Si and Ge NWs grown from a thin SiO_2 layer without using metal catalyst have also been reported [55].

In addition, a few examples of catalyst–free growth of III–V NWs have been reported, (e.g., oxide–assisted growth). For instance, GaAs NWs (covered with gallium oxide) are synthesized via the laser ablation of a mixture of GaAs and gallium oxide. This growth was explained by a growth mechanism based on an oxidation–reduction reaction of gallium oxide, which is significantly different from catalyzed VLS growth mechanism.

2.2.2 Catalyst–Free Selective–Area Growth

Selective–area growth (SAG) is a template method which is the combination of bottom–up and top–down approaches. This method is different from the VLS, where any catalysts are not needed for one–dimensional crystal growth. Thus, there have been no concerns over contamination originated form any catalysts. In addition, the SAG enables the fabrication of nanowires (NWs) with precisely controlled their size and position due to the use of partly masked substrate with lithographically defined openings as a template for NW growth. The NW growth in SAG proceeds under the faceting growth mechanism [56]. Because the preferential growth directions are <111>A or <111>B, III–V (111)A or (111)B oriented substrate is usually adopted for the growth of vertically–aligned NWs surrounded by six {110} vertical sidewalls. Mask materials used usually in SAG are amorphous films, such as SiO_2 and SiN_x. Schematic illustration of NW growth process in the catalyst–free SAG is shown in **Figure 2–10**, and its advantages are generally summarized as follows,

i. Formation of defect free structures in nm–scale without process–induced damage and contamination.

ii. Atomically smooth interfaces and surfaces are obtained.

iii. Position and size of grown structures can be controlled in nm–scale based on a standard lithography technique.

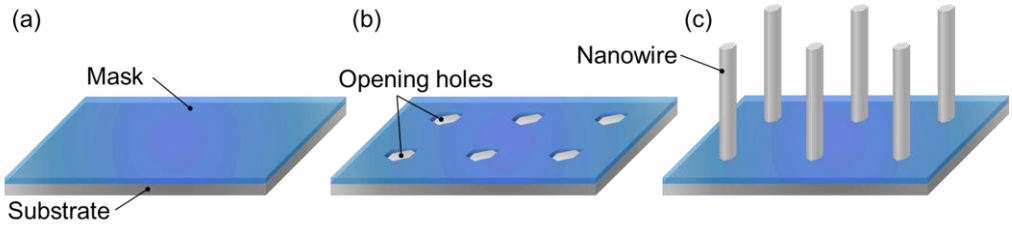

Figure 2–10

Growth process for forming nanowires by using catalyst–free selective–area growth. (a) Formation of mask material onto the substrate (e.g., SiO_2). (b) Fabrication of the opening holes by using lithography and etching technique. (c) Crystal growth for forming nanowires.

The research on the SAG has been begun in early 1960's, where Si was grown by chloride phase epitaxy and was firstly used for integrated circuit [57]. In 1965, F.W. Tausch *et al*. reported the first demonstration of the SAG of GaAs and showed that single crystal epitaxial growth of GaAs occurs in SiO_2 windows on GaAs substrate, and that the growth tends to appear the facets grown most slowly [58]. A quarter–century later, H. Asai *et al*. reported the narrow two–dimensional electron gas (2DEG) channels in GaAs/AlGaAs sidewall interface [59], by using selective–area metal–organic vapor–phase epitaxy (SA–MOVPE).

Formation of the small structures having {–110} vertical facets normal to the (111)B–oriented surface has been demonstrated by T. Fukui *et al*. in 1990 [60]. S. Ando *et al*. demonstrated that the micron–sized hexagonal pillar structures with the {–110} facets as a vertical sidewalls could be formed and these structures have been applied into laser and photonic crystals in 1993 [61]. Today's NW fabrication technique by using SAG is based on this strategy. T. Hamano *et al*. reported GaAs pillar with small diameter with nm–scale selectively grown along the <111>B axial direction by using MOVPE on a GaAs (111)B substrate with lithography–defined SiO_2 mask opening in 1997 [62]. In 2004, J. Motohisa *et al*. investigated the diameter dispersion of GaAs hexagonal pillar arrays selectively grown by MOVPE in an effort to fabricate a photonic crystal lattice [63], and they proposed SA–MOVPE as the catalyst–free fabrication technique for the growth of "Nanowires" [64].

Our group has intensively been studied the SAG of III–V compound semiconductor NW arrays, such as GaAs [65], InAs [66], InP [63][67], and InGaAs [68], by using MOVPE over the past several years. Moreover, various kinds of heterostructure NWs, such as GaAs/InGaAs axial (vertical) heterostructures [69], GaAs/AlGaAs radial (lateral) [35] and axial heterostructures [70], an InAs quantum tube sandwiched by InP [71], GaAs/GaAsP radial/axial heterostructure [19][72], and InP NW including InAsP quantum dot [20][73], have been fabricated to characterize crystal structures, atomic composition profiles, and photoluminescence properties with quantum size effects. In addition, the use of low cost substrate, such as Si and poly–Si, for SAG of III–V NWs has actively been investigated [34][41][74]. In particular, site–controlled and vertically–aligned InAs NWs and GaAs/AlGaAs radial heterostructure NWs have been achieved with quite high uniformity of their size.

2.3 Nanowire–Based Applications

Potential features in nanowires (NWs) and their synthesis, mentioned in **Section 2.1.2**, have continuously been generating many innovative ideas of novel applications. Simultaneously, the rapid progress in the researches on NW–based device applications really requires deeper understanding of fundamental properties of NWs and their growth. Our research described in this thesis is also driven by the developments in the studies on NW–based applications. In this section, we briefly introduce some notable examples of applications using NWs, regarding electronic, optical, thermoelectric, and sensor devices. This brief introduction is not intended to be comprehension of all unique ideas proposed previously. Nevertheless, these examples enable us to understand how the NWs can be a promising material for device application.

2.3.1 Electronic Devices

Field–Effect Transistors

With scaling of planar Si CMOS no longer a long–terms option, other approaches to improved device performance are investigated. As device dimensions are scaled down to the sub–20–nm range, it becomes extremely difficult to define device patterns by optical lithography techniques, so–called top–down techniques. Self–assembled III–V compound semiconductor NWs are promising building blocks for future scaled down and high efficient electronic devices [75].

There are two major possible benefits of NWs for electronic devices. First one is achieving integration of two lattice–mismatched materials without the formation of extended defects that is cause of detrimental for the device performance. Due to their small lateral dimensions, NWs may exhibit surface–strain relaxation. Another possible benefit of NWs is the vertical geometry which enables vertical transistors where the gate length can be controlled with high precision through the deposited metal thickness. Additionally, surrounding gate electrodes and the thin one–dimensional NW channels give an opportunity for ideal channel control. For example, vertical surrounding gate InAs NW transistors on Si substrate have been demonstrated

[76]. The NW geometry is also a practical geometry for realizing steep–slope devices such as tunneling field effect transistors (TFETs). The cylindrical geometry simplifies gate positioning at the tunnel junction, and the possibility to combine lattice–mismatched materials gives a great flexibility in the design of tunnel junction. Furthermore, one–dimensional transport, which is attainable in NWs, could potentially be a requirement for sub–60mV/dec operation [77]. As we mentioned before, an initially strained NW, in principle, can be grown infinitely long without generating any dislocation, as long as its footprint is smaller than the critical diameter. This lateral relaxation opens an opportunity to integrate high–quality III–V NWs onto Si–based electronic devices. Therefore, some fundamental research for growing III–V NWs on Si substrate and realizing steep–slope behavior [78] was conducted recently.

2.3.2 Optical Devices

Light–emitting diodes

There have been a number of advancements of optical devices using NWs in recent years. Radial heterojunctions, known as core–shell structure which has radial composition and/or material variations, have been employed for carrier and photon confinement along two dimensions, with propagation allowed along the axis of the wire [72][79]. This unique confinement has led to many reports of nanowire lasers [11][72][80]–[82], and light–emitting diodes (LEDs)[31][83]–[85]. The optical properties of these structures depend on the materials present, their spatial arrangement, and the size of the structure. Ultimately, such building blocks could lead to a wide range of more complex photonic devices and possibly even “silicon photonics” that is integration of photonic elements into traditional CMOS integrated circuits (ICs). For light emitting devices, core–shell nanowires, which is radial heterostructure fabricating in a NW, are expected to be a promising candidate for high–efficiency LEDs, because these types of heterostructures have large junction areas and potentially achieve a large junction area of more than 10 times that of conventional planar LEDs.

Solar cells

Energy generation is another area where NW materials offer unique possibilities for improving current technology, and NW–based solar cells are one example [86]–[91]. For conventional solar cells that have a planar layer structure with *pn* junction, increases in absorption are possible by increasing thickness of each layer, but this typically leads to increased recombination and thus no overall performance improvement. On the other hand, NW–based solar cells with radial *pn* junctions have a large length for absorption of light along the axial direction, while a short dimension for collecting of carriers along the radial direction is maintained. These results in devices that can absorb more of the incident radiation without requiring long diffusion length of carriers before collection, thereby NW–based solar cells can give overall efficiency improvements.

Another important feature of NWs for solar cell application is available for axial hetero–junction with highly lattice–mismatched materials. Good quality axial hetero–junction nanowires can be formed despite highly lattice mismatched. For example, no threading dislocation is formed in 200–nm diameter NWs with as much as 2% lattice mismatched [39]. This is an important advantage for multi–junction NW solar cell formation. If we fabricate four junction (InGaP/AlGaAs/InGaAs/InGaAs) NW solar cells with the diameter of less than 200 nm, theoretical calculation suggests that coherent growth could be obtained without misfit dislocation formation [39] and the efficiency has been calculated at 55.3% [92].

Recently, “flexible nanowire solar cell array” without a substrate are proposed as an entirely new strategy for achieving dramatically improvement of efficient utilization of semiconductor materials with maintaining the high efficiency. This type of structure can be fabricated by peeling of the as–grown NWs from the substrate using interface stress between the NWs and substrate. This enables the substrate to be used many times, and it would greatly reduce the material cost of nanowire solar cells. In comparison to conventional solar cells, the flexible nanowire solar cell array is requires two orders less of semiconductor materials for same electric power generation [91].

2.3.3 Thermoelectric Devices

Nanowires (NWs) have also been investigated for use in thermoelectric devices, which is one of an application in energy generation. The reduced dimensionality of NWs affects both the electrical and thermal conductivity of the material, thereby altering the thermoelectric figure of merit ZT [93]. Surface roughness on Si NWs increases phonon scattering over bulk materials, thus reducing the thermal conductivity and ultimately increasing ZT by a factor of approximately 100 over bulk Si [94]. The Si NW devices studied so far still trail behind the best bulk thermoelectric materials, although they are more easily integrated into existing Si integrated circuits (ICs), with the exciting possibility of on–chip thermal energy recovery or cooling applications [95].

2.3.4 Sensor Devices

Higher surface/volume ratio of nanowires (NWs) compared to the bulk materials makes them attractive as sensors [9]. Patolsky *et al*. [18] were able to detect the binding of single Influenza A viruses to Si NW based sensors. The same group also demonstrated multiplexed detection of several important cancer marker proteins using similar NW sensors [96]. Charged target molecules bind to ligands on the surface of the Si NW field effect transistors (FETs), and their electric field causes depletion of charge carriers in the semiconductor. In similar bulk devices, depletion is limited to the region near the surface, whereas the high surface area to volume ratio of NWs allows the external field to affect the entire volume of the wire, thus increasing the sensitivity of the devices over bulk sensors [9].

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Chapter 3

Experimental Techniques

3.1 Introduction

This chapter gives a brief overview of the experimental techniques for fabrication and characterization of the nanowires (NWs) used in this work. In this study, InGaAs NWs are formed by selective–area metal–organic vapor–phase epitaxy (SA–MOVPE) which is one of the bottom–up and self–assembled formation methods of semiconductor nanostructures based on pure vapor phase growth. In SA–MOVPE, we used a substrate partly covered with mask material as a template for crystal growth in MOVPE. These fabrication methods of masked substrate and growth technique of MOVPE growth bring us to well–controlled position and size of NWs. First of this chapter, we introduce the system and principle of MOVPE and the details of NW fabrication procedures in SA–MOVPE.

After the growth, NWs have to be characterized from morphology and shapes of the structures. Due to their small dimensions, the resolution of optical microscopy is not sufficient; electron sources have to be used instead of optical one. The overall morphology and shapes of the nanostructures are investigated by scanning electron microscopy (SEM). Then, deeper insights in the optical properties of NWs are given by micro–photoluminescence measurement.

3.2 Metal–Organic Vapor–Phase Epitaxy

3.2.1 Overview

Epitaxial growth is defined as a precise oriented growth of a single crystal material upon the surface of a single crystal substrate. Growth of a layer with the same kind of atoms as are in the substrate is called homoepitaxy, and growth with a different kind of atoms is called heteroepitaxy. The growth of epitaxial films can be done by a number of methods including liquid phase epitaxy (LPE), molecular beam epitaxy (MBE), vapor–phase epitaxy (VPE), hydride vapor–phase epitaxy (HVPE), and metal–organic vapor–phase epitaxy (MOVPE). Such methods for the epitaxial growth are important and are used to produce high quality single crystal layers with low defect density and complex heterostructures for electrical and optical applications.

In particular, MOVPE is one of the leading techniques for the production of III–V materials for electric and photonic devices. In this technique, III and V metal–organic (MO) and hydride molecules are used for growing III–V compound semiconductors. These source molecules are provided to growth substrate with purified hydrogen or nitrogen gas and diffuse near the surface of the growth substrate. These molecules are thermally decomposed and then chemically react near the surface of growing substrate. Atoms are incorporated at certain positions on the surface in relationship to the underlying crystal structure. For instance, trimethylgallium (TMGa), $Ga(CH_3)_3$, and arsine, AsH_3, are introduced above a heated GaAs substrate, an epitaxial film of GaAs can grow according to the following reaction,

$$Ga(CH_3)_3(g) + AsH_3(g) \rightarrow GaAs(s) + 3CH_4$$

where (g) and (s) represent “gas” and “solid” phase, respectively.

The major attraction of MOVPE relative to the other techniques is that the MOVPE is suitable for mass production. Moreover, this single growth technique can be used to produce virtually all of the III–V materials and structures required for the cutting edge of electronic and photonic devices including AlGaInP for red or yellow light–emitting diodes (LEDs), III–V nitrides for blue LEDs, and III–V highest efficiency tandem solar cells.

3.2.2 MOVPE System

This section explains the MOVPE system used in this work. **Figure 3–1** shows the schematic illustration of the MOVPE system. The essential components are the gas delivery system, the reactor and temperature controller, and the low pressure pumping system. All growth in this work was carried out with a horizontal low–pressure MOVPE system.

First, we describe about gas delivery system. Palladium diffused purified hydrogen (H_2) is used as a carrier gas. The carrier gas transport the source gases flowing over the heated susceptor and substrate to the exhaust as shown in **Figure 3–2**. The vapor–phase source molecules are fed to the reactor in separate lines for metal–organic (MO) source and gas source. The MO sources are provided from bubblers and gas sources are provided from gas cylinders.

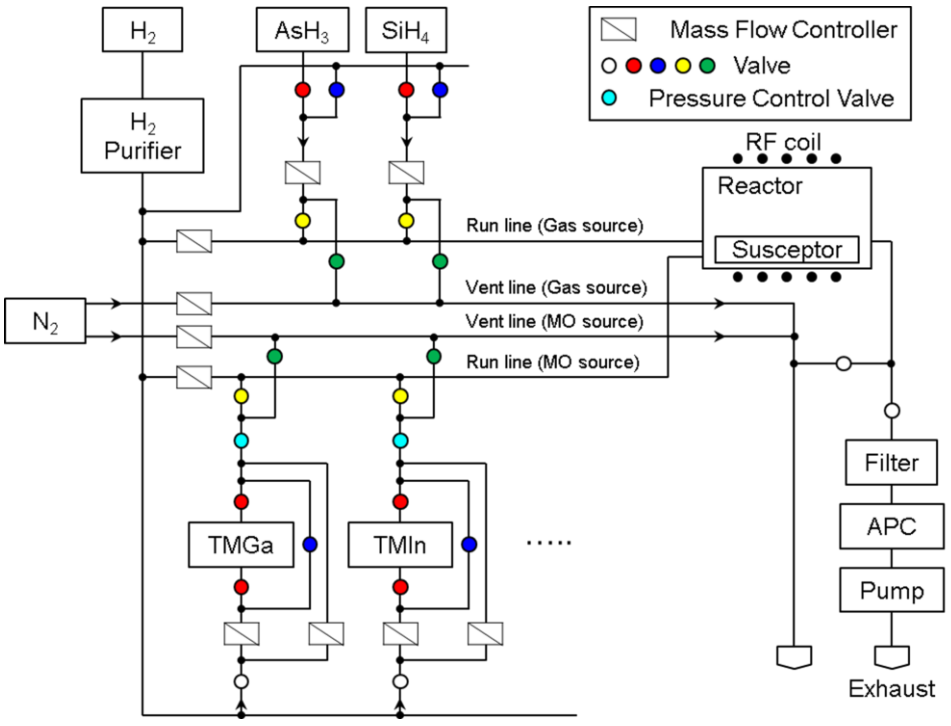

Figure 3–1

Schematic illustration of the MOVPE system. Red valves are opened (or are closed) and blue valves are closed (or are opened) when the source is used (or is not used). Yellow valves are opened and green valves are closed when the source is fed to the reactor, and yellow valves are closed and green valves are opened when the flow from the source is led through the vent line to the exhaust.

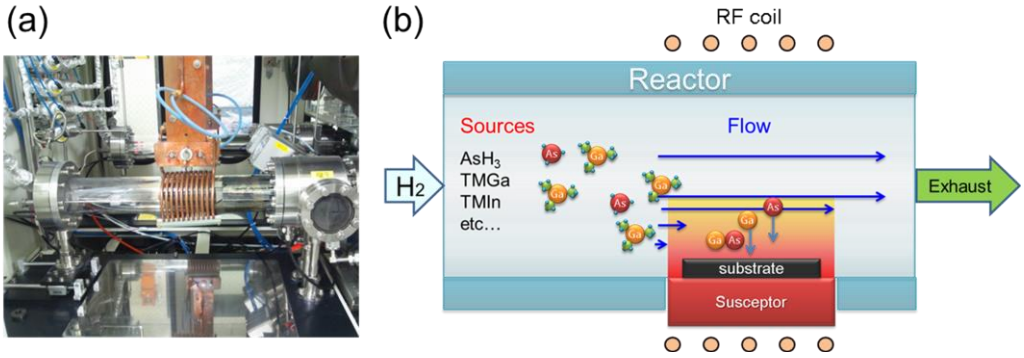

Figure 3–2

(a) MOVPE reactor. (b) Schematic illustration of the MOVPE reactor.

The MOVPE reactor used as the growth chamber was horizontal type SiO_2 tube (**Figure 3–2(a)**). The substrate for NW growth was put on a graphite block (or carbon susceptor) or quartz plate inside the reactor and the graphite was heated by radio frequency (RF) induction (**Figure 3–2(b)**). The substrate temperature was monitored by a thermocouple inserted beneath the graphite block. The total flow rate of the gases in the reactor was maintained at 4.00 or 3.00 standard liters per minute (SLM). The working pressure of 0.1 atm is automatically maintained with automatic pressure controller (APC) and by vacuum pumping during MOVPE.

3.2.3 Source Molecules

The MO source materials for group–III are trimethylgallium (TMGa), trimethylindium (TMIn). Tertiarybutylphosphine (TBP) is used for the MO source material for group–V. Silane (SiH_4, gas) and diethylzinc (DEZn, MO) are used for *n*–type and *p*–type doping, respectively. For group–V gas source, 5% or 20% arsine (AsH_3) diluted in H_2 is used.

The MO sources are provided in the bubblers, which are kept at a certain temperature by the thermal bath to control and maintain the partial pressure of material supply as shown in **Figure 3–3(a)**. The carrier gas is led through the liquid or solid source material in the bubbler. As a result, the carrier gas contained MO sources with saturated vapor pressure, which is controlled by the temperature of the bubbler, is provided to the reactor (**Figure 3–3(b)**). The partial pressure of each MO sources fed to the reactor is determined by the carrier gas flow

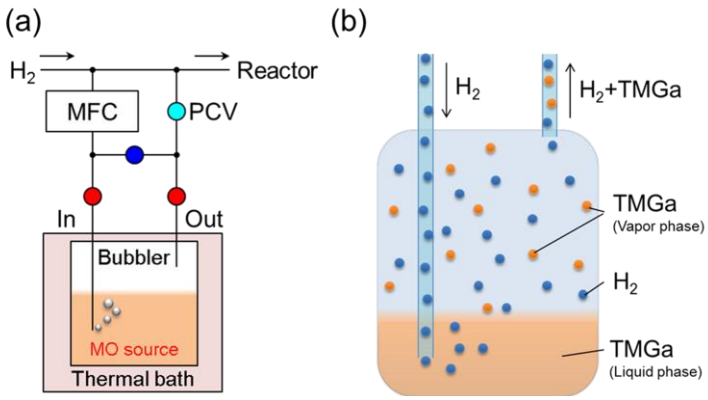

Figure 3–3

(a) Schematic illustration of the line for metal–organic (MO) source provided by bubblers. Red valves are opened (or are closed) and blue valves are closed (or are opened) when the source is used (or is not used). From the viewpoint of safety, red valves and blue valves are normally open and normally close type, respectively. A pressure control valve maintains the pressure inside of bubbler at the desired value around 760 Torr. (b) Schematic illustration of the inside of the bubbler. In this illustration, trimethylgallium (TMGa) is carried along with the flow of carrier gas (H_2).

through the bubbler which is controlled by mass–flow controllers (MFCs). Pressure controller keeps a fixed pressure in the bubbler, and then, mixture of H_2 and MO down to the reactor pressure.

The vapor pressure of a MO sources is a critical parameter used to control the precise concentration of MO sources entering the reactor, and subsequently the rate of deposition in the MOVPE process. Hence, an accurate evaluation of the vapor pressures of the MO sources is essential to the MOVPE process. The vapor pressure equation in linear logarithmic form,

$$log_{10}P_{MO} = B - \frac{A}{T}$$

has been found to be the most acceptable form for representing the vapor pressure of MO sources (P_{MO} (Torr)) in MOVPE, where T (K) is the absolute temperature of MO sources (or thermal bath) and A and B are the gas constant for each MO sources as shown in **Figure 3–4** [1]–[7].

(a)

	A	*B*	Ref.
TMGa	1703	8.07	[1], [2]
TMIn (New)	3204	10.98	[3], [4]
TMIn (Old)	3014	10.52	[3], [5]
TBP	1529	7.552	[6]
DEZn	2109	8.28	[1], [7]

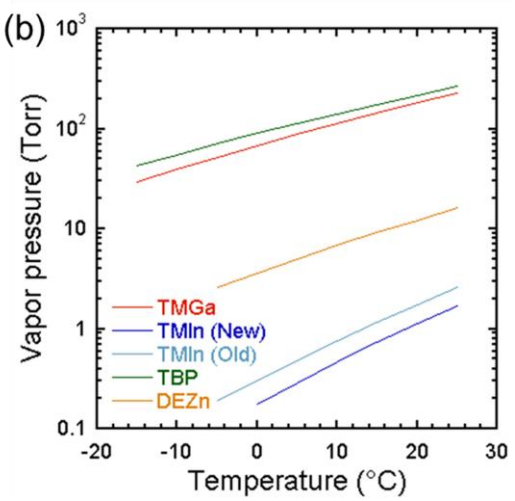

Figure 3–4

(a) Properties on the vapor pressure of metal–organic (MO) sources. (b) Saturated vapor pressure curves for trimethylgallium (TMGa), trimethylindium (TMIn), tertiarybutylphosphine (TBP), and diethylzinc (DEZn). As for the vapor pressure curve of TMIn, we used the new and old gas constant.

In this study, the temperatures of TMGa, TMIn, TBP, and DEZn are set to be –9, 5, 10, and 3 °C, respectively. Under these conditions, the vapor pressure of TMGa, TBP, and DEZn can be calculated to be 41.97, 141.92, and 4.39 Torr, respectively. As for the TMIn, when we use the new gas constant [3], the vapor pressure of TMIn is calculated to be 0.29. Meanwhile, the vapor pressure of TMIn is calculated to be 0.48, when we use older gas constant [5]. Although the new gas constant of TMIn gives accurate vapor pressure equation, in this work, we used the older gas constant for the comparison of the results between this work and our previous reports.

To calculate the flow of the MO sources from a bubbler, we consider the typical arrangement shown in **Figure 3–4**. The flow of carrier gas (H_2), F_{H2} (sccm), is measured by mass flow controller (MFC), and then enters the bubbler at some input pressure, P_{H2}. A pressure control valve maintains the pressure inside of bubbler at the desired value around 760 Torr, $P_{bubbler}$. The carrier gas is assumed to be completely saturated by vapor–phase MO sources. The total pressure within the bubbler, $P_{bubbler}$ (Torr) is given by following equation,

$$P_{bubbler} = P_{H_2} + P_{MO} = 760 \text{ (Torr)}.$$

The total flow of outlet hydrogen gas containing MO sources, F_{H2+MO} (sccm), can be calculated using simple ideal gas equation given by,

$$F_{H_2+MO} = F'_{H_2} + F_{MO} = \frac{P_{H_2} + P_{MO}}{P_{H_2}} F_{H_2} = \frac{P_{bubbler}}{P_{H_2}} F_{H_2} = \frac{P_{bubbler}}{P_{bubbler} - P_{MO}} F_{H_2},$$

where F'_{H2} (sccm) and F_{MO} (sccm) are the flow of H_2 and MO at outlet of the bubbler, P_{H2} (Torr) is the partial pressures of H_2 at outlet of the bubbler, and P_{MO} (Torr) is saturated vapor pressure described in **Figure 3–4** and is also the partial pressure of MO at outlet of the bubbler. The flow of gas through the reactor is typically dominated by H_2, and includes the total flow associated with the gas sources such as AsH_3 and SiH_4, the total flows associated with the MO bubblers, and counter (outer tube) purge flows. The total reactor pressure $P_{reactor}$ is 76 Torr, in this study.

Keeping this information in mind, the partial pressure of MO sources, [MO] (atm), is given by following equation,

$$[\mathrm{MO}] = \frac{F_{MO}}{F_{reactor}} \times \frac{P_{reactor}}{760}$$
$$= \frac{P_{MO}}{P_{bubbler} - P_{MO}} \times \frac{F_{H_2}}{F_{reactor}} \times \frac{P_{reactor}}{760}$$
$$= \frac{P_{MO}}{P_{bubbler}} \times \frac{F_{H_2+MO}}{F_{reactor}} \times \frac{P_{reactor}}{760},$$

where $F_{reactor}$ (sccm) (= 4000 or 3000 sccm, depending on MOVPE system used in this study) is total flow rate of the inner tube of the reactor, which is contributed to the crystal growth.

On the other hand, the partial pressures of gas sources, [Gas] (atm), is simply described by following equation,

$$[\mathrm{Gas}] = \frac{F_{Gas}}{F_{reactor}} \times \frac{m}{100} \times \frac{P_{reactor}}{760},$$

where F_{Gas} (sccm) is the flow rate of gas source and m (%) is percentage of diluted gas sources in H_2. [MO] and [Gas] are essentially important for the crystal growth in MOVPE.

3.2.4 Thermal Decomposition of Source Molecules

As shown in **Figure 3–2(b)**, supplied metal–organic (MO) and gas sources are thermally decomposed by the heated temperature of susceptor near the surface of substrate. The decomposition behavior is dependent on the kinds of source material, and this factor is also important for the crystal growth. The thermal pyrolysis (or decomposition) of MO and gas sources has been studied [8]–[15]. Typically these studies monitor, optically or through mass spectrometry, the decrease in the concentration of a particular reactant as it passes through a SiO_2 reactor. The temperature ranges for thermal pyrolysis for various MO and gas sources are summarized in **Table 3–1**. The kind of carrier gas affects the pyrolysis range, for instance, the pyrolysis range for TMGa diluted in N_2 is higher than that for H_2 carrier gas. In addition, the pyrolysis range for AsH_3 is strongly affected by the presence of GaAs wafer and TMGa [14]. In this work, we used TMGa, TMIn, and AsH_3 with H_2 carrier gas for forming InGaAs NWs, and the used growth temperature was above 590 °C. Thus, we think that the source molecules used in this work are completely decomposed by the temperature for InGaAs NW growth.

	Carrier gas & Experimental condition	Pyrolysis range (˚C)		Ref.
		start	completed	
TMGa	H_2	370	470	[8], [9]
TMGa	H_2	400	580	[8], [10]
TMGa	N_2	450	570	[8], [9]
TMIn	H_2	~ 250	~ 340	[8], [12], [13]
TMIn	H_2	~ 300	~ 340	[8], [11]
TMIn	N_2	~ 340	~ 430	[8], [11]
AsH_3	H_2	650	750	[8], [10]
AsH_3	H_2	~ 470	~ 640	[14]
AsH_3	H_2 + GaAs wafer	< 450	~ 640	[14]
AsH_3	H_2 + TMGa (V/III =25)	< 450	~ 570	[14]
AsH_3	H_2 + TMGa (V/III =10)	< 450	~ 570	[14]
TBP	H_2	400	550	[15]

Table 3–1

Thermal pyrolysis (or decomposition) of various metal–organic (MO) and gas sources.

3.3 Principle of MOVPE

3.3.1 Overview

The study of the kinetics in MOVPE involves the attempts to understand the actual processes how the vapor phase source materials are transformed into the atoms constituting the semiconductor solid. Because these mechanisms are extremely complex, the description of the processes should be divided into that of some major processes. The key processes during the crystal growth in MOVPE have been summarized by Stringfellow [1] and are listed below.

iv. Mass transport: The carrier gas carries the source materials to the reactor. A boundary layer above the growing surface is formed by the laminar flow of the vapor in the reactor. Molecules diffuse through the boundary layer towards the surface before surface reactions can take place. The growth pressure and the velocity of the carrier gas define the thickness of the boundary layer.

v. Physical process: At the surface during growth, adatoms such as molecules and radicals absorb at the substrate surface, and in homogeneously deposit at the surface. Adatoms incorporate into appropriate lattice positions at kinks or steps, or desorb into the vapor phase, while species at the surface diffuse at the substrate surface. At the growing surface, two– or three–dimensional nucleation can be occur and surface takes the energetically stable configuration as a surface reconstruction, simultaneously.

vi. Chemical reactions: It must be taken into account for a more detailed description of the growth process. For MOVPE, the chemical processes have very complex radial reactions. Surface reconstruction, adsorption or desorption process of precursors, and density of step, kink or other defects are also strongly depended by the chemical reaction. Moreover, we should consider the thermal decomposition of source molecules under certain growth conditions.

vii. Thermodynamics: The growth rate is affected by thermodynamic properties since these define the deviation from equilibrium and thus the driving force for growth. The incorporation of native defects or dopants and surface stoichiometry are also

influenced by thermodynamics. Furthermore, the reason to selective growth can be explained by thermodynamics.

3.3.2 Mass Transport (Boundary Layer Model)

The precursor gases are transported to the reactor with the carrier gas and flowing over the growth substrate. The boundary condition between the gas flow and the reactor walls or surface of substrate is that the velocity is zero according to Newton fluid model. Naturally, the velocity component perpendicular to the surface is zero since no flux across the boundary exists. As a consequence of this boundary condition, the gas velocity is slower near the wall of the reactor as shown in **Figure 3–5(a)**. This region, in which gas velocity is decreased, is referred to as the boundary layer. The boundary layer thickness, δ, defined here as the distance from the interface at which the velocity component parallel to the wall becomes 99% of its free–stream value, is inversely proportional to the square root of the gas velocity. The boundary layer model is the most widely used model for the calculation of the growth rate in the mass transport limited growth. This model assumes that mass transport occurs only by diffusion through the boundary layer.

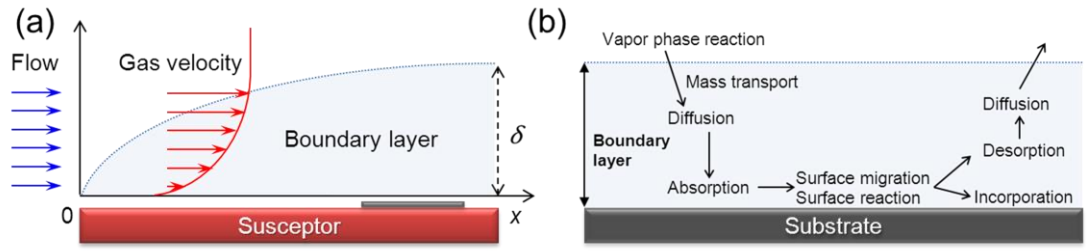

Figure 3–5

(a) Schematic illustration of the flow into the reactor, gas velocity decreasing near the susceptor surface, and boundary (stagnant) layer. The δ represents the thickness of boundary layer. The gas flow feeds from left side ($x < 0$, upper stream of the reactor) to right side ($x > 0$, downstream of the reactor) of this figure. The black rectangle lied on the susceptor represents the growth substrate. The vertical axis represents the direction, which is perpendicular to the surface of the susceptor or to the growth surface of the substrate. (b) Schematic illustration of the some kinds of mechanisms involved in the MOVPE process.

Figure 3–5(b) shows schematic illustration of the different mechanisms involved in the MOVPE process. There are some concentration gradients of the growth species during the growth, because the growth species are consumed at growth surface by incorporation of growth species into the crystal. The precursors diffuse from the gas flow to the surface of substrate driven by the concentration gradients of growth species. The diffusion flux from the boundary layer by concentration gradient, J_{in}, is

$$J_{in} \approx \frac{P_{in-III} - P_{sub-III}}{RT_s\delta} \approx \frac{P_{in-III}}{RT_s\delta}$$

where P_{in-III} is input partial pressure of group–III material in the gas flow, $P_{sub-III}$ is partial pressure of group–III material at the growth surface, R is gas constant, T_S is growth temperature and δ is thickness of boundary layer. In the case of planar growth, $P_{sub-III}$ can be ignored, because almost growth species at the growth surface consumed by the crystal growth.

Under the standard growth condition for III–V compound semiconductors, group–V precursors are sufficient near the surface of the substrate and maintain a thermal equilibrium condition between the surfaces, because the partial pressure of group–V materials is much higher than that of group–III material. For instance, at standard growth condition of GaAs in MOVPE, concentration of TMGa is only 0.01 ~ 0.001 % in all of gas flow. Moreover, chemical reaction rate at the surface is much higher than the diffusion flux of precursors. Therefore, in the case of planar growth, desorption of group–III materials from the surface can be ignored, and the growth rate is determined by only J_{in}.

As for the correlationship between δ and the growth rate, Leys and Veenvliet showed that increasing the flow velocity increases the growth rate due to a decrease in the mass transport boundary layer thickness [16]. This led to the idea of tilting the susceptor or superior wall of flow channel to compensate for gas phase depletion effects and the increasing boundary layer thickness along the flow direction due to the developing concentration profile. The use of this reactor configuration of controlling the gas flow leads to improved thickness uniformity.

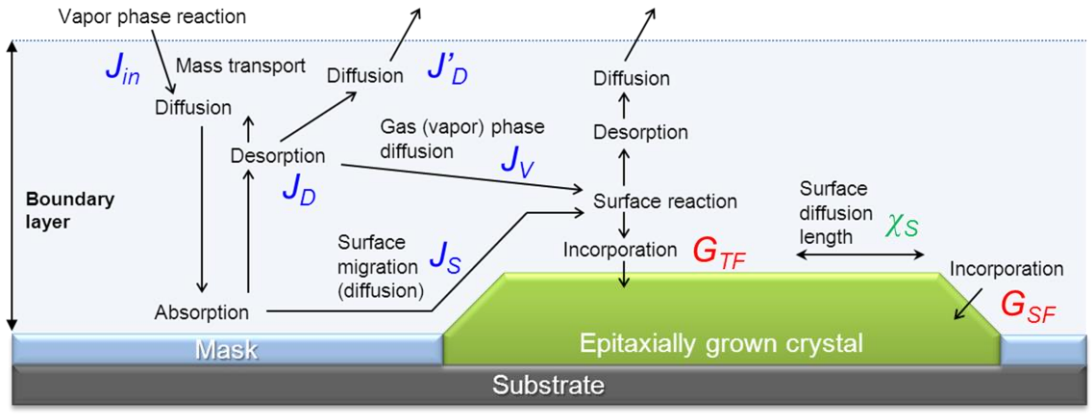

Figure 3–6

Schematic illustration of the some kinds of mechanisms involved in the selective–area (SA) MOVPE process.

In the case of selective–area growth, the situation is more complicated. **Figure 3–6** shows schematic illustration of some kinds of mechanisms involved in the selective–area (SA) MOVPE process. We should take into account that the growth rate is affected by diffusion of the growth species from masked region and desorption to the outside of the boundary layer, in addition to controlling the boundary layer thickness and diffusion of growth materials etc. for the planar growth. G_{TF} and G_{SF} shown in **Figure 3–6** indicate the growth rate for top and side facet of the grown crystal, respectively. In the case of $G_{TF} >> G_{SF}$, G_{TF} is determined by J_{in}, J_V, and J_S. J_V is gas (vapor) phase diffusion flux from lateral direction, and J_S is surface diffusion flux on side facet.

$$G_{TF} \propto J_{in} + J_V + J_S$$

Therefore, growth rate in SA–growth is affected by diffusion of the growth species from masked region. In addition, the diffusion flux of desorbed growth species from masked region, J_D is partially contribute to the crystal growth as J_V, and the other species diffuse to out of boundary layer existing on the masked region, as J'_D shown in **Figure 3–6**. J_D is indicated by following equation,

$$J_D = J_V + J'_D,$$

where J_D highly depends on the growth temperature. In addition, χ_S is diffusion length of group–III species on the growth surface, and this is indicated below.

$$\chi_S = \sqrt{D_S \tau_S}$$

Here, τ_S is the life time of growth species at the growth surface, where the life time means resident time from the growth species are absorbed on growth surface to those are left from surface by the incorporation of growth species into the crystal or the desorption. In addition, D_S is surface diffusion factor, and this is determined by next equation,

$$D_S = a^2 \nu \exp\left(-\frac{E_S}{k_B T}\right),$$

where a is lattice constant, υ is oscillation frequency of absorption molecules and E_S is activation energy of surface diffusion. Consequently, smaller E_S and/or higher temperature result in larger D_S. We thus need to longer diffusion length of growth species (or precursors) to improve the flatness of grown surface in the SA–growth, because the growth species mainly diffuse from masked region to the opening area of surface. This is the reason why we use higher growth temperature in the SA–growth compared with the planar growth.

Another important point of the SA–growth is to avoid a deposition of poly–crystals on the masked region. Desorption of poly–crystals in dependent on J_{in} and τ. The τ is the life time of growth species (or precursors) on the masked region. Poly–crystals are preferentially deposited by longer τ, because the encounter probability of group–III species becomes higher for longer τ. On the other hand, τ can be shortened by increasing the probability of desorption of growth species under the higher growth temperature condition. Consequently, to suppress the deposition of poly–crystals on the masked region, we have to choose the growth condition with low J_{in} and short τ. In other words, we should carry out the crystal growth under the low working pressure and high growth temperature.

3.3.3 Physical Processes on Surface

At the surface during growth, adatoms (such as molecules and radicals) adsorb at the substrate, and inhomogeneously deposit at the surface. Adatoms incorporate into appropriate lattice positions at kinds or steps, or desorb into the vapor phase, while the species diffuse at the substrate surface. Desorbed species are transported away with the carrier gas.

The surface during growth has been thought to consist of atomically flat regions separated by steps, as shown schematically in **Figure 3–7**. Kossel model (Terrace–Step–Kink model) simply describes the thermodynamics of crystal surface formation and transformation. It is based upon the idea that the energy of an atom's position on a crystal surface is determined by its bonding to neighboring atoms and that stability involving the counting of bond formations. Thus, this model brings an intuitive understanding of the physical process on the surface structure.

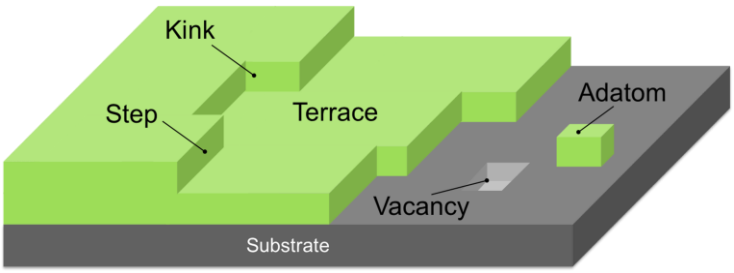

Figure 3–7
Schematic of arsenic–trimer coverage on GaAs (111)B surface.

3.4 Selective–Area MOVPE

3.4.1 Procedures of Selective–Area Growth

Selective–area MOVPE (SA–MOVPE) is one of the bottom–up approaches for crystal growth using partially masked substrate. The crystals of semiconductors can selectively be grown at the opening area of the substrate. To date, the micro– or nano–structures fabricated by SA–MOVPE has widely been used in a variety of applications, such as integration of waveguide with lasers and detectors [17], optical integrated circuit [18], and formation of hexagonal–facet double heterojunction laser structure [19].

Figure 3–8 shows the overview of fabrication procedures of semiconductor nanowires (NWs) by SA–MOVPE, and we briefly explain as follows. First, 10– or 20–nm–thick SiO_2 films are formed by radio frequency (RF) plasma sputtering system (ANELVA, L–250S–FH). Thickness of SiO_2 is verified by ellipsometry. After degreasing in acetone, ethanol, and ultrapure water in an ultrasonic bath, an electron–beam (EB) resist is coated on the surface of substrate by using spin–coater. In this work, ZEP520A7 (Nippon Zeon) are used as the EB resist. The thickness of coated ZEP520A7 is about 100 nm. After the spin–coat process, the substrates are pre–baked at 170 °C for 2 min and 90 °C for 10 min, and then, the samples are naturally cooled to room temperature preventing from surface crack of resist by thermal contraction.

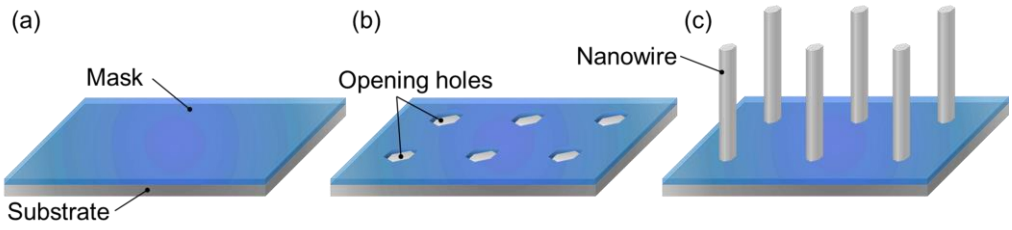

Figure 3–8

Overview of the fabrication procedures of semiconductor nanowires by SA–MOVPE. (a) Formation of the mask material (e.g., SiO_2) by using RF plasma sputtering system. (b) Fabrication of the opening holes by using electron–beam lithography (EBL), and wet or dry etching technique. (c) MOVPE growth for forming nanowires.

EB lithography system (JEOL, JBX–6300FS) with ZrO/W field emitter was used for making a fine opening pattern on the EB resist. The accelerating voltage is 100 kV. It has two objective lens systems, where one is the 4th lens mode and the other one is the 5th lens mode. 4th lens and 5th lens modes are basically used for making rough and fine pattern, respectively. In particular, 5th lens mode with beam current of 100 pA was used for patterning fine opening holes for NW growth with diameter of ~30 nm, because the EB spot size for this lens mode is very small and is about 2 nm. Typical area dose is about 150 μC/cm^2 for ZEP520A7 and 200 μC/cm^2 for ZEP520A. Here, exposure time can be described as follows,

$$t = \frac{R \times S^2 \times 0.01}{I},$$

where t (μsec) is exposure time, R (μC/cm^2) is resist sensitivity (or area dose), S (nm) is exposure interval, and I (pA) is beam current, respectively. Because the beam current for 4th lens mode is typically set to be 5 nA and this value is larger than that for 5th lens mode (100pA), exposure time can be shortened by using 4th lens mode and is suitable for roughly exposing large area pattern.

After EB exposure, substrates are developed with ZED–N50 for 60 sec and isopropyl alcohol (IPA, 2–propanol) is used for a rinse. And then, the substrate is post–baked at 120 °C for 2 min and cooled at room temperature. Then, exposed SiO_2 region was etched by using wet or dry etching technique. For wet etching, we used buffered hydrofluoric acid (BHF) solution (Hydrofluoric acid (HF): Ammonium fluoride (NH_4F) = 1:20), while for dry etching, we used reactive–ion etching (RIE) system with CF_4 gas etchant. After the etching, resist film is removed by using NN–dimethylacetamide.

Before loading samples to the chamber (or reactor), the samples are degreased in organic solvents in an ultrasonic bath and etched to remove a native oxide on the sample surface using Semicoclean (Furuuchi Chemical) with ultrasonic bath. Before the growth, the samples are thermally cleaned at certain temperature for 5 min under group–V precursor (or source) ambient which is material constituting of the substrate. For example, AsH_3 or TBP was used for thermal cleaning in this work, when the growth substrate was GaAs or InP, respectively.

3.5 Characterizations

The characterization of structural properties is particularly important so that reproducible relationships can be established between their desired functionality and their geometrical/structural characteristics. Due to their small size, it is not possible to use an ordinary light microscope, which has a resolution limited by the wavelength of the light. Instead of the light, accelerated electrons can be used as the illumination sources allowing the imaging of nm–scale objects. The scanning electron microscopy (SEM) was used for structural characterization of nanowires (NWs) in this work, and the explanation about SEM described briefly in this section.

In addition, the optical characterization of NWs is also important for understanding physical properties including their band–gap energy. The X–ray diffraction (XRD) analysis has frequently been used for the estimation of alloy composition of thin film semiconductors by obtaining the information of their lattice constant. However, the XRD is difficult to be adopted for the characterization of alloy composition of NWs, because the NWs has nano–scale geometry and typical spacing between the neighboring NWs is large and is from 200 nm to 5μm. On the other hand, the value of band–gap energy obtained by micro–photoluminescence (μ–PL) measurement gives us the information of alloy composition of InGaAs NWs easily. Thus, the explanation about μ–PL measurement is also described in this section.

3.5.1 Scanning Electron Microscopy

Scanning electron microscopy (SEM) is a commonly used tool to characterize and to quickly identify the grown NWs or other small objects that are too small to be observed in normal optical microscopy. The spatial resolution is generally much higher in an SEM as compared with a state–of–the–art optical microscope, because the wavelength of the electrons for typical acceleration voltages used in the SEM is significantly shorter than that of visible light. A simple schematic illustration of an SEM is depicted in **Figure 3–9(a)**. Basically, it consists of an electron column with an electron source, condenser lenses, aperture, scanning coils, an objective lens, and a specimen chamber. It is important to have high vacuum in the

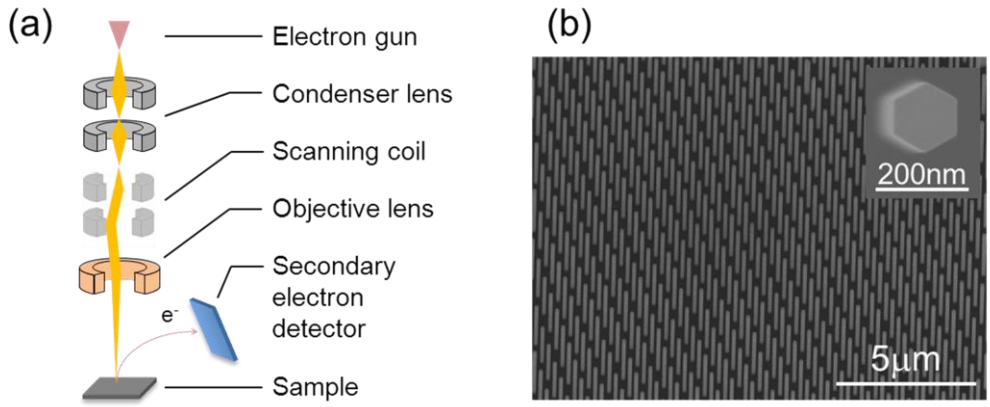

Figure 3–9

(a) Schematic illustrations of Scanning Electron Microscopy (SEM). (b) Typical SEM image of InGaAs nanowires grown by SA–MOVPE (45°–tilted). The inset of (b) is the image of top of a nanowire (0°–tilted).

electron column to prevent electrical discharge, prolong the electron source lifetime and reduce unwanted collisions between electrons and air molecules, leading to scattering along the path to the sample. The electron beam trajectory and focus are further controlled by a set of magnetic condenser lenses, which focal length is controlled by varying the current through the coil. When the electron beam hits the sample, it creates a certain excitation volume. Depending on the acceleration voltage and the atomic density of the specimen, the electron beam will penetrate the sample to different depths. For instance, a higher voltage (lower density) will increase the excitation penetration depth. The electrons are also scattered from their original trajectories leading to a three–dimensional excitation volume.

The image is generated by scanning the beam over the sample and presenting the signal on a separate screen. Typical image of nanostructures (InGaAs NWs) obtained by SEM is shown in **Figure 3–9(b)**. The magnification is given by the ratio between the area of the screen and the area of the sample being scanned. By scanning shorter lines on the sample, the magnification increases. The interaction between the electron beam and the sample will result in different kind of signals used for detection. The electrons will interact elastically and inelastically with a sample, generating primary (such as backscattered) and secondary electrons

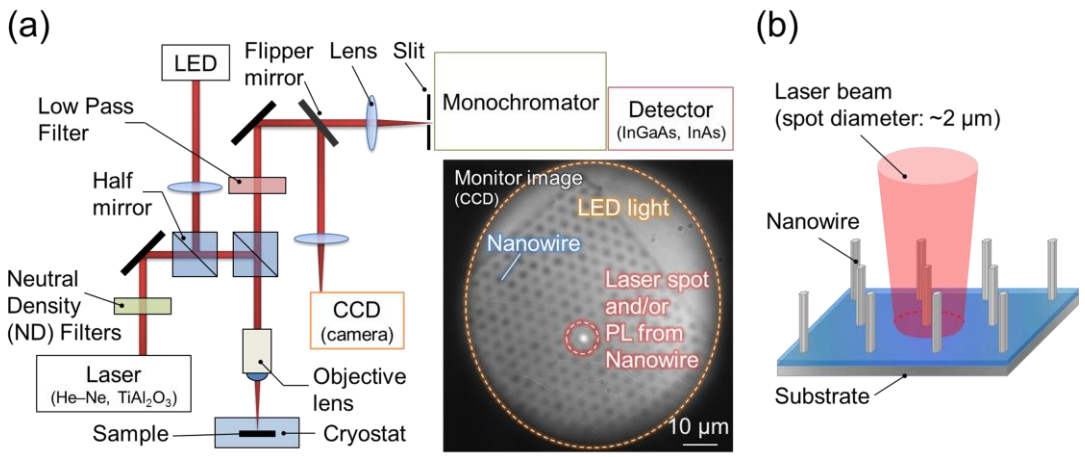

Figure 3–10

Schematic illustrations of (a) PL measurement system and (b) a substrate with nanowires excited by a laser beam focused to about 2 μm in diameter during PL measurements.

(such as secondary and auger electrons), respectively. The backscattered electrons are affected by the vicinity of a nucleus, hence altering its trajectory but without losing much velocity. Some of these electrons are scattered back towards the electron source (backscattered electrons), and can be detected by a detector above the sample. The probability for scattering increases with atomic number, and lager fraction is scattered by a heavier element. These electrons, consequently, contain the information about the sample composition (atomic number contrast). The secondary electrons are created after the collisions with a nucleus, which typically are sample response signals that most commonly used for the detection in SEM. These electrons contain topographical information, as they are typically emitted from a depth of a few tens of nanometers. A practical limit for the SEM used in this work is about 10 nm. The SEM provides valuable information about the appearance shape, structural arrangement, surface morphology, and geometrical features of the NWs.

3.5.2 Micro–Photoluminescence

The micro–photoluminescence (μ–PL) measurement was carried out to analyze the optical properties of the NWs at the sample temperature of 4.2 K. Typical PL measurement

system is illustrated in **Figure 3–10(a)**. Two kinds of lasers were used as the excitation source in this work. The $TiAl_2O_3$ laser operating at 773 nm pumped by Nd: YVO_4 laser was used for analyzing indium–rich $In_{1-x}Ga_xAs$ NWs ($x < 0.5$), while He–Ne laser operating at 632.8 nm was used for analyzing gallium–rich $In_{1-x}Ga_xAs$ NWs ($x > 0.5$). The laser lights were focused to 10 μm and 2 μm in diameter by objective lens for the former and latter cases, respectively. We can measure PL from single NW or bundles of them depending on the mask pitch (i.e., the mask pitch is wider or narrower than the diameter of laser light spot) as shown in **Figure 3–10(b)**. The charge–coupled–device (CCD) camera and light–emitting–diode (LED) were used to confirm the position of NWs, and typical monitored image is shown in inset of **Figure 3–10(a)**. When we begin the PL measurement, flipper mirror was removed to open the optical pass to the detector and LED was turned off. Then, the low pass filter was inserted to cut the reflected light of excitation laser. The PL from NW samples was guided into a monochromator and detected with two kinds of photodiodes. We used 77–K–cooled InAs photovoltaic device and InGaAs photodiode for analyzing indium–rich InGaAs and gallium–rich InGaAs NWs, respectively.

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Chapter 4

Selective–Area Growth of GaAs, InAs, and InGaAs Nanowires

4.1 Introduction

This chapter reviews the features of the growth behaviors of GaAs, InAs, and InGaAs nanowires (NWs) in selective–area metal–organic vapor–phase epitaxy (SA–MOVPE). This thesis explains composition–dependent growth dynamics of InGaAs NWs in SA–MOVPE in chapter 5, 6. Because InGaAs is an alloy between GaAs and InAs, the knowledge on the growth properties of selectively–grown GaAs and InAs NWs is especially important to understand the growth dynamics of InGaAs NWs in SA–MOVPE. In particular, effects of growth temperature (T_G) and V/III ratio in selective–area growth of GaAs and InAs NWs exhibited inherent dissimilarities [1]–[6], which is thought to be due to the inherent difference between GaAs and InAs in binding energy, lattice constant, surface energy of the growth surface, and so on [7].

Selective–area growth of GaAs, InAs and InGaAs NWs has previously been reported by our group. The semiconductor NWs are attracted much research interest for building blocks of novel device applications, such as field–effect transistor (FETs), solar cells, lasers, and so on, because of their unique electrical and optical properties [8]–[16]. In particular, the GaAs, InAs, and InGaAs NWs are expected having superior material properties. The physical properties of bulk or thin film GaAs, InAs, and InGaAs are shown in **Table 4–1**. Both bulk GaAs and InAs have direct band gap covering infrared range, and higher electron mobility. These properties are superior to those of Si, where Si has indirect band–gap and lower electron mobility. Thus the GaAs and InAs NWs are promising for use in optical and electrical devices. As for InGaAs NWs, it is also expected higher electron mobility than that of Si and direct band gap covering

	Crystal Structure	Lattice Constant (Å)	Energy Gap (eV)	Electron Mobility (cm^2/Vs)
GaAs	Zincblende	5.65325	1.424 (D)	8500
InAs	Zincblende	6.0583	0.354 (D)	40000
$In_{0.53}Ga_{0.47}As$	Zincblende	5.8687	0.74 (D)	12000
InP	Zincblende	5.8687	1.344 (D)	5400
Si	Diamond	5.431	1.12 (ID)	1400

Table 4–1

Physical properties of GaAs, InAs, $In_{0.53}Ga_{0.47}As$, InP and Si in bulk. “D” and “ID” represent direct transition and indirect transition, respectively. [17]

infrared and telecommunication range (Wavelength: λ = 1.3, 1.55 μm). Conventionally, InGaAs thin films are grown on InP substrate, because the lattice mismatch between $In_{0.53}Ga_{0.47}As$ and InP is very small. In addition, the growth of InGaAs thin films having other alloy composition ($In_{1-x}Ga_xAs$, $x \neq 0.53$) is difficult to obtain with high crystal quality, because its lattice constant change depending on its alloy composition, resulting in large lattice mismatch between InGaAs and substrate. On the other hand, for the NW growth, alloy composition of InGaAs can continuously be controlled without any dislocations, owing to their quite small footprints [18].

In this chapter, we firstly describe about selective–area growth of GaAs NWs. To date, by the detailed characterizations of growth properties of GaAs NWs in SA–MOVPE [1][2], it has been clarified that fundamental properties of the NW–growth in SA–MOVPE can be explained by the faceting growth model and the twining growth model. These models become to be most famous NW growth model among researchers studying NW growth and NW–based applications in the world. Therefore, first of **Section 1.3**, we describe about these growth model of NWs. Following them, we summarize and discuss the effects of growth temperature, V/III ratio, and mask pitch in the selective–area growth (SAG) of GaAs NWs.

In **Section 4.3**, we describe about selective–area growth of InAs NWs. In particular, the effects of growth temperature and V/III ratio in selective–area growth of InAs NWs are explained in detail [4]. In addition, crystal structure and twining frequency is also discussed.

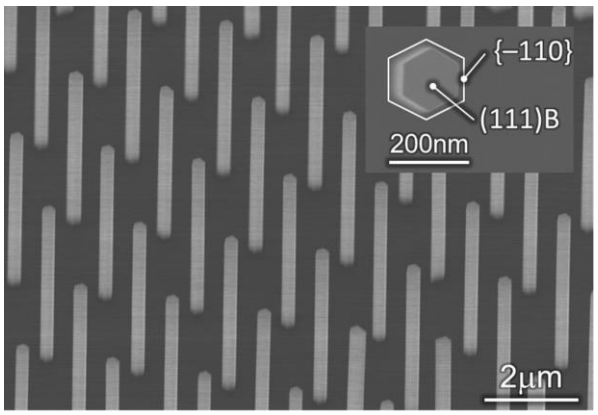

Figure 4–1

Typical SEM image of selectively–grown InGaAs nanowires on (111)B–oriented substrate. Inset shows the top view of a nanowire.

In **Section 4.4**, we describe about the growth of InGaAs NWs in SA–MOVPE. First of this section, we explained about the time evolution of InGaAs NWs based on the diffusion equation. Following them, we show the effects of group–III supply ratio, growth temperature (for gallium–rich InGaAs NWs), and geometry of mask openings in the selective–area growth of InGaAs NWs. Differently from GaAs and InAs NWs, simultaneous control of NW diameter, NW height and alloy composition of NWs are critical issue for realizing application of InGaAs NWs to various kinds of electrical/optical devices. Because it was found that the group–III supply ratio, growth temperature, and mask geometry clearly affect the NW size and alloy composition [19]–[21], we describe about these effects. We think that the knowledge of these effects on NW size and alloy composition is important to understand the results and discussion of **Chapter 5**, **6**, and **7** of this thesis. Finally, we show the characterization of crystal structure of InGaAs NWs [22].

The GaAs, InAs, and InGaAs NWs reviewed in this chapter are selectively grown with high uniformity of their size and geometry, as shown in **Figure 4–1**, unless otherwise specified. In addition, all of such highly uniform GaAs, InAs, and InGaAs NWs are consisted of (111)B NW–top facet and six {–110} NW–side facets normal to (111)B.

4.2 Selective–Area Growth of GaAs Nanowires

4.2.1 Faceting Growth for Selectively–Grown Nanowires

This section explains the faceting growth of GaAs nanowires (NWs) in selective–area metal–organic vapor–phase epitaxy (SA–MOVPE). The growth mechanism of SA–MOVPE is in formation of facet during growth, and this fact is now well known in the world. However, until K. Ikejiri *et al*. has reported on this issue [1], some claim that it is not possible to rule out the catalyst– or oxide–assisted mechanism for the preferential growth in one direction. Namely, the nanowire growth modes and their mechanisms in SA–MOVPE have been controversial. Thus, K. Ikejiri *et al*. investigated the mechanism of growth of nanowires by SA–MOVPE [1]. The dependence of SA–growth mode on the substrate orientation and growth conditions was studied and it was found that the NWs were formed only in a limited combination of growth conditions and substrate orientations, which identifies clearly that the formation of NWs solely relied on the formation of facets during SA–MOVPE.

The SA–MOVPE of GaAs NWs was carried out on GaAs (111)B substrate partially covered with SiO_2 film. The source materials were trimethylgallium (TMGa) and arsine (AsH_3). The growth time was 40 min. Two kinds of growth conditions were used in this experiment to investigate growth condition dependence. In the growth condition–A, growth temperature, T_G, and partial pressure of AsH_3, [AsH_3], were 750 °C and 5.0×10^{-4} atm, respectively, and this condition was called as high T_G and low [AsH_3] condition in this report. Also this is a standard growth condition for the growth of GaAs NWs on (111)B substrates. For the growth condition–B, GaAs were grown at 600 °C and 1.0×10^{-3} atm, respectively, and this condition was called as low T_G and high [AsH_3] condition in this report. The partial pressure of TMGa was 2.7×10^{-6} atm for both conditions.

Upper left SEM image in **Figure 4–2** shows typical GaAs NWs grown on (111)B substrates with the growth condition– A. Array of uniformly sized NWs were formed. Note that NWs have hexagonal cross–section. The sidewalls of the NWs are confirmed to be {–110} facets vertical to (111)B based on the relative directions of the sidewalls and substrates. Results of the SA–growth carried out on the substrates with different orientations and under different

growth conditions are summarized in **Figure 4–2**. The NW structures were formed only on (111)B substrate with growth condition–A. These experimental data clearly indicate that the mechanism of NW growth in SA–MOVPE is neither catalyst– nor oxide–assisted but is the formation of facet sidewalls that have slower growth rates than that on (111)B. These results were examined in detail below. Firstly, the dependence of the substrate orientation was focused on. In the case of NWs in VLS mechanism, the NWs tend to grow in some particular direction, for instance, in the <–1–1–1> direction for III–V compound semiconductor NWs. Therefore, the NWs are vertical or tilted to the substrates if the substrate is (111)B or (001), respectively. For GaAs NWs by oxide–assisted mechanism, the preferential growth direction is also in the <–1–1–1>. In any case, it could be expected to obtain NWs in the particular (namely, in the <–1–1–1>) direction independent of the orientation of the substrates if the catalysts or oxides would play a role. This clearly is not this case, identifying the absence of catalyst– or oxide–assisted mechanisms in SA–MOVPE.

As shown in **Figure 4–2**, grown structures on (001) and (311)B substrates exhibited pyramidal–like structures and surrounded clear crystallographic facets. Theses facets are assigned to be {–110}, (111)A and (111)B surfaces from the orientation of the substrates and the

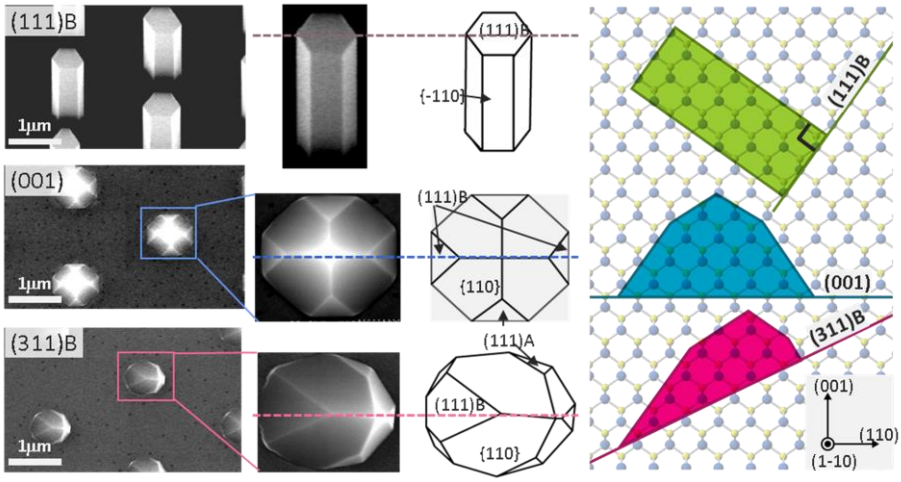

Figure 4–2

Faceting growth of GaAs on GaAs (111)B, (001), and (311)B substrate for condition–A.

angle between each facet and substrates, as schematically shown in the middle of **Figure 4–2** We obtained almost the same index facets on both (001) and (311)B. Note, generally in selective–area or patterned–area growth, that a facet appears because the growth stops or the growth rate is quite slow in that particular orientation of the surface. In the case of (001) or (311)B, the growth rate on {–110}, (111)A, and (111)B is much lower than that on (001) and (311)B. In addition, very little growth occurred and flat (–110) surface is obtained in the case of SA–MOVPE on (110) surface. Thus, the results indicate clearly that {–110} facets preferentially appear during GaAs growth on any substrate orientation in the present growth condition–A (high T_G and low [AsH_3] condition). Therefore, it is concluded that the NWs on (111)B are obtained with faceted {–110} surfaces.

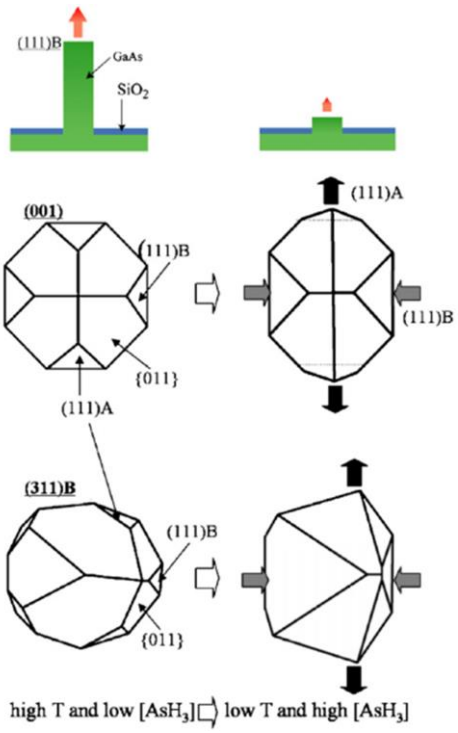

Figure 4–3

Schematic illustrations of grown structures on (111)B, (001) and (311)B under high growth temperature and low partial pressure of AsH_3, [AsH_3] (or low V/III ratio) condition, left) and low growth temperature and high V/III ratio condition, right).

Formation of the facets was further confirmed by the dependence on growth conditions. Particularly for the growth on (111)B–oriented substrate, the growth is considerably suppressed for condition–B as shown in **Figure 4–3**. It is well known that, under this condition where effective coverage of arsenic is high, arsenic overlayer attaches onto the arsenic–terminated (111)B surface to form stable arsenic–trimers as shown in **Figure 4–4** [23][24]. Because they prevent growth from proceeding on the (111)B surface, the growth rate becomes low. Similar suppression of the growth in (111)B surface was also observed on the structures grown on (001) and (311)B partially masked substrates, in which the areas of (111)B facet were enlarged, as schematically shown in **Figure 4–3**. The increase of the growth rate on (111)A facet was also observed, and as a result, (111)A facets disappeared from the growth structures, as shown in **Figure 4–3** On the (110) substrate, the growth towards the <–110> direction was enhanced for condition–B. These enhancements of the growth on the (111)A and {–110} surfaces can be explained by the increase of available gallium sites at high arsenic coverage, or the low T_G and high [AsH_3]. These results on growth condition dependence indicate that the growth mechanism of GaAs nanowires by SA–MOVPE is attributable to the formation of specific low–index facets and those growth rates depend strongly on the growth conditions.

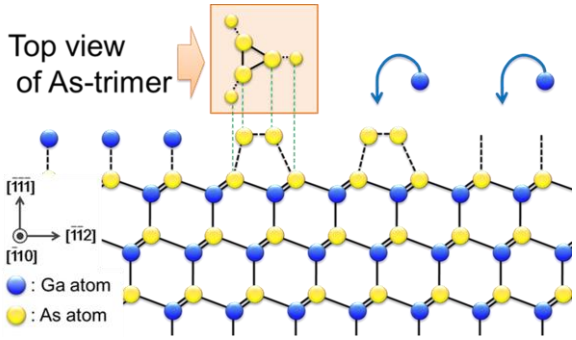

Figure 4–4

Schematic of arsenic–trimer coverage on GaAs (111)B surface.

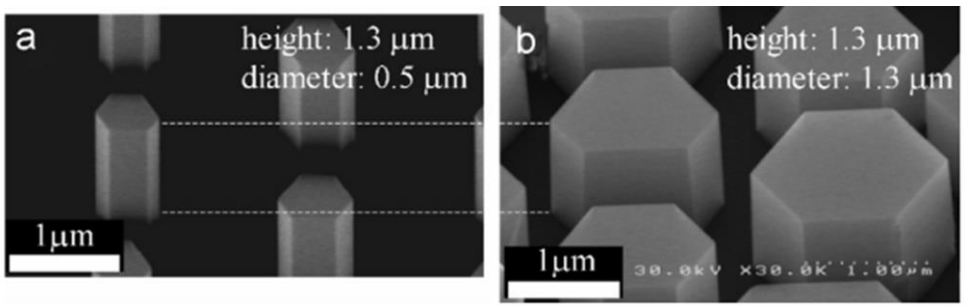

Figure 4–5

SEM images of selectively grown GaAs on GaAs (111)B substrate with first step (a) condition–A and second step (b) condtion–B.

Finally, GaAs was grown with condition–A for 40 min, and successively grew with condition–B for 20 min. Results of growth are summarized in **Figure 4–5**. The height and the diameter of GaAs nanowires were 1.3 and 0.5 μm, respectively, after the first GaAs growth. However, their diameter became 1.3 μm after the second GaAs growth, while their height was maintained. This result further confirms that GaAs grew only on (111)B under the high T_G and low [AsH_3], and only on {–110} under the low T_G and high [AsH_3], and the importance of the formation of facets during SA–MOVPE. This controllability of the growth mode is promising for the formation nanowires with of complex structures, such as core–shell heterostructures or *pn* junctions.

4.2.2 Twining Growth Model

In this section, we explain the twinning growth model for NW growth in SA–MOVPE. This model was proposed by K. Ikejiri *et al*. [2], and is well known as fundamental growth model for NW growth in SA–MOVPE. The SA–MOVPE of GaAs NWs was carried out on GaAs (111)B substrate partially covered with SiO_2 film. The source materials were trimethylgallium (TMGa) and arsine (AsH_3). The partial pressure of AsH_3, [AsH_3], TMGa, [TMGa], were 5.0×10^{-4} and 2.7×10^{-6} atm, respectively.

SEM images of the substrate surface taken for 10 min of growth temperature at 750 °C with a mask window (opening) diameter of 1 μm and mask pitch of 2 μm are shown in **Figure 4–6**. The grown GaAs seems to have an intermediate shape between tetrahedral and hexagonal and clearly indicates three–fold–symmetry facets, as identified from the SEM images in **Figure 4–6**. It can be seen that the direction of the crystal corner is either along <11–2> or <–1–12>. The result is very similar to that observed for the tetrahedral GaAs crystals grown using a window diameter of 100 nm (not shown here, but it is shown in Ref. [2]).

TEM images and an electron diffraction pattern of a GaAs NW grown at 700 °C are

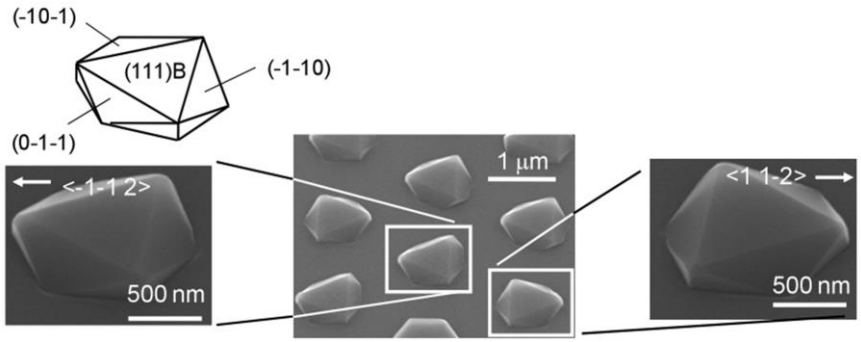

Figure 4–6

SEM images of GaAs substrate surface after MOVPE for a growth time of 10 min at 750 °C. The mask window diameter was 1 μm and mask pitch was 2 μm. The schematic picture of the polygon in the upper left depicts three–fold–symmetry facets (–1–10), (–10–1), and (0–1–1) corresponding to the grown crystal shown in the enlarged SEM image below.

shown in **Figure 4–7**. The images indicate that the NW width was about 185 nm but it had a tapered shape with the smallest width of 105 nm at the base. This indicates lateral overgrowth of GaAs onto the SiO_2 masked area during MOVPE. **Figure 4–7(b)** reveals twin boundaries (indicated by arrows on the TEM image) perpendicular to the <–1–1–1> direction identified as anti–symmetry layers in the lattice image. The twin structure of zincblende (ZB) was also confirmed by the electron diffraction pattern shown in **Figure 4–7(c)**. The single–crystal layer sandwiched between the neighboring twin boundaries was from as thin as a few monolayers (MLs) up to 20 MLs, as counted in the TEM image of **Figure 4–7(b)**.

A hypothetical growth model of how the GaAs shape changes from triangular to hexagonal in an early growth stage is shown in **Figure 4–8**. SEM images posted above or next the drawings (denoted (a), (b), (c), and (f)) correspond to the crystal shapes for the respective stages. At growth stage (a), the crystal shows an inverse mesa shape. The inverse mesas have a high growth rate in the lateral three–fold symmetrical directions of <11–2>, <1–21>, and <–211>. The triangular crystal grows into a hexagonal base (b) and then grows thicker to stage (c).

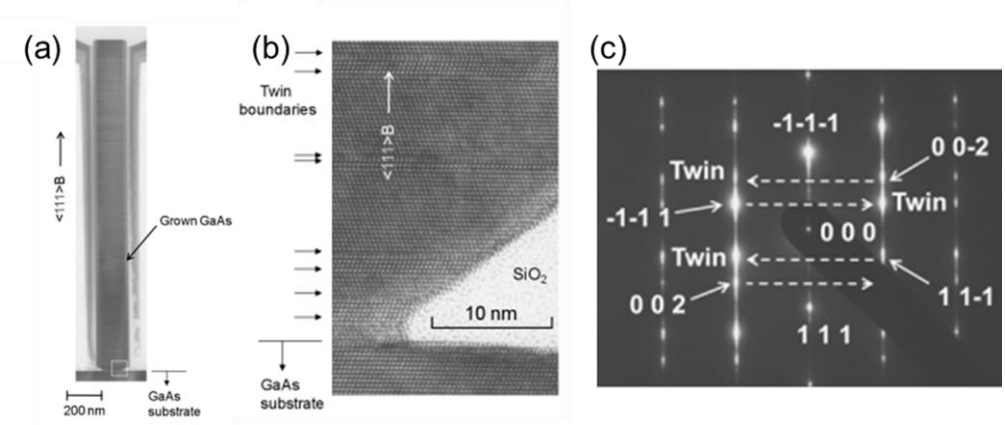

Figure 4–7

Transmission electron microscope images and an electron diffraction pattern of a GaAs nanowire grown at 700 °C at a SiO_2 mask opening. The incident electron beam was normal to the (1–10) facet. (a) Whole image of the nanowire. (b) Enlarged image of an open square near the nanowire base shown in (a). (c) Transmission electron diffraction pattern of nanowire.

A twin plane develops on the triangular (111)B top surface at stage (d). In this way, three inverse mesa facets are formed and fast lateral growth is again promoted towards the three–fold–symmetry directions of <–1–12>, <–12–1>, and <2–1–1>, as schematically depicted in (d)–(f). When stage (f) is reached, the next twin develops at stage (g). Thus, a hexagon pillar grows along the <–1–1–1> direction by piling up twins one after another. This model is the twinning growth model for SA–grown NWs proposed by K. Ikejiri *et al*., and further detailed explanations about this model are described in elsewhere [25]. This model is backed up with the comparison of Gibbs free energy change of nucleation between tetrahedron and hexagons. Change in Gibbs free energy for nucleation growth of tetrahedrons is lower than that of hexagons, and this fact strongly supports the proposed twining growth model. This model can also be adapt to the growth of InAs and InGaAs NWs in SA–MOVPE, and it has been extended to understand the growth mechanism of InP NWs [26][27], and further extension is expected.

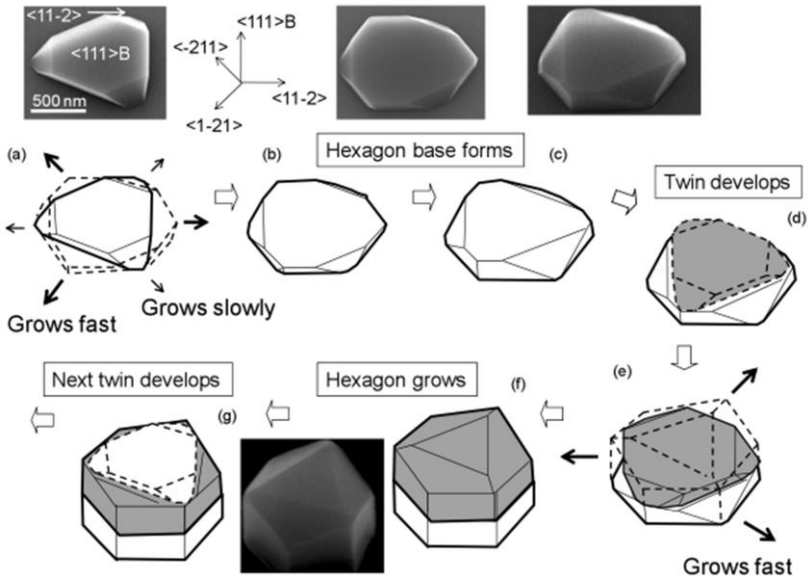

Figure 4–8

Estimated evolution of a GaAs hexagon featuring lateral growth and twin development from a triangular crystal. Drawings (a)–(g) partly connected with SEM images depict how the crystal shape changed during growth. Crystal twins are shaded grey and white, for clarity.

4.2.3 Effects of Growth Temperature for GaAs Nanowires

In this section, we explain about the effects of growth temperature for GaAs NWs. K. Ikejiri *et al.* has reported that the growth temperature dependence of NW height as shown in **Figure 4–9**, and found that the NW height decreases as the growth temperature increases [2]. It is probably because the desorption of atoms or growth species from NW top (111)B facet. However, the effect of growth temperature in lower growth temperature than 700 °C has not been reported. We investigated, therefore, the growth behavior and growth rate of GaAs NWs in growth temperature of 650 °C, and found that the growth rate increases to a certain maximum, then decreases as the growth temperature increases.

Figure 4–10(a) shows SEM image GaAs NWs grown at 650 °C (opening diameter, d_0 = 200 nm, and mask pitch, a = 2 μm). Hillock like growth and thin/flat hexagonal shapes were observed. Nevertheless, the NW growth could be obtained and NW height, h, is plotted as a function of NW diameter, d, as shown in **Figure 4–10(b)**. We assumed that the value of NW diameter corresponds to that of opening diameter. Red closed squares represent the measured value of h for $d \cong$ 200 and 300 nm, and a = 2 μm. These values are similar to that of fitting line proportioning to 1/d, and this fact corresponds to the result of Ref. [2], where the source supply from NW side surface greatly contributes to the NW growth. From the value of average NW height for $d \cong$ 200 nm, we obtained growth temperature dependence of axial growth rate of

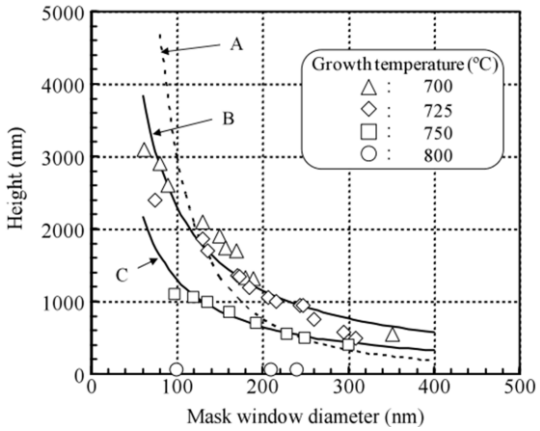

Figure 4–9

GaAs nanowire height as a function of mask window (opening) diameter d_0. (a = 2 μm)

NWs, as shown in **Figure 4–11**. It was found that the growth rate increases to a certain maximum, for lower temperature range (< 700 °C). It is probably because the incorporation of gallium atoms hindered by arsenic–trimer coverage on GaAs (111)B NW top facets [23][24].

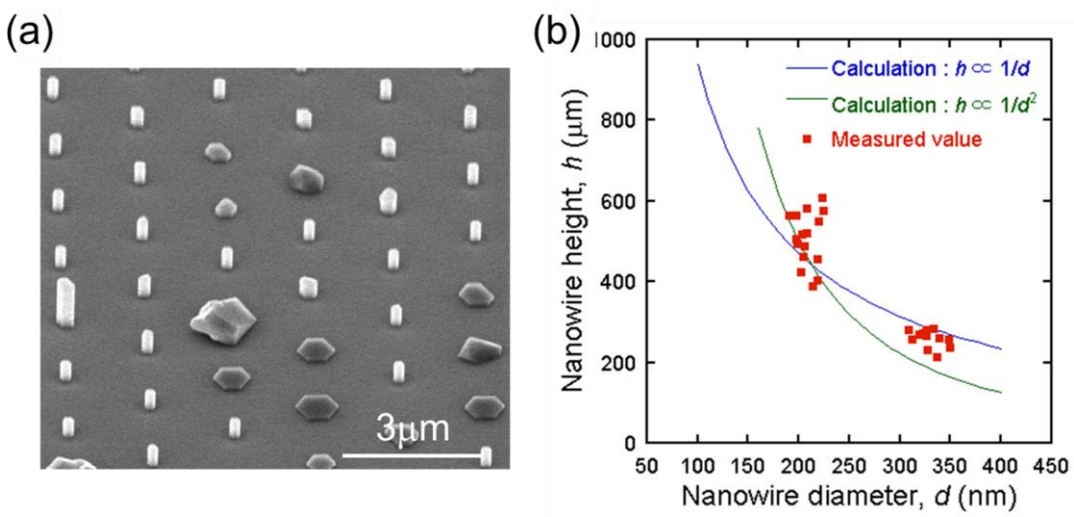

Figure 4–10

(a) SEM image of GaAs nanowires at growth temperature of 650 °C (d_0 = 200 nm, and a = 2 μm). (b) Nanowire diameter, d, versus nanowire height, h. The blue line and green line represent calculated values for h proportional to $1/d$ and $1/d^2$, respectively. Red closed square represents measured value of h and d of GaAs nanowires.

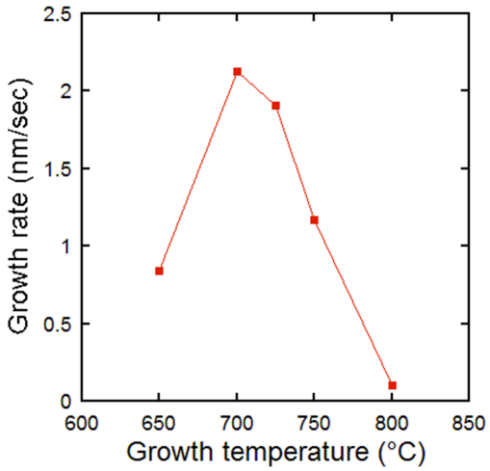

Figure 4–11

Growth temperature dependence of axial growth rate of nanowires.

4.2.4 Effects of V/III Ratio for GaAs Nanowires

This section explains the effects of V/III ratio on the growth of GaAs NWs. J. Noborisaka *et al.* has reported the V/III ratio dependence of NW height, *h* [3]. **Figure 4–12** shows a diameter and pitch dependence of *h* for various partial pressures of AsH_3 (V/III ratio). J. Noborisaka *et al.* assumed that the value of NW diameter corresponds to that of opening diameter. Within the used growth conditions, where the growth temperature was relatively high and V/III ratio was low, as compared to the ordinary GaAs growth conditions, we expected that the growth rate on (111)B would be much higher than that on a (–110) surface. This is because adsorbed Ga atoms do not have strong bonding on a (–110) surface for small arsenic coverage, and they can desorb very easily. In fact, according to SEM study, almost no lateral growth over the SiO_2 mask was observed, indicating that there is almost no growth on (–110) vertical surfaces and thus $d \sim d_0$. Formation of hexagonal structures, therefore, was explained by the six–fold symmetry of the (111)B–oriented surface and the fact that (–110) vertical facets exhibited the slowest growth rate. In addition, it was found that *h* decreased with increasing V/III ratio. This growth behavior could qualitatively be explained by the surface reconstruction of (111)B GaAs surfaces [23][24]. That is, when the V/III ratio is high, the growth of the (111)B surface is suppressed by the formation of stable arsenic–trimers, whereas they become less stable at lower V/III ratio, resulting in an increase in the growth rate.

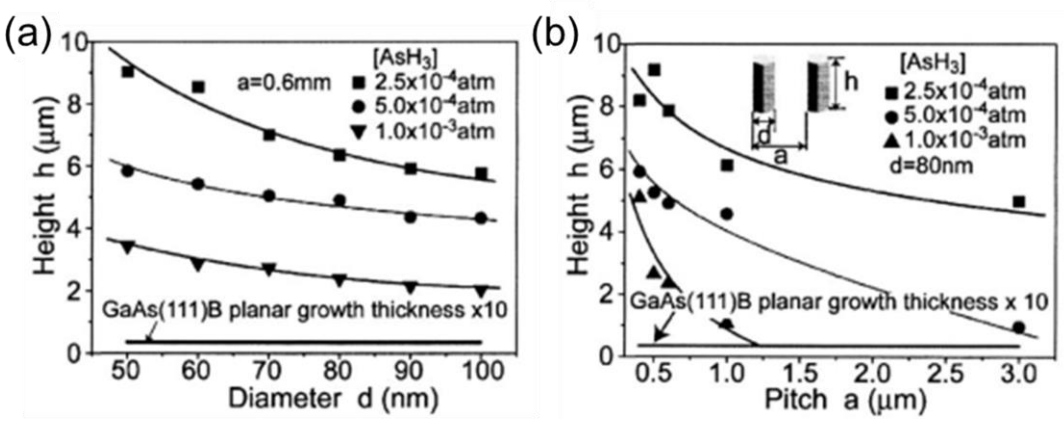

Figure 4–12

Height, *h*, of GaAs nanowires versus (a) nanowire diameter, *d*, and (b) mask pitch, *a*.

4.2.5 Effects of Mask Pitch for GaAs Nanowires

Next, we explain the effects of mask pitch for GaAs NW growth. In **Figure 4–13(b)**, NW height, *h*, increased with decreasing the value of mask pitch. This enhancement of the growth rate on patterned substrates and the dependence of *h* on the pattern geometry (*a* and d_0) cannot be explained in the simple model. To examine the growth rate enhancement in more detail, J. Noborisaka *et al.* plotted in **Figure 4–13** the calculated total volume V_2 of the nanowires in a unit cell of the triangular lattice on a patterned substrate normalized by the volume V_1 of a planar growth in the same area. The area of the unit cell is given by a^2 and the cross–sectional area of hexagonal nanowires is given by d^2. The ratio V_2 /V_1 is therefore calculated as $(d/a)^2(h/h_p)$, where h_p is the growth thickness on a planar substrate and is 42 nm. J. Noborisaka *et al.* could see a significant increase in V_2/V_1 as *a* becomes smaller. Note that V_2/V_1 should go to 1.0 in the limit $a \rightarrow 0$, though it looks unlikely at first sight within the present experimental results. In the case of SA–MOVPE on a (100) GaAs surface, the enhancement of the growth rate in the opening region of the mask is generally observed. This is explained by the gas–phase and/or surface diffusion of the growth species from the masked to opening regions. This enhancement is known to be dependent on the pattern geometry, and in the present case where the patterned area is limited to 100×100 μm regions, J. Noborisaka *et al.*showed that the enhancement was only about 20 to 30% of the planar growth rate [28][29]. If we take into

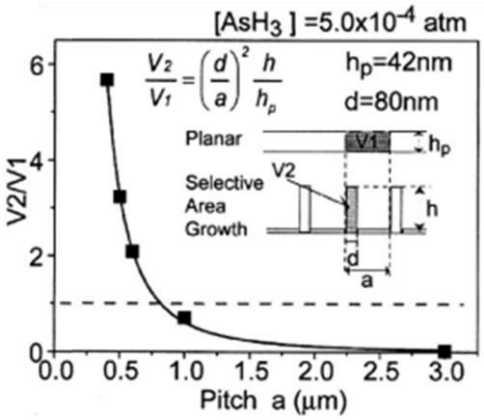

Figure 4–13

Volume ratio V_2/V_1 of GaAs grown on patterned and planar substrates in a unit cell of the triangular lattice. Growth volume V_1 is for the planar and V_2 is for the nanowires, as shown in the inset.

account the fraction f of the mask opening [in the present case, $(d_0/a)^2$] in the patterned regions, the growth rate increases slightly as f is reduced, as expected from the diffusion of growth species. Nevertheless, the ratio V_2 /V_1 of the total growth amount between the patterned and planar growth does not exceed unity as reported in Ref. [30]. That is, the total amount of growth is always smaller on patterned substrates than on planar substrates, indicating that the thermal decomposition of the column III precursor is effectively decreased in the patterned area or a considerable amount of the growth species diffuse out to the exposed regions surrounding the patterned regions. This simple gas–phase/surface diffusion model can partly explain our present results. As in **Figure 4–12(a)**, h increases as f decreases. This simple model, however, completely contradicts the results of **Figure 4–12(b)** and **Figure 4–13**. To get more insight for the growth process of the NWs, J. Noborisaka *et al*. considered diffusion processes in and between three different regions, namely, (111)B top surface, (–110) sidewall facets, and masked areas, as shown in **Figure 4–14**. In this model, J. Noborisaka *et al*. assume the following diffusion equation for the concentration N of growth species on the surface in each region and that the growth proceeds by the incorporation of species into the crystal phase:

$$-\frac{d}{dx}\left(D\frac{dN}{dx}\right) = J - \frac{N}{\tau}.$$

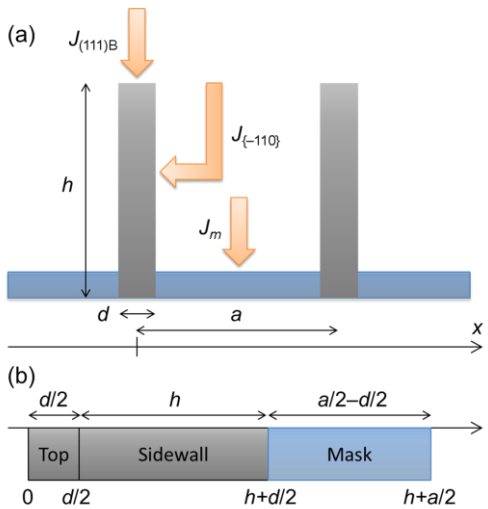

Figure 4–14

(a) Diffusion model for the nanowire growth in SA–MOVPE. (b) Two–dimensional developed figure of (a).

Here, D is the surface diffusion constant, $1/\tau = 1/\tau' + 1/\tau''$, where τ' is the incorporation time, τ'' is the re–evaporation time of species, and J is the impinging flux of growth species from the vapor phase. It is also assumed that a complicated interplay of gas–phase diffusion can be considered within effective flux J. All of these parameters are defined in each of the three regions [J. Noborisaka *et al*. use subscript (111)B, {–110}, and *m* for their distinction], and the continuity of the flux at the boundary of different regions is used as the boundary condition. Then, the growth rate is proportional to $N\tau'$. The conclusion of this model is that the dominant factor of diffusion between different regions is $J\tau$, which is exactly the surface concentration of the growth species and is readily acceptable if one thinks of the nature of diffusion. Thus, if three regions considered here take a different $J\tau$, there could be diffusion between (111)B and {–110} surfaces, {–110} surfaces or masked regions, as usually seen in SA–MOVPE. If we assume $d << L_{(111)B}$, where $L_{(111)B} = \sqrt{D_{(111)B}\tau_{(111)B}}$ is the diffusion length and is thought to be in the order of a few microns, and no incorporation into the crystal phase in {–110} and masked region (that is, $\tau'_{\{-110\}}$, and τ'_m, are infinite), J. Noborisaka *et al*. find that the most relevant parameters are, $J_{\{-110\}}\tau''_{\{-110\}}$, $J_m\tau''_m$, and $J_{\{-110\}}J''_{\{-110\}} \ll J_m J''_m$. Note here that, if these parameters are independent of the period *a* of the mask pattern and size *d* and *h* of nanowires, J. Noborisaka *et al*. end up with the conventional model of SA–MOVPE mentioned earlier, and we cannot explain the anomalous enhancement of the growth rate and diffusion. Thus, to explain the experimental data, we have to think $J_{\{-110\}}J''_{\{-110\}}$ to be increased, or $J_m J''_m$ to be decreased as *a* is decreased: In fact, there are several possibilities. If the species once desorbed from the masked area are reabsorbed on {–110} surfaces, particularly, in dense pillar arrays, this gives additional contribution to $J_{\{-110\}}$. It is also possible that τ_m is effectively shortened when *a* is reduced, since the species diffusing or migrating on the mask can easily find the NWs to be incorporated.

4.3 Selective–Area Growth of InAs Nanowires

4.3.1 Effects of Growth Temperature for InAs Nanowires

This section explains the effects of growth temperature for the growth of InAs NWs. K. Tomioka *et al*. has reported that the effects of growth temperature [4]. **Figure 4–15(a)** and **(b)** shows SEM images for InAs NWs grown under optimum growth condition, where the growth temperature and V/III ratio were 540 °C and 265, respectively. Highly uniform NWs were observed and the size of their diameter was same as that of mask opening. NW diameter, *d*, and NW height, *h*, were 100 nm and 1.5 μm, respectively, in **Figure 4–15(a)**. In **Figure 4–15(b)**, we can see thinner (~50 nm) and longer (~5 μm) NWs, which was achieved by reducing the size of mask openings. The NWs were composed of six vertical {–110} facets and (111)B plane, as in the case of SA–MOVPE of GaAs NWs on GaAs (111)B substrate.

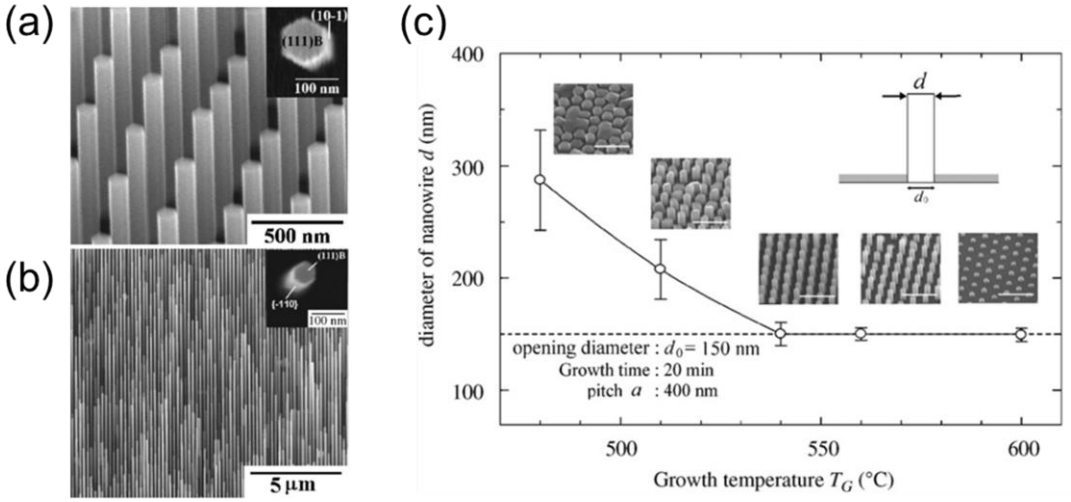

Figure 4–15

(a), (b) 45°–tilted SEM images for InAs nanowires, the insets show a top view of a nanowire. (c) Temperature dependence of InAs nanowire growth, where diameter of the nanowires, *d*, is plotted as a function of growth temperature, T_G. The diameter of the mask openings (see inset), d_0, is 150 nm. P_{TMIn} (partial pressure of TMIn) is 4.87×10^{-7} atm and P_{AsH3} (partial pressure of AsH_3) is 1.3×10^{-4} atm. The scale bars for inset SEM images are 1 μm.

Figure 4–15(c) and **Figure 4–16** show growth temperature dependence of *d* and axial growth rate of NWs for V/III ratio of 265, SEM images in **Figure 4–15(c)** is grown InAs for each growth temperature, T_G. The opening diameter, d_0 was 150 nm. We can see T_G strongly influenced the uniformity and growth mode of nanowires. For T_G < 540 °C, InAs was not uniform and *h* was considerably low, as shown in the insets of **Figure 4–15(c)** and **Figure 4–16**. In addition, *d* was much larger than d_0, indicating that the lateral overgrowth in the {–110} directions took place. In contrast, the InAs structure became more uniform and *d* followed d_0 for T_G > 540 °C, suppressing the lateral growth. At T_G = 600 °C, the vertical growth of InAs was also suppressed although the *d* equal to d_0. Thus, the optimized T_G for obtaining uniform InAs NWs is concluded to be in between 540 and 560 °C. Desorption rate of arsenic in InAs is greater than that from GaAs with respect to the increase of T_G, as previously reported in Ref. [31]. For InAs, the similar mechanism as GaAs is predicted and thought to be enhanced due to weaker bonding of indium and arsenic resulting in the decrease of lateral growth along the {–110} directions. Furthermore, at much higher temperature, T_G > 600 °C, desorption of arsenic or indium on (111)B thought to be more enhanced.

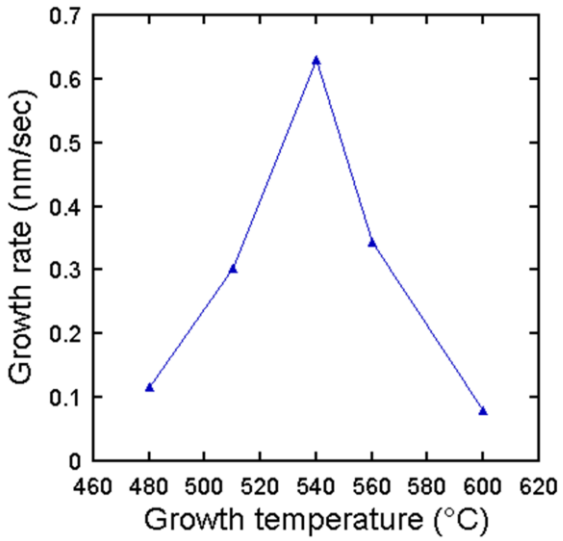

Figure 4–16

Growth temperature dependence of axial growth rate of InAs nanowires. V/III ratio and the diameter of the mask openings, d_0, were 265 and 150 nm, respectively.

4.3.2 Effects of V/III Ratio for InAs Nanowires

K. Tomioka *et al*. has also reported that the effects of V/III ratio for InAs NW growth [4]. The NW height, *h*, plotted as a function of NW diameter, *d*, as shown in **Figure 4–17(a)**. The growth condition was the same as in **Figure 4–15(a)** except for AsH_3 partial pressure, P_{AsH3}, guaranteeing $d \sim d_0$. The *h* increased as the *d* decreased and was inversely proportional to d^2, independent of P_{AsH3}. This result can be explained by a simple surface diffusion process of indium on masked region, where the *h* is proportional to $1/d^2$ when we assume the surface diffusion contributes to the planar growth. In addition, the axial growth rate of NWs became faster as the P_{AsH3} was increased.

Figure 4–17(b) shows the growth rate of InAs NWs, which diameter is 100 nm, and on (001), and (111)B planar substrates, plotted as a function of the P_{AsH3} or V/III ratio at T_G = 540 °C. The dependence of growth rate on V/III ratio is similar to that of (001) planar but opposite to that of the (111)B planar. In the case of (001) planar, the growth rate became faster with the increase of P_{AsH3}, presumably because the growth process is limited by reaction or

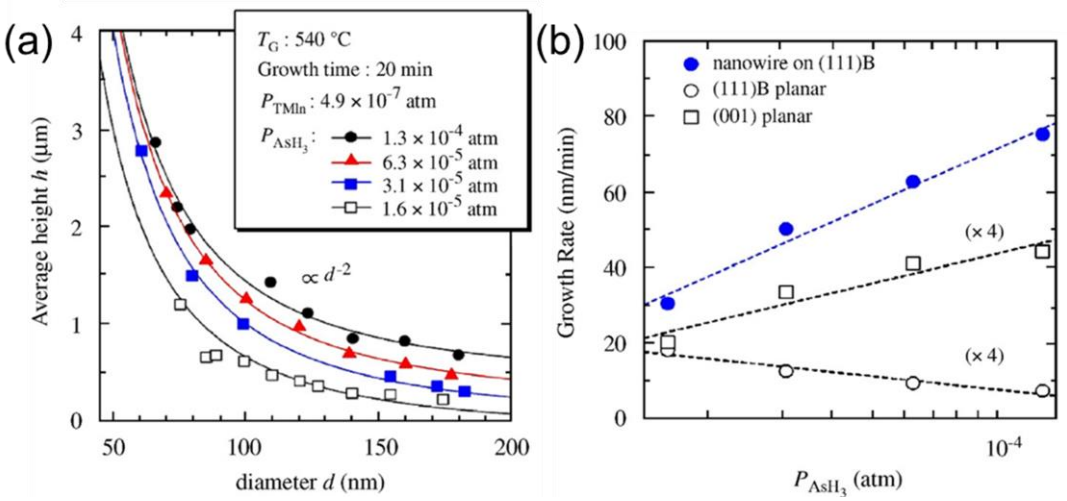

Figure 4–17

(a) Height, *h*, of InAs nanowires as a function of diameter, *d* and (b) growth rate of nanowires (closed circles) for d_0 = 100 nm, (001) planar (open circles), and (111)B planar (open squares), as a function of P_{AsH3} (partial pressure of AsH_3).

decomposition of AsH_3. In contrast, the decrease of growth rate at higher P_{AsH3} on (111)B surface is due to the formation of stable arsenic–trimers and their hindrance to the growth, as similar to the case of GaAs (111)B surfaces [32]. In this context, we expected the reduction of growth rate in the case of SA–MOVPE of InAs NWs on (111)B. However, the growth result for InAs NW growth is in contradiction with above expectation.

K. Tomioka *et al*. argued that this apparent inconsistency in (111)B surface between planar growth and SA–growth of NWs is in the difference of growth mechanism between them. That is, suppression of the growth due to arsenic–trimers is absent during SA–MOVPE on InAs (111)B. Such behavior has not been observed for SA–MOVPE on GaAs on (111)B. However, it is possible, for instance, the existence of high–density step or kink sites in the case of SA–MOVPE and effectively large indium concentration due to surface diffusion of indium species. Therefore, the situation of SA–MOVPE on InAs (111)B is more or less similar to the case of planar MOVPE growth on InAs (001). If one compares the enhancement of the NW growth with respect to (001) planar substrates, it was six and seven times for $P_{AsH3} = 1.6\times10^{-5}$ and 1.3×10^{-4} atm, respectively, exhibiting less dependence on P_{AsH3}.

4.3.3 Crystal Structure of InAs Nanowires

Characterizations of crystal structure of InAs NWs by transmission electron microscopy (TEM) have been reported by K. Tomioka *et al.* [5]. TEM observation was performed with acceleration voltages of 300 kV at the <1–10> incidence. Selected area electron diffraction (SAED) patterns were also observed through the [1–10] projection. **Figure 4–18(a)** shows a bright–field TEM image of the InAs NW grown by SA–MOVPE. The NW diameter, *d*, was 60 nm. The SAED patterns and high–resolution TEM images are shown in **Figure 4–18(b)** and **Figure 4–18(c)**, respectively. The growth direction of the InAs nanowire was in the (111)B direction. **Figure 4–18(c)** indicates that the NW had a zincblende (ZB) structure, because the lattice images are stacked at an angle of approximately 19.5° with respect to the (111)B direction. **Figure 4–18(a)** and vertical streaks in **Figure 4–18(b)** also indicate that the existence of rotational twins along the growth direction. In addition, the crystal structure deduced from the SAED pattern would be neither a ZB nor a wurtzite (WZ) structure.

The inconsistencies between the SAED pattern and the high–resolution images can be explained by the analysis of the atomic layer stacking. The sequence of the layer stacking can be expressed as ABCABC... for ZB crystal, whereas it is ABAB... for WZ crystal. The atomic configuration at the boundary of the rotational twins usually has a WZ–type crystal structure [33]. Following this definition, it can be categorized that the stacking of every three monolayers (MLs) in the lattice images as a ZB or a WZ segment. For example, ABC or ACB stacking is a ZB segment, whereas ABA, ACA, or BCB stacking is a WZ segment. The analysis of the transition thickness from ZB to WZ segments, or *vice versa*, in InAs NWs was carried out for NWs of various diameters (d = 28, 60 and 170 nm) and is summarized in **Figure 4–18(d)**. The percentages of the transition in 1, 2, and 3 MLs for the 60–nm–thick InAs NW were 56, 27, and 7 %, respectively. This indicates that the rotational twins were introduced in every one to three MLs. This tendency has no dependence on their diameter. Such quasi–periodic stacking forms a sort of superlattice with ZB and WZ structures and gives rise to satellite peaks in the SAED pattern [34]. This suggests that the coexistence of ZB and WZ segments with randomly stacked atomic layers in the very small transition thickness caused the inconsistencies found in the high–resolution lattice image and diffraction patterns. The quasi–periodic crystal phase

transition caused the coexistence of ZB and WZ crystal phases in the SA–grown NWs. Such coexistence has not been observed in other SA–grown NWs, such as GaAs [34] and InP [34] NWs. Koguchi *et al*. has observed a crystal change from ZB to WZ structure in VLS–grown InAs NWs [33], and WB structure has also been observed in VLS–grown InAs NWs [35]. This indicates that both crystal phases can exist with rotational twins at every stacking sequence, but the SA–grown InAs NWs in this study are quite different from those for VLS–grown InAs NWs. The growth mechanism is considered to be the factor behind such phenomenon because the SA–MOVPE is based on chemical reaction occurring at the vapor–solid interface and the VLS is based on supersaturation in the liquid phase. The higher growth temperature, T_G, of the InAs NW compared with those of typical InAs planar growth (T_G < 500 °C) and VLS–grown InAs NWs (T_G = 350 °C [33]) is also considered to be one of the factors.

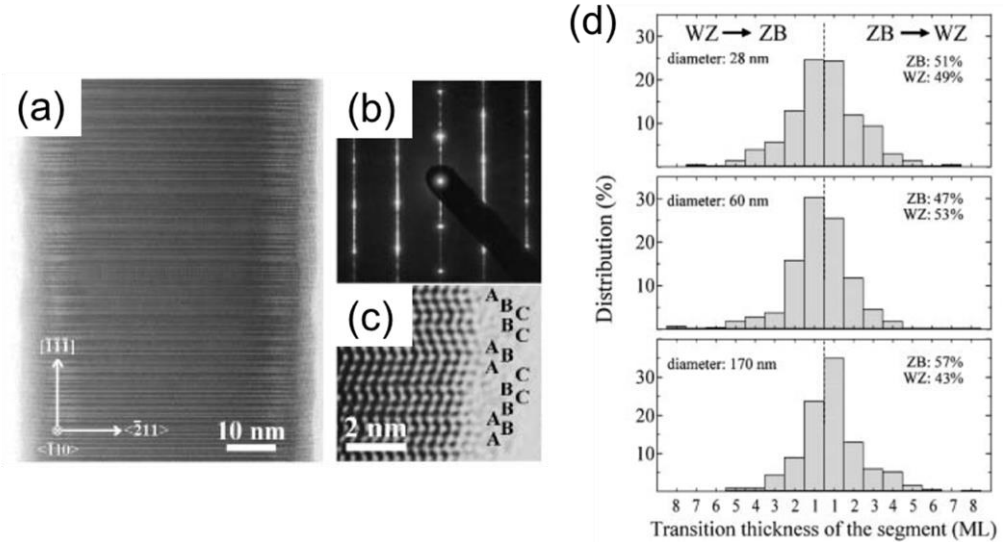

Figure 4–18

(a) Bright–field transmission electron microscopy (TEM) image of an InAs nanowire grown on an InAs (111)B substrate. The dark and bright contrast is due to rotational twins. (b) Selected area electron diffraction (SAED) pattern and (c) high–resolution lattice image of InAs nanowires. The letters (A, B, and C) in (c) represent labels for layer stacking used in the statistical analysis and are determined by the relative position of the spots in the lattice image. (d) Statistics of the transition thickness from ZB to WZ segments, or *vice versa*, in nanowires.

4.4 Selective–Area Growth of InGaAs Nanowires

4.4.1 Effects of Group–III Supply Ratio for InGaAs Nanowires

Effects of group–III supply ratio for SA–MOVPE of InGaAs NWs have been reported by T. Sato *et al*. [19][20]. The SA–MOVPE of InGaAs NWs was carried out on InP (111)B substrate partially covered with SiO_2 film as shown in **Figure 4–19(a)**. The source materials were trimethylgallium (TMGa), trimethylindium (TMIn) and arsine (AsH_3). The growth temperature was 650 °C and the partial pressure of AsH_3, [AsH_3], was 5.0×10^{-4} atm. The total of the partial pressures of TMGa, [TMGa], and TMIn, [TMIn], were 4.9×10^{-6} atm [36], and x_{supply} = [TMGa]/([TMGa]+[TMIn]) was changed as 0.80, 0.65, 0.52, and 0.20.

Figure 4–19(b)–(e) show the results of the SA–growth of InGaAs with various x_{supply} (or Ga_{supply}). The growth time was 10 min, and the mask pitch, *a*, was 1 μm. Highly uniform hexagonal structures were formed in the mask openings. The sidewalls of the hexagonal structures are confirmed to be {–110} facets vertical to (111)B. It is also clear that the height of the grown structures becomes higher as x_{supply} increases. The diameter, *d*, of hexagonal

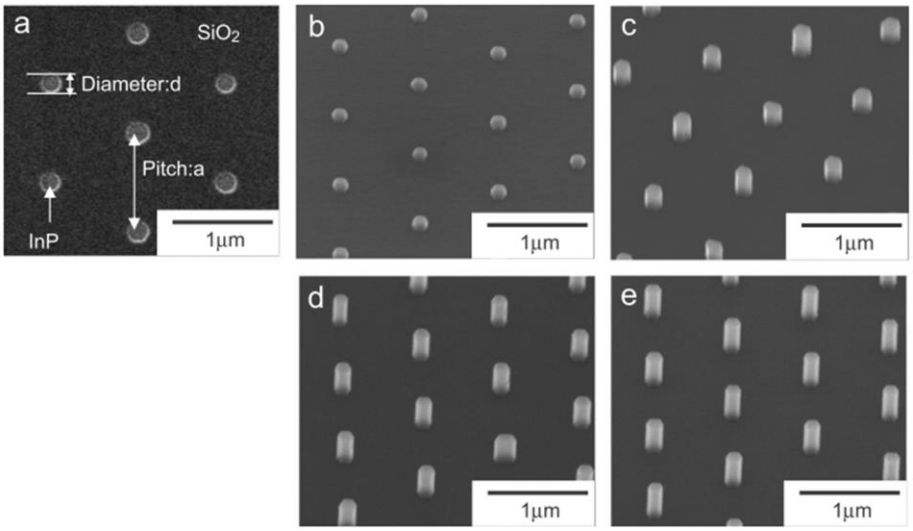

Figure 4–19

(a) SEM image of a patterned substrate. The diameter of the mask hole is 120 nm. Results of SA–MOVPE of InGaAs on masked substrate of (a) with x_{supply} (or Ga_{supply}) of (b) 0.20, (c) 0.52, (d) 0.65, and (e) 0.80. The growth time is 10 min.

structures is 100 nm and is almost the same as the opening size (see **Figure 4–19(a)**). These results indicate that the growth in the lateral direction of NWs (i.e., growth in the <–110> direction) is negligible, while the growth rate in the vertical (i.e., in the <111>B) direction (or their height, *h*) depends on the composition of the input flow.

In addition, *h* increased for small *d*, particularly for high x_{supply} (not shown here). This dependence of *h* on *d* seems to be explained simply by the diffusion of growth species from masked area to open areas [37]. Care must be taken, however, since the height does not follow a constant volume model, that is, the volume per unit area, $h(d/a)^2/t$, is not constant but varies with *d*. In addition, the total volume of the growth is reduced compared to the volume expected for the planar growth. Furthermore, the enhancement of the growth rate for small *d* is larger for larger values of x_{supply}. This is in contradiction with the fact that the diffusion length for indium is longer than that for gallium [38]. It also has been found that the vertical growth rate is enhanced for shorter *a* (not shown here). Similar dependence for the growth of GaAs NWs has already been reported, which is also not explained by the simple diffusion equation, and should be attributed to the increase of group–III materials supply as described in **Section 4.2.5** [3].

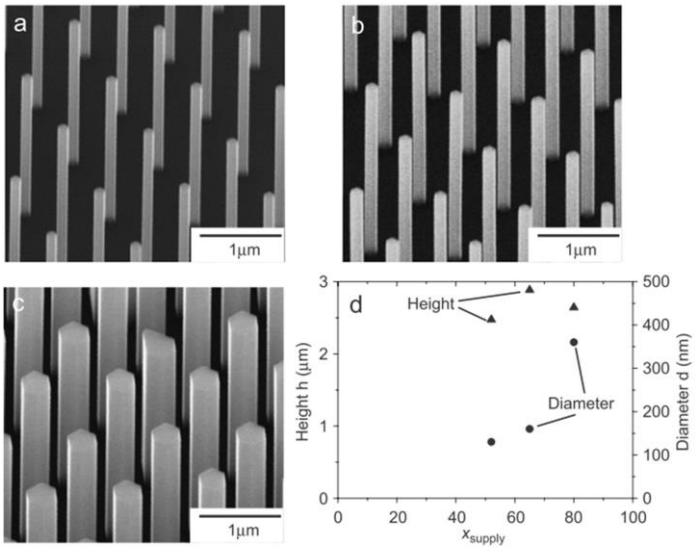

Figure 4–20

(a)–(c) SEM images of InGaAs nanowires for a growth time of 30 min. x_{supply} (Ga_{supply}) is 0.52, 0.65, and 0.80 for (a)–(c), respectively. (d) Height and diameter of InGaAs nanowires plotted as a function of x_{supply}.

Figure 4–20(a)–(c) show the results of InGaAs growth for 30 min with different x_{supply}. Hexagonal NWs were obtained independently of the x_{supply}. Note that the grown height (see **Figure 4–20(d)**) increased greatly as compared to the case of 10 min. The enhancement is larger for smaller x_{supply}. In addition, though the initial opening diameters, d_0, of the substrate patterns were the same (in this case, d_0 =120 nm), it is clear that the NWs are much thicker and that considerable lateral growth took place for x_{supply} =0.80.

Figure 4–21(a) shows the axial growth rate of InGaAs NWs versus mask pitch for d = 120 nm. The growth time was 30 min. The growth rate is larger for narrower pitch. This dependence cannot be explained by a simple diffusion model, which predicts that the smaller filling fraction results in the larger enhancement [3][19]. Nevertheless, the result is thought to indicate that the gallium composition increases with narrow pitch. To confirm this expectation, micro–photoluminescence (μ–PL) measurement of InGaAs NW arrays grown under various x_{supply} were carried out and evaluated the alloy composition of InGaAs NWs from PL peak energy. **Figure 4–21(b)** shows the estimated gallium composition of InGaAs nanowires. Gallium composition of NWs is increased with narrowing pitch, as expected from the results of **Figure 4–21(a)**. Thus, T. Sato *et al*. concluded that the gallium enhances the growth rate, and the increase of growth rate with narrowing pitch is mainly originated from gallium diffusion.

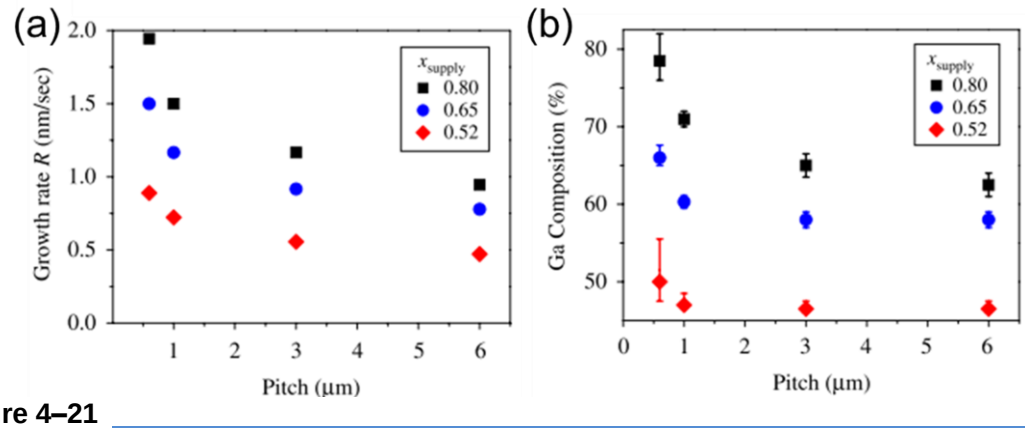

Figure 4–21

Pitch dependence with 120 nm diameter : (a) growth rate and (b) gallium (Ga) composition. Full–width of half–maximum (FWHM) of PL spectrum are indicated as the error bars in (b).

4.4.2 Time Evolution of InGaAs Nanowires

Study on the time evolution of InGaAs NWs has been reported by T. Sato *et al*. [19]. The SA–MOVPE of InGaAs NW was carried out on InP (111)B substrate partially covered with SiO_2 film, and growth conditions are same as those for described in **Section 4.4.1**. In previous section, we have described about the growth results of selectively–grown InGaAs NWs for growth time, *t*, of 10 and 30 min. Further increase of the growth time revealed the complicated dynamics of SA–MOVPE of NWs. **Figure 4–22** shows the typical results for the time evolution of height (closed squares), *h*, and, diameter (closed circles), *d*, of NWs. The supply ratio, x_{supply} was 0.52, the pitch, *a*, is 1 μm, and d_0 is 80 nm. In addition to the experimental data for $t > 30$ min, an extrapolated data point of *h* for $t = 10$ min with $d_0 = 80$ nm is also plotted with an open square. If taking into account this extrapolated data, *h* increased superlinearly for short *t*, but almost linearly for longer *t*. Such superlinear increase of *h* with increasing growth time has already been reported [39], where the height of the InGaAs NWs was more than doubled when the growth time was increased from 7.5 to 15 min. On the other hand, the diameter, *d*, increased nearly linearly for $t > 60$ min, suggesting that the lateral growth becomes significant after a certain amount of growth. It was also found that the distribution of both height and diameter of nanowires becomes broader as *t* increases, as indicated by the error bars shown in **Figure 4–22**.

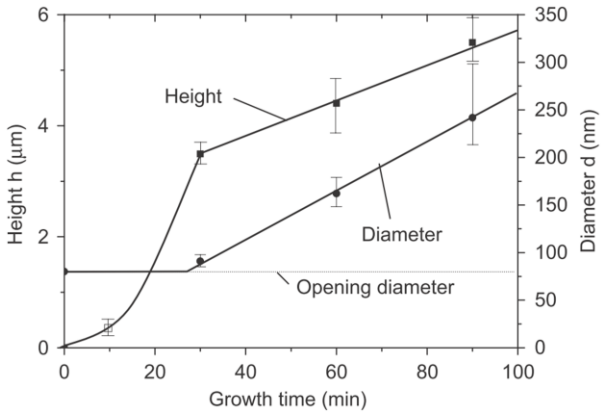

Figure 4–22

Time evolution of nanowire height (closed squares) and diameter (closed circles). The opening diameter of the mask is 80 nm and x_{supply} is 0.52. Extrapolated height for 80 nm–thick nanowires is also shown as an open square.

Results of **Figure 4–22** show nonlinear behaviors in the growth rate both in the vertical and lateral directions, and that nonlinearity depends on x_{supply}. It is also suggested that the lateral growth results in the non–uniformity in the size of NWs. To explain these experimental observations, the model suggested in Ref. [3] was used, and the details of this model are described in **Section 4.2.5**. For adapting this model to this study, two growth species, namely, gallium and indium should be considered. In the following, the subscripts *m*, {–110}, and (111)B for the distinction of parameters appearing in diffusion equation for masked area, the sidewall, and the top, respectively, and superscripts Ga and In for the species of gallium and indium when it is necessary. It was assumed that they are constant for given temperature and do not depend on the NW size. Then, the diffusion length on the top NW surface, $L_{(111)B} = \sqrt{D_{(111)B}\tau_{(111)B}}$ is assumed to be much longer than the NW diameter, *d*, and the lifetime, τ'_m, of species for incorporation at the masked region is assumed to be infinite. These hypotheses are validated by the experimental results. It is also assumed that fluxes J^{Ga} and J^{In} are simply proportional to the partial pressures of TMGa and TMIn, respectively. At the beginning of the growth, the height of the NWs is low, thus, it is considered that $h \ll L_{\{-110\}}$, where $L_{\{-110\}} = \sqrt{D_{\{-110\}}\tau_{\{-110\}}}$ is the diffusion length of the growth species on the sidewalls. In this case, the growth on the nanowire sidewalls, which is proportional to $N_{\{-110\}}\tau'_{\{-110\}}$, is minimal, and thus, the growth of NWs is determined by the diffusion of growth species from masked area to mask opening. This situation holds for t = 10 min, and a key to understanding the dependence on group–III pressure is a difference in optimum growth temperatures for GaAs and InAs. According to our previous reports as shown in **Sections 4.2.3** and **4.3.1**, optimal growth temperature for GaAs and InAs NWs in SA–MOVPE are 750 °C [3] and 540 °C [4], respectively. The size of InAs NWs becomes non–uniform for temperatures higher than 560 °C. The growth temperature for InGaAs is 650 °C in this study. Therefore, it can be expected that indium atoms are easily evaporated from the mask, while gallium atoms incorporate into the NWs. It means that $\tau_m^{In\prime\prime}$ is short and that the diffusion length, $L_m = \sqrt{D_m\tau_m}$, on masked area for indium is effectively shorter than that for gallium in SA–MOVPE in this growth conditions. The shorter L_m^{In} would result in the weaker dependence of the growth height *h*, on the diameter, *d*, and this is actually found in the experimental results, where the diameter dependence is weaker for larger [TMIn]. One of the other possibilities we can think of is that the lower growth

rate with larger [TMIn] is due to short $\tau^{In''}_{\{-110\}}$ for indium at such high temperature; In other words, the sticking coefficient of indium is lower on (111)B. However, this cannot explain the weaker dependence of *h* on *d*. There also is a much more complicated situation where $\tau^{In''}_{\{-110\}}$ is also short, but as long as $h \ll L_{\{-110\}}$ is held, it does not fully explain the experimental results. The last two situations are also in contradiction with the enhancement of the vertical growth for longer growth time.

The diffusion from the masked area to the openings also can explain the superlinear increase of the NW height at the initial stage of the growth. However, the situation becomes somewhat different when the lateral growth sets in, for instance, at longer growth time and larger *h*. It would be plausible that shorter diffusion length, $L_{\{-110\}}$ on the sidewalls results in the enhanced growth on the sidewall and suppression of the vertical growth. In the absence of diffusion, the growth rate of both vertical and lateral direction is constant, as observed in **Figure 4–22**. Thus, the onset of the lateral growth and transition into constant growth rate is thought to be at $L_{\{-110\}} \sim h$. Furthermore, to explain the experimental results of **Figure 4–20**, the diffusion length on the sidewall, $L_{\{-110\}}$, should be longer for indium than that for gallium. A short diffusion length of gallium on the sidewalls of the NWs is also possible, since the growth temperature for this case is lower than the optimum temperature for GaAs NWs without any lateral growth, and is much more preferable for the growth on {–110} surfaces [1]. If one accepts this, it may be possible to explain the larger enhancement of the vertical growth rate for larger TMIn supply.

T. Sato *et al*. concluded this study as follows. At the initial stage, the lateral growth was negligible and the growth rate was higher for smaller *d* and higher [TMGa]. This suggested shorter diffusion length from mask to opening for indium than that for gallium, and was attributed to the indium evaporation from the mask due to the higher growth temperature of InGaAs NWs than that for InAs NWs. The height of the NWs increased superlinearly with time at the initial stage, but almost linearly for longer growth times. Simultaneously, the diameter of NWs also increased almost linearly after some time of growth. This was interpreted as the reduction of diffusion from sidewalls and the top of the NW, which takes place when the diffusion length from sidewalls to the top surface is comparable to the NW height.

4.4.3 Effects of Growth Temperature for Gallium–Rich InGaAs Nanowires

Effects of growth temperature for the SA–growth of gallium–rich InGaAs NWs have been reported by M. Yoshimura *et al*. [21]. The SA–MOVPE of InGaAs NWs was carried out on GaAs (111)B substrate partially covered with SiO_2 film. The source materials were TMGa, TMIn and AsH_3. The partial pressure of AsH_3, [AsH_3], TMGa, [TMGa], and TMIn, [TMIn], were 1.25×10^{-4}, 1.42×10^{-6}, and 1.22×10^{-7} atm [36], respectively. The V/III ratio was 81, and x_{supply} = [TMGa]/([TMGa]+[TMIn]) was 0.92. The growth temperature, T_G, was varied between 600 and 700 °C.

SEM images of patterned substrate after the SA–MOVPE at T_G from 600 to 700 °C are shown in **Figure 4–23(a)–(e)**. Particle–like depositions with diameters of 1 to 3 μm on the patterned areas were observed for the samples grown at 600, 625, and 650 °C. The density of the particle–like depositions was maximum at 600 °C [**Figure 4–23(a)**], but the depositions decreased in size and density with increasing T_G [**Figure 4–23(b)** and **Figure 4–23(c)**] and disappeared at approximately 675–700 °C [**Figure 4–23(d)** and **Figure 4–23(e)**]. Arrays of hexagonal pillar–shaped NWs grew from the mask openings on the patterned areas where the particle–like depositions were not observed, as shown in **Figure 4–23(a)–(e)**. **Figure 4–24(a)** shows the T_G dependence of NW height, *h*, and axial growth rate of the NWs. The *h* and growth rate of the NWs clearly increased at higher T_G and for smaller d_0. This can be explained by the enhanced surface migration and the incorporation of source materials into the NWs at higher T_G. **Figure 4–24(b)** shows the T_G dependence of NW diameter, *d*, for various d_0. The *d* for each d_0

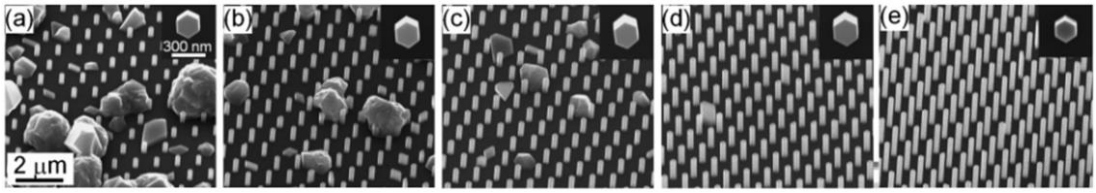

Figure 4–23

SEM images of InGaAs nanowires grown at (a) 600, (b) 625, (c) 650, (d) 675, and (e) 700 °C. The mask pattern pitch *a*, and mask opening diameter d_0 are 1.0 μm and 100 nm, respectively. The inset shows a top view of the nanowire.

appear to be roughly equal and independent of T_G, under this growth condition. On the other hand, d increased by about 80–160 nm from d_0 of 50–200 nm and the amount of diameter increase showed no dependence on d_0.

Figure 4–25(a) shows PL spectra of InGaAs NWs grown at 700 °C with d_0 = 50–300 nm, and a = 0.5 μm, respectively. The observed PL peak energies for the NWs grown with a = 0.5 μm were 1.36–1.37 eV. Clear dependence of the PL peak energy shift on d_0 was not confirmed. The PL spectra of NWs grown at temperatures of 600–700 °C is plotted in **Figure 4–25(b)** for a = 1 μm and d_0 = 200 nm, respectively. The PL peak energy increased from 0.95 eV for NWs grown at 600 °C to 1.31 eV for NWs grown at 700 °C, indicating a strong dependence on T_G. Gallium composition of InGaAs NWs was estimated by PL peak energy, and are plotted in **Figure 4–26(a)** [40]. The full widths at half maximum (FWHM) of the PL spectra for the NWs are also plotted in **Figure 4–26(a)**. It was found that the gallium composition of the NWs grown at 700 °C was nearly equal to the group–III supply ratio, x_{supply}. It was also found that the gallium composition decreased with decreasing T_G. However, FWHM increased with decreasing temperature. The T_G dependence of FWHM in the PL spectra was thought to be caused by the effect of crystal alloying, which became marked owing to the increase in indium composition from 10 to 40 %, and the lattice mismatch between the grown InGaAs and GaAs substrate increased with decreasing T_G.

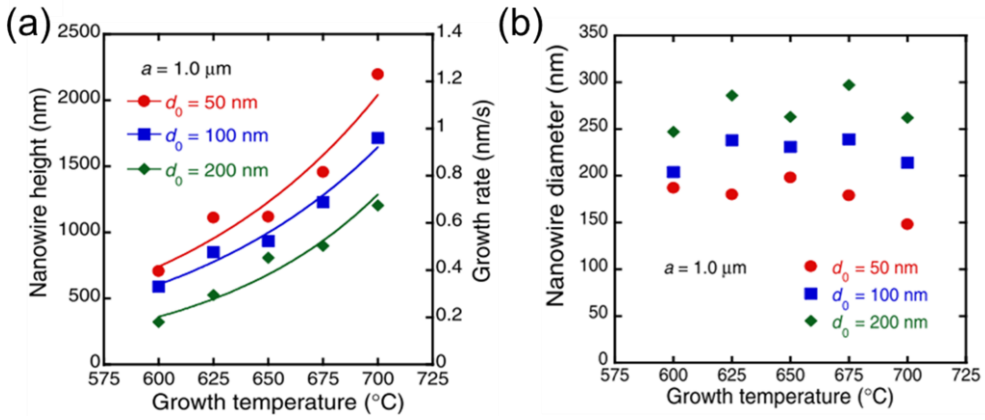

Figure 4–24

Growth temperature dependence of (a) height and growth rate, (b) diameter of InGaAs nanowires for a = 1.0 μm.

M. Yoshimura *et al*. argued that the arsenic–trimers on a GaAs(111)B surface may be related to the growth characteristic of gallium–rich InGaAs NW growth. It was reported that the GaAs (111)B surface was partially covered by arsenic–trimers [41], and these coverage increased with decreasing growth temperature [23]. The increase in the coverage of arsenic–trimers on GaAs (111)B may hinder gallium atoms from being adsorbed onto the surface, causing a decrease in growth rate along the (111)B direction [1][24]. InGaAs NWs grown at 700 °C have a gallium composition of up to 88 %; therefore, the growth characteristics are thought to be similar to those of GaAs NWs. It is considered that the decrease in growth rate with decreasing growth temperature may be due to the increased coverage of arsenic–trimers.

From the T_G dependence of InGaAs NW height and atomic composition obtained in this study, M. Yoshimura *et al*. estimated the portions for GaAs and InAs inside an InGaAs NW, as plotted by squares and diamonds, respectively, in **Figure 4–26(b)**. It was found that the InAs portion was almost independent of temperature, but the GaAs portion decreased with decreasing T_G. It was reported that for GaAs NWs grown on a GaAs(111)B substrate, the optimum growth temperature was about 750 °C [2], and the growth rate in the (111)B direction decreased with decreasing T_G owing to increased coverage of arsenic–trimers on the (111)B substrate [1].

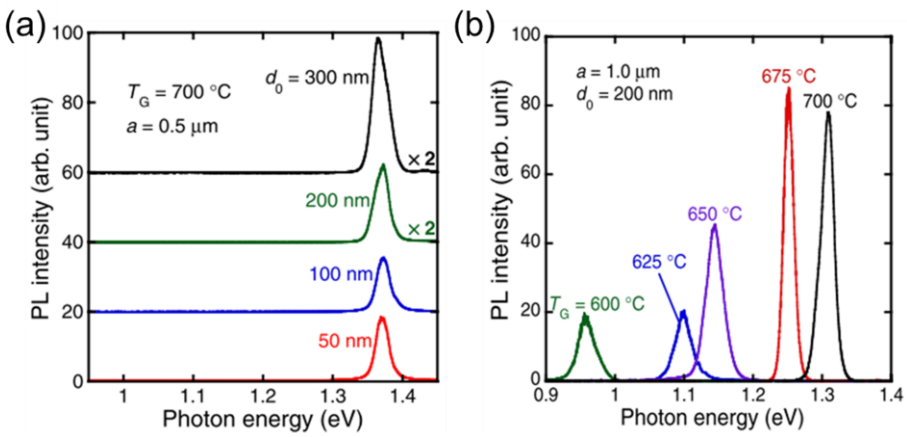

Figure 4–25

(a) PL spectra for InGaAs nanowires measured at 4.2 K. Spectra taken for pattern pitches of 0.5 μm. The base of each spectrum is shifted along the vertical direction for clarity. (b) PL spectra for InGaAs nanowires grown at 600, 625, 650, 675, and 700 °C with a = 1.0 μm.

Therefore, result of this study for the decreased height of the GaAs portion in the InGaAs NW with decreasing T_G agrees well with the model of GaAs NW growth on a GaAs(111)B substrate. On the other hand, K. Tomioka *et al*. found that the optimum growth temperature of InAs NWs grown on an InAs(111)B substrate using SA–MOVPE was about 540 °C [4]. They argued that InAs NW growth was not hindered by arsenic–trimers, but was similar to planar InAs layergrowth on InAs(001) as shown in **Section 4.3.2**. The result for the InAs portion plotted in **Figure 4–26(b)** indicates that InAs NW growth was not affected by the formation of arsenic–trimers on (111)B. From this argument, it can be speculated that some amount of the source material to be consumed as the GaAs portion of the InGaAs NW might be changed to the particle–like depositions on the masked surface, as observed in **Figure 4–23**.

Regarding the dependence of PL peak energy on d_0 for a = 0.5 μm, it was confirmed that no distinct dependence of peak energy on d_0, and was also found no clear dependence of PL peak energy on d_0 for a = 1.0 μm (not shown here). It cannot be understood why there was no diameter dependence, but there was dependence for a = 2.0 μm (not shown here). Detailed study on this issue were required and left for future study.

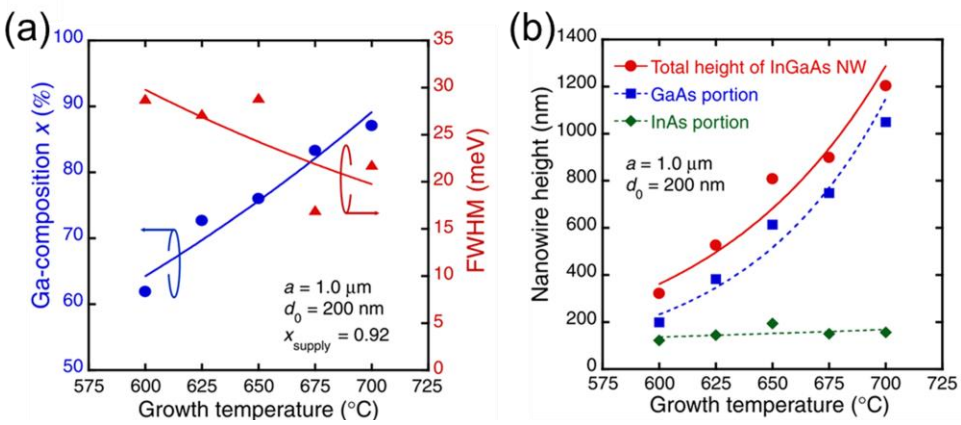

Figure 4–26

(a) Growth temperature dependence of gallium composition x in $Ga_xIn_{1-x}As$ nanowire and the full widths at half maximum. (b) Growth temperature dependence of GaAs and InAs portions in height and total InGaAs nanowire height for d_0 = 200 nm and a = 1.0 μm.

4.4.4 Crystal Structure of InGaAs Nanowires

M. Yoshimura et al. has also reported the characterizations of crystal structure of InGaAs NWs grown by SA–MOVPE [22]. The growth of InGaAs NWs was carried out on GaAs (111)B substrate partially covered with SiO_2 film and of InGaAs undoped semi–insulating GaAs (111)B and GaAs (100) substrate. The source materials were TMGa, TMIn and AsH_3. The partial pressure of AsH_3, [AsH_3], TMGa, [TMGa], and TMIn, [TMIn], were 1.25×10^{-4}, 4.97×10^{-7}, and 1.22×10^{-7} atm [36], respectively. Structural characterizations of the InGaAs NWs were carried out using SEM and high–resolution transmission electron microscopy (HR–TEM) with an acceleration voltage of 300 kV along the <–110> incidence. Selective area electron diffraction (SAED) patterns were also observed on the <–110> projection. The compositional variations within NWs were analyzed using energy dispersive X–ray spectroscopy (EDX) combined with TEM. The specimens were cut along (–211) by focused ion beam (FIB) after being buried in resin. μ–PL measurement was carried out using a He–Ne laser as the excitation source with a power density of about 1.0 kW/cm^2. The laser spot size was focused to approximately 2 μm in diameter on the sample surface using a ×50 microscope objective with a 0.42 numerical aperture.

Figure 4–27(a)–(d) shows cross–sectional HR–TEM images of an InGaAs NW (NW diameter, d = 90 nm and NW height, h = 2 μm) and locally magnified images at the top, middle, and bottom of NW, respectively. The corresponding SAED patterns are shown on the right side of the magnified HR–TEM images, **Figure 4–27(e)–(g)**. It was found that the hexagonal spot patterns in **Figure 4–27(e)–(g)** indicate a zincblende (ZB) structure and that there is no wurtzite (WZ) material anywhere from top to bottom except for the twin boundaries. The TEM images and the SAED patterns also show that the NW has rotational twins around the <111> axis as known from streak satellite spots found near the main spots (corresponding to the ZB structure). The formation mechanism was discussed by K. Tomioka *et al*. [5] for InAs NWs and by H. Yoshida *et al*. [42] for GaAs NWs. Yoshida *et al*. argued that the density or frequency of rotational twins, along the <111> direction increased as the mask opening diameter, d_0, decreased. Tomioka *et al*. [5] stated the coexistence of ZB and WZ segments with randomly stacked atomic layers in the very small transition thickness for the InAs NWs with diameters

ranging from 28 to 170 nm. Their analyses also revealed that the frequency of rotational twins was not clearly dependent on the position along the NW. The TEM measurements for the InGaAs NWs with diameters of 60 nm and 90 nm showed that the twin frequency for the 60 nm diameter NW was higher than that for the 90 nm diameter NW. The dependence was similar to that reported by Yoshida *et al*. Thus it is thought to the formation mechanism of the rotational twins in the InGaAs NWs is similar to that in GaAs NWs.

Figure 4–28(Left figure) shows atomic content profiles for arsenic, As, gallium, Ga, and indium, In, obtained by EDX line–scans along the longitudinal direction of NW, with an high angle annular dark–field (HAADF)–TEM image posted above the profiles. The image shows that the NW is about 2 μm long and 60 nm in diameter and a bit curved near the middle

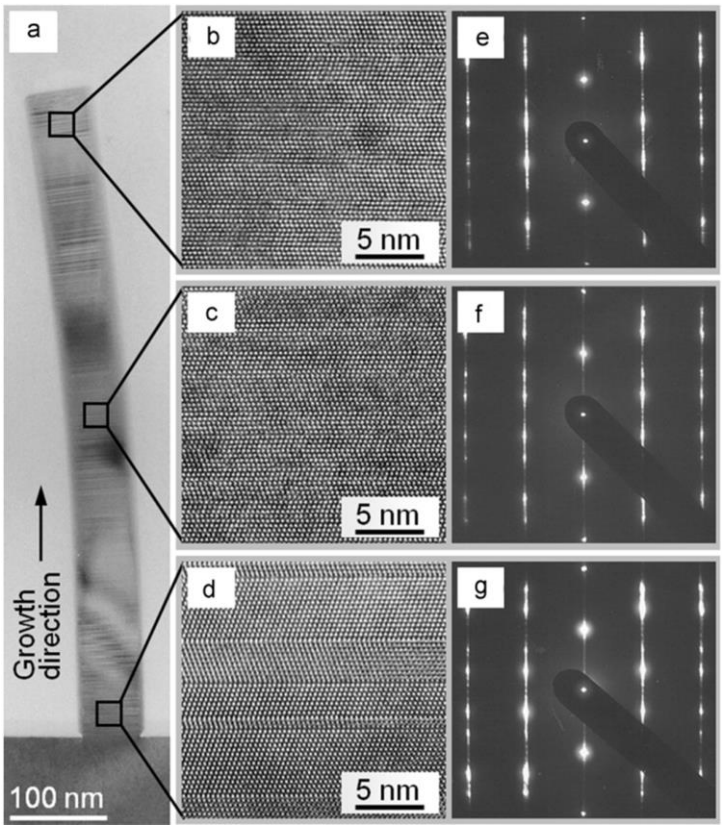

Figure 4–27

(a) Cross–sectional TEM images of InGaAs nanowire 90 nm in diameter and locally magnified images at the (b) top, (c) middle, and (d) bottom of the nanowire. The corresponding SAED patterns at the (e) top, (f) middle, and (g) bottom of the nanowire.

point. In **Figure 4–28(Left figure)**, the green, blue, and red lines represent atomic fraction profiles of elemental As, Ga, and In, respectively. The content ratio of In to Ga is about 26–74, as deduced from the profiles. Therefore, the lattice mismatch between the InGaAs NW and the GaAs substrate is approximately 1.9%. The atomic content profiles in **Figure 4–28(Left figure)** indicate that the group–III mole fractions are virtually constant along the 2 μm–long NW, which also indicates that the difference in migration length between In and Ga atoms on the sidewall facets has no effect on longitudinal composition change in NWs up to 2 μm. This result is very important to fabricate lattice–mismatched InGaAs NW devices, in which the atomic composition needs to be constant along the longitudinal direction of a NW.

Figure 4–28(Right figure)(a) shows an HR–TEM image of a heterointerface between the InGaAs NW and GaAs substrate. The diameter and height of the NW are 90 and 950 nm, respectively. The lattice mismatch between the NW and the substrate is 2.1%, as estimated from

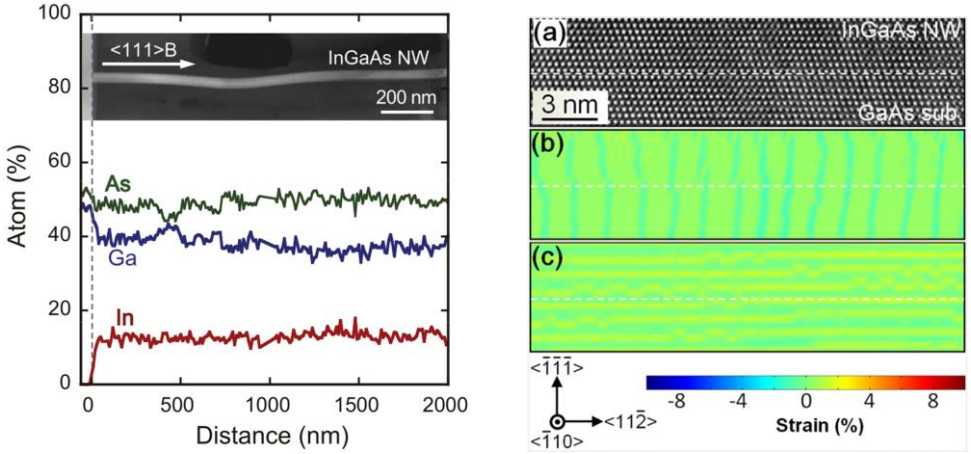

Figure 4–28

Left figure: Atomic content profiles for gallium, indium, and arsenic measured along an InGaAs nanowire by EDX. An HAADF–TEM image of the sample is posted above the profiles. The dashed line shows the interface between the nanowire and GaAs substrate.

Right figure: (a) HR–TEM image at the interface between an InGaAs nanowire and the GaAs (111)B substrate. The white broken line shows the interface; (b) ε_{xx} and (c) ε_{yy} are two–dimensional strain maps calculated along the <-1-12> and the <-1-1-1> directions from image (a).

the peak position of the μ–PL spectrum of NWs (not shown here). The displacements in lattice image of the heterointerface were calculated and converted them into strain maps using the peak–pair findingmethod developed by Galindo *et al*. [43], who analyzed strain distributions around the interface of CdTe/GaAs. The result of this analysis is shown in **Figure 4–28(Right figure)(b)** and **Figure 4–28(Right figure)(c)**. **Figure 4–28(Right figure)(b)** describes two–dimensional strain fields ε_{xx}, whose ***x*** vector is parallel to the <–1–1 2> direction and **Figure 4–28(Right figure)(c)** describes strain fields ε_{yy}, whose ***y*** vector is parallel to the <–1–1–1> direction, calculated from the displacement of the bright spots in the HR–TEM image. If misfit dislocations developed at the heterointerface, pairs of red–and–blue spots (the color indicating the magnitude of the localized compressive/tensile strain) at a dislocation could be observed on the strain map as described by Galindo *et al*. Tomioka *et al*. reported InAs NWs grown on Si (111) and observed the pairs of red–and–blue spots corresponding to misfit dislocations at the interface using the peak–pair finding method [44]. The period was about 3 nm, caused by the lattice mismatch of 7 % between InAs and Si. For InGaAs NWs in this study, despite the lattice mismatch of as high as 2.1% (the period for misfit dislocations is estimated at 16.8 nm for total relaxation), no pair of red–and–blue spots was observed at the heterointerface as shown in **Figure 4–28(Right figure)(b)** and **Figure 4–28(Right figure)(c)**, suggesting no misfit dislocation. The InGaAs NWs grown on GaAs (111)B are well within the coherent growth range calculated by F. Glas [18]. It is thus stated that InGaAs NWs as thick as 90 nm can be grown without defects, and therefore with good crystal quality over planar layers in heteroepitaxial growth.

4.5 Summary

We reviewed the features of the growth behaviors of GaAs, InAs, and InGaAs NWs in SA–MOVPE. We firstly described about the faceting growth and the twining growth model for NW growth was explained and knowledge of this mechanism is important for understanding the results and conclusions of this thesis. Following them, we explained the effects of growth temperature, V/III ratio, and mask pitch in the SA–growth of GaAs and InAs NWs, and the crystal structure of these kinds of NWs. Let us summarize the features of growth of GaAs and InAs NWs particularly for the effects of growth temperature and V/III ratio, as follows.

We explained the effects of growth temperature on the growth of GaAs and InAs NWs in SA–MOVPE in **Section 4.2.3** and **4.3.1**. It was confirmed that the optimum growth temperature for GaAs NWs was around 750 °C and that for InAs NWs was between 540 to 560 °C. This difference is thought to be due to the inherent dissimilarity in binding energy between GaAs and InAs. In addition, growth temperature dependence of NW height exhibited systematical and similar trend for GaAs and InAs NW growth, and the origin of this growth behavior is discussed in **Section 5**.

The effects of V/III ratio on the growth of GaAs and InAs NWs were explained in **Section 4.2.4** and **4.3.2**. It was confirmed that the V/III ratio dependence of NW height exhibited opposite trend between the growth of GaAs and InAs. This is thought to be originated form dissimilarity in surface reconstruction, that is, the existence or stability of arsenic–trimer coverage on (111)B surface. Such dissimilarity between GaAs and InAs originates the composition–dependent growth dynamics of InGaAs NWs discussed in **Section 6**.

Other dissimilarities between GaAs and InAs NW growth in SA–MOVPE are also important to understanding the results and conclusions of this thesis.

Finally, we reviewed the growth of InGaAs NWs based on our previous reports. Knowledge obtained from these reports is to be the basis of discussion of this thesis.

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Chapter 5

Composition–Dependent Effect of Growth Temperature on Selective–Area Growth of InGaAs Nanowires

Indium–rich InGaAs nanowires were grown on an InP(111)B substrate by catalyst–free selective–area metal–organic vapor phase epitaxy, and its growth–temperature dependence of growth rate and composition was studied. In particular, nanowire growth rate rapidly decreases as growth temperature increases. This tendency is opposite (for a similar temperature range) to that found in a previous study on selective–area growth of gallium–rich InGaAs nanowires. This difference between indium–rich and gallium–rich nanowires suggests that the influence of growth temperature on the growth of InGaAs nanowires is dependent on the group–III supply ratio. On the basis of previous experimental observations in InAs and GaAs nanowires, temperature dependence of nanowire growth rate and its dependence on group–III supply ratio are predicted. A guideline to determine the optimum growth conditions of InGaAs nanowires is also discussed.

5.1 Introduction

Epitaxially grown semiconductor nanowires (NWs) have generated much research interest lately because of their unique potential as building blocks of future electronic/photonic devices [1]–[5]. Because lattice strain allows elastic deformation without introducing misfit dislocations due to ultra–small growth regions [6], it is possible to achieve integration of III–V compound NWs on silicon platform [7]. One of the major approaches for growing NWs is a

catalyst–assisted vapor–liquid–solid (VLS) method, which includes however the possibility of catalyst incorporation, leading to lower quality NWs. On the other hand, the growth of NWs by catalyst–free selective–area metal–organic vapor–phase epitaxy (SA–MOVPE) was previously reported [8]–[11], which is fortunately capable of forming precisely controlled NWs in terms of size, position, and growth direction and producing future nanowire–based devices [12][13] without lowering quality of the NWs. Recently, indium–rich InGaAs channel metal–insulator–semiconductor FETs (MISFETs) has been studied intensively [14][15], because of its high electron mobility and good interface properties [16], which are however very sensitive to the mole fraction of group–III atoms [17].

The key issues for growing InGaAs NWs are controlling and uniformity of their size and alloy composition. In a recent study on SA–grown InGaAs NWs [18], we obtained highly uniform NWs and found that their alloy composition was constant along their whole length, which is more favorable to VLS–grown NWs [19][20] where their alloy composition varied unacceptably. However, our previous reports on the SA–growth of InGaAs NWs are still limited to the cases where growth rate and alloy composition were investigated as a function of group–III supply ratio [21][22] at fixed temperature, and of growth temperature under gallium–rich supply condition [23]. In the present study, temperature dependence of the growth of InGaAs NWs under an indium–rich supply condition was investigated and was compared with our previous results on InAs, gallium–rich InGaAs and GaAs NWs. A guideline to find the optimum growth conditions for InGaAs NWs across the whole alloy composition range is also discussed.

5.2 Experimental Details

The procedure of SA–MOVPE for fabricating InGaAs NWs is explained as follows (see **Figure 5–1(a)** and **Figure 5–1(b)**). After a 10–nm–thick SiO_2 film is deposited on an InP (111)B substrate by RF sputtering, periodic patterns of the openings in a SiO_2 mask were defined by electron–beam (EB) lithography and wet chemical etching. The patterns consisted of circular holes with diameter, d_0, ranging from 40 to 100 nm and mask pitch, a, was 1000 nm. NWs were then formed by a horizontal MOVPE system working at 0.1 atm, supplying

trimethylindium (TMIn), trimethylgallium (TMGa), and 20% arsine (AsH_3) diluted in hydrogen. The partial pressures of TMIn, [TMIn] and TMGa, [TMGa] were 1.63×10^{-6} and 0.70×10^{-6} atm [24], giving indium–supply (group–III supply) ratio In_{supply} = [TMIn]/([TMIn]+[TMGa]) being 0.70. The partial pressure [AsH_3] of AsH_3 was 2.5×10^{-4} atm, giving V/III ratio of 107. Growth temperature, T_G, and growth time, t, were varied from 590 to 650 °C and 10 to 90 min, respectively.

Height, h, and diameter, d, of the NWs were measured by scanning–electron microscopy (SEM). Alloy composition of NWs was estimated by micro–photoluminescence (μ–PL) measurement at 4 K. Excitation light from $TiAl_2O_3$ laser operating at 773 nm was focused on NW arrays by ×20 microscope objectives with a numerical aperture of 0.40, which was also used to collect the PL from the NWs.

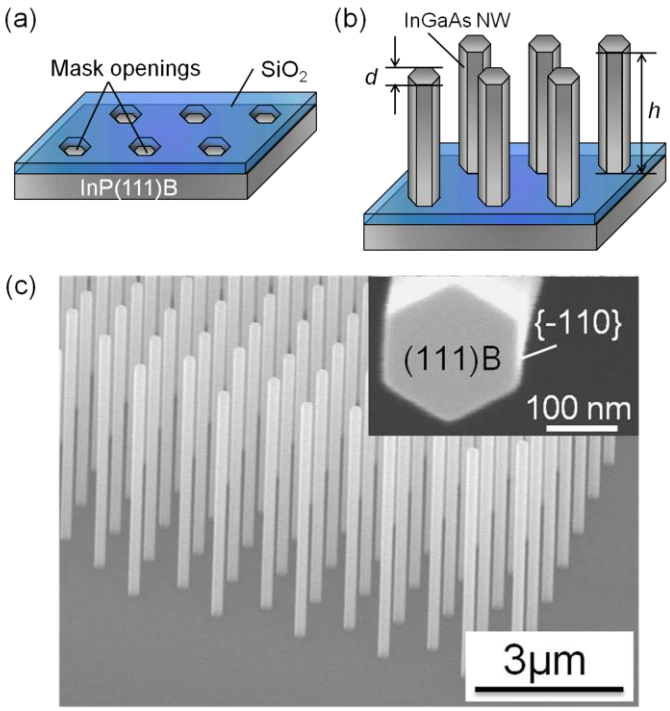

Figure 5–1

SA–MOVPE method for forming InGaAs nanowire array : (a) definition of opening patterns using EB lithography and wet chemical etching, (b) MOVPE growth of InGaAs nanowire, and (c) SEM image of InGaAs nanowires grown at 635 °C. The insets show a top view of the nanowires. The white scale bar represents 100 nm. (t = 30 min; d_0 = 100 nm)

5.3 Experimental Results

5.3.1 Growth of Indium–Rich InGaAs Nanowires

Figure 5–1(c) shows a typical SEM image of InGaAs NWs grown by SA–MOVPE. Growth temperature, T_G, and growth time, t, were 635 °C and 30 min, respectively, with opening diameter, d_0, of 100 nm. We can see that highly uniform and non–tapered NWs. In addition, these NWs have six sidewall {–110} facets normal to the (111)B plane in a similar manner to the cases of InAs, gallium–rich InGaAs, and GaAs NWs [10][11][21]. Similar NWs were observed for T_G from 590 to 650 °C.

It is noted here that the present study differs from our previous report on gallium–rich InGaAs NWs (In_{supply} = 0.08) in one respect [23]. Previously, particle–like depositions were found on the mask–opening regions for the samples grown at T_G from 600 to 650 °C. The density of particle–like depositions decreased as T_G increased, and the depositions disappeared at T_G of 700 °C. These particle–like depositions were not confirmed in the case of the present study (In_{supply} = 0.70), in aforementioned temperature range.

5.3.2 Temperature Dependence of Nanowire Size

Figure 5–2 shows temperature dependence of NW height, h, and diameter, d, at each d_0 for t = 30 min. It is clear that h significantly decreases as T_G increases, particularly above 620 °C. This result can be explained by an increase of desorption of constituent atoms from NWs or re–evaporation of precursors from masked area with increasing T_G [10].

It should be noted that this trend is in contrast to the results of gallium–rich NWs (In_{supply} = 0.08) [23], where higher T_G resulted in increased h from T_G = 600 to 700 °C. Namely, temperature dependence of h is quite different in the cases of indium–rich and gallium–rich NWs in the same T_G range. In addition, in Ref. [23], NW diameter, d, was larger than d_0, and it appeared to be independent of T_G. This is also in contrast to the result of the present study, where d clearly dependent on T_G, particularly above 620 °C and lateral growth is negligible at 650 °C.

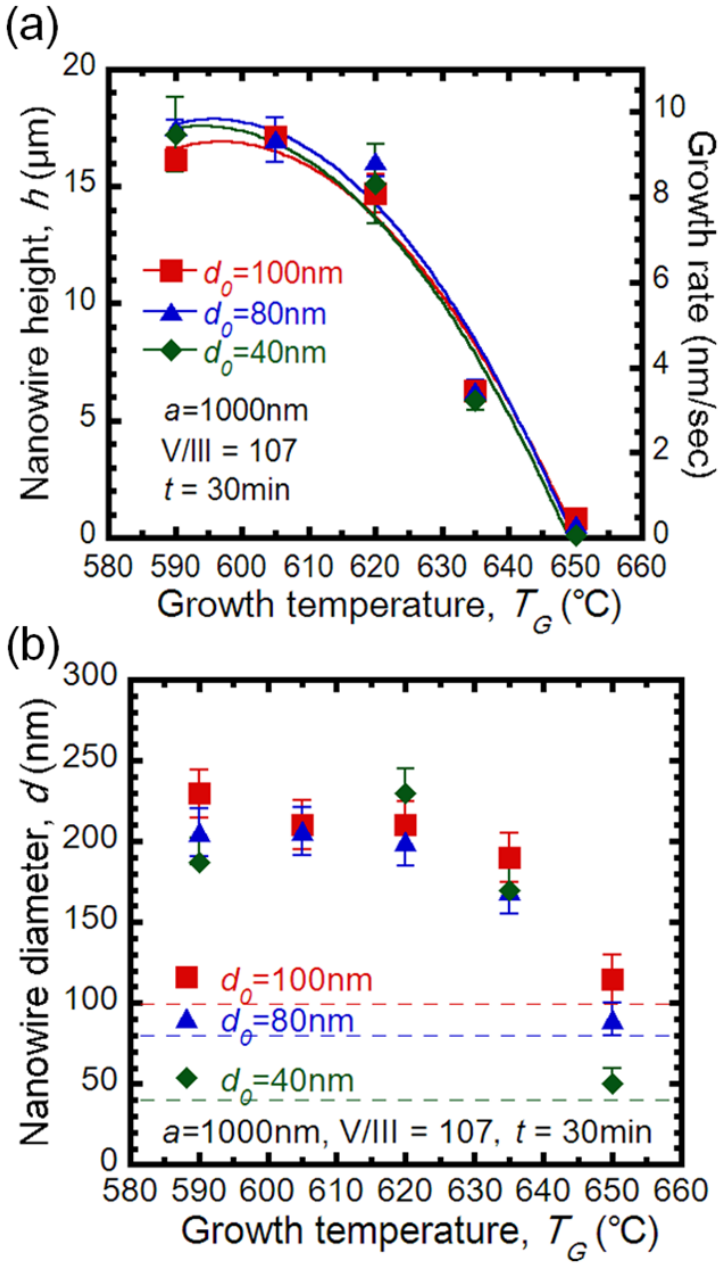

Figure 5–2

Growth temperature dependence of nanowire (a) height, *h*, and (b) diameter, *d*. The dashed line of inset (b) shows d_0. The error bars show maximum and minimum. (t = 30 min; d_0 = 40–100 nm)

5.3.3 Time Evolution of Nanowire Size

As shown in **Figure 5–2(b)**, significant lateral growth was observed in the samples grown below 635 °C. To identify the origin of this lateral growth, the time evolution of NW size was studied (see **Figure 5–3**). The Figure shows superlinear evolution of *h* for shorter *t*, and almost linear evolution for longer *t*. In addition, the lateral growth became significant after a certain amount of growth. This result is similar to our previous results presented in Ref. [21], where time evolution of the NW size was explained by a model based on a diffusion of growth species. In this model, it was argued that the lateral growth took place when *h* becomes larger than the critical length, which is determined by the diffusion length on the sidewalls of the NWs. We consider that the present results of time evolution of NW size can also be explained by the same model. The origin of the lateral growth is therefore mainly due to excessive growth time, and it can be ignored when an appropriate growth time is used.

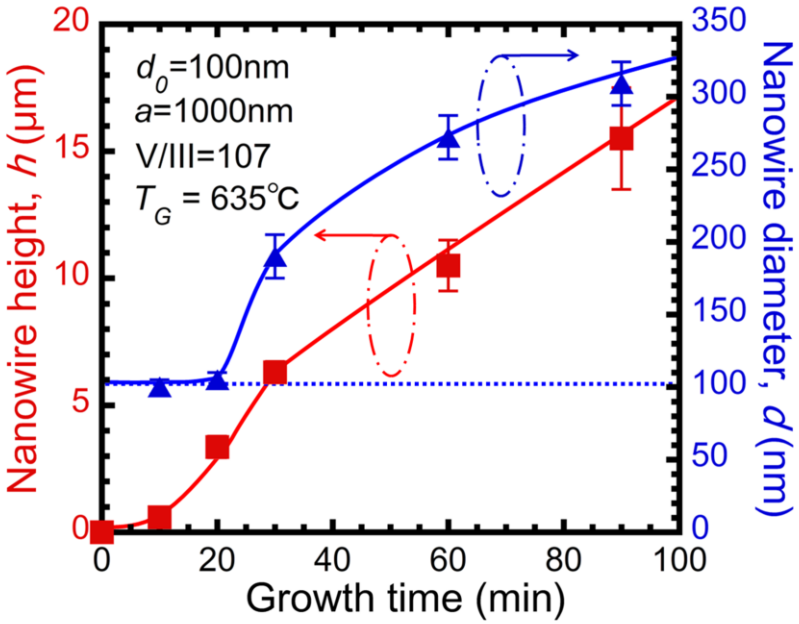

Figure 5–3

Time evolution of nanowire height, *h*, and diameter, *d*. Closed squares and closed triangles represent *h* and *d*, respectively. The dashed line shows d_0. (T_G = 635°C; d_0 = 100 nm)

Beside, as shown in **Figure 5–2**, h and d are not dependent on d_0. This independence is also due to the excessive growth time, since long–term growth over the critical NW length will enlarge d and eventually result in a similar NW size independently of d_0. Note, however, that it implies that the lateral growth was more enhanced in the initial stage of growth for smaller d_0. To confirm this implication, more experiments on dependence on d_0 and growth time are necessary and left for future study.

5.3.4 Temperature Dependence of Indium Composition

Figure 5–4(a) shows alloy composition of NWs, plotted as a function of T_G with d_0 = 100 nm. The alloy compositions and their error bars were estimated from PL–peak–energy position and full width at half maximum (FWHM) [25]. It was found that NW composition is clearly dependent on T_G, where indium composition increases from 64% to 90% as T_G decreases. It is noted that this composition dependence on T_G is similar to that in the case of gallium–rich NWs (In_{supply} = 0.08) [23]. In Ref. [23], composition dependence on T_G was explained by arsenic trimers on the (111)B plane. As for GaAs, its (111)B surface was partially covered by arsenic trimer [26], and this stable coverage increases as temperature decreases [27]. The increase of this coverage hinders gallium atoms from absorbing onto the (111)B surface [8], while indium absorption is less influenced by arsenic trimers [11]. As a result, it became difficult for gallium atoms, compared to indium atoms to incorporate into the NW top facet. Simultaneously, h decrease as T_G decreases in gallium–rich InGaAs NWs as we have mentioned in **Section 3.2**. In addition, d_0 dependence of composition was absent for T_G = 590 and 650 °C (not shown here) in the present study, as reported in Ref. [23].

From h and composition dependence on T_G, the contributions of InAs and GaAs included to InGaAs NW height for d_0 = 100 nm were estimated (see **Figure 5–4(b)**). The Figure shows that InAs contribution is strongly dependent on T_G. On the other hand, the GaAs contribution is slightly dependent on T_G. This result suggests that the composition dependence on T_G is attributable to larger desorption of indium atoms compared with that of gallium atoms [11]. It is thus, we considered that, contrary to the case of gallium–rich NW growth,

composition dependence does not relate to arsenic trimers in the case of indium–rich NW growth.

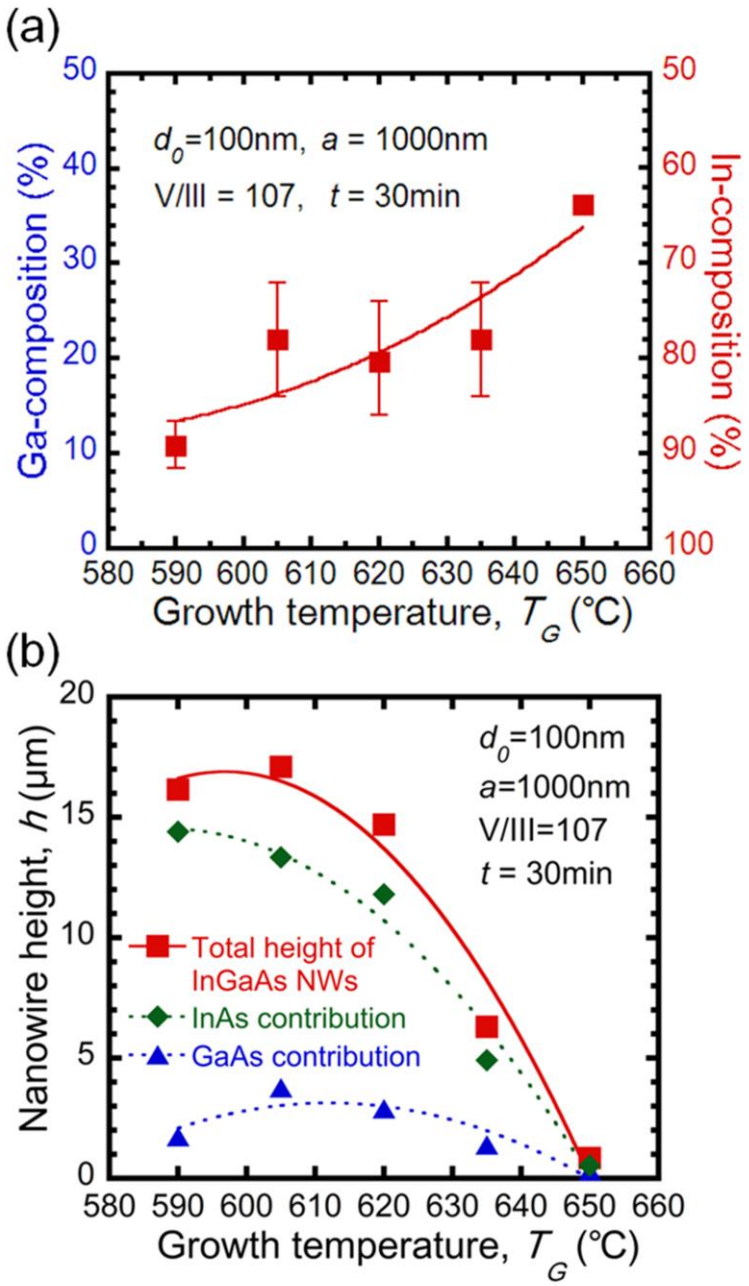

Figure 5–4

(a) Growth–temperature dependence of gallium (Ga) or indium (In) composition of InGaAs NWs. The error bar shows FWHM. (b) InAs and GaAs contributions in nanowire height, and total height of InGaAs NW. (t = 30 min; d_0 = 100nm)

5.4 Discussions

5.4.1 Composition–Dependent Growth Behavior

In the previous section, it was shown that indium–rich InGaAs NWs exhibited different growth behavior to that of gallium–rich NWs under varied growth temperature, T_G. When T_G increases, the axial (vertical) growth rate corresponded with NW height, h, reduced drastically in indium–rich NWs. This reduction is attributable to the InAs contribution, which indicates the less incorporation of indium. Meanwhile, the axial growth rate increases in gallium–rich NWs due to enhancement of GaAs growth at higher T_G. It is noted that these two behaviors are observed in the same T_G range, indicating that temperature dependence of the growth rate is significantly influenced by the group–III supply ratio, In_{supply}.

To further emphasize composition–dependent behavior, the axial growth rate for the InAs and GaAs NWs are compared with those for the indium–rich and gallium–rich InGaAs NWs in **Figure 5–5**. The data includes results from previous reports [10][11][23] and unpublished data for GaAs NWs. The axial growth rate is normalized with group–III supply. The lines are eye guides. Because the actual growth rate depends on various factors (for instance, V/III ratio, pitch a [8], and group–III supply ratio [21]), the vertical scale is shown as an arbitrary scale. As mentioned in the previous section, quite different trends in temperature dependence for the indium–rich and gallium–rich InGaAs NWs are shown. On the other hand, interestingly, common and systematic trends are confirmed in the cases of the InAs and GaAs NWs. That is, the axial growth rate increases as T_G increases until certain temperature, T_{GC}, above which axial growth rate decreases as T_G increases. T_{GC} for InAs and GaAs are about 540 and 700 °C, respectively.

In the higher T_G range (i.e., $T_G > T_{GC}$), highly uniform NWs were observed [10][11]. Furthermore, d was similar to d_0, indicating that the lateral growth was suppressed effectively. Note that the optimum growth temperature for InAs and GaAs NWs were thus concluded to be in about 540 and 750 °C, respectively. In addition, in this T_G range, axial growth rate decreases as T_G increases, where it is probably due to the fact that desorption of constituent atoms from the NW top facet increases as T_G increases [11]. In regard to GaAs NWs [10], this behavior was

explained by less incorporation of gallium due to reduced frequency of introduction of stacking faults. It is noted that less incorporation should be accompanied by desorption of constituent atoms in SA–MOVPE.

In the lower temperature range (i.e., $T_G < T_{GC}$), on the other hand, unfavorable growth was observed. In the case of InAs NWs [11], the uniformity of NWs was deteriorated, and considerable lateral overgrowth took place. This behavior is thought to be due to the preferential incorporation of growth species into the side walls of NWs, resulting in suppression of axial growth. On the other hand, in the growth of GaAs NWs at 650 °C, their height was much shorter than those grown at 700 °C, and hillocks or particle–like depositions were observed in some part of the mask opening. Reduction of axial growth rate can be explained by arsenic trimers, which prevents incorporation of gallium.

Because it is an alloy, the temperature dependence of the axial growth rate of InGaAs NWs has a peak as the cases of InAs and GaAs NWs, and it is plausible that growth behavior becomes closer to the case of InAs (GaAs) when the NWs are indium (gallium)–rich. Consequently, T_{GC} and growth behavior exhibited in InAs and GaAs NW growth exhibits a shift in accordance with In_{supply}. It explains an apparent opposite growth behavior in the cases of indium–rich and gallium–rich NWs, where it was observed in the same T_G range. Furthermore, it also explains the results presented in Ref. [21], which was carried out at fixed T_G and found that axial growth rate decreases as In_{supply} increases.

As discussed in **Section 5.3.1**, no particle–like depositions were observed in the present study, whereas they were observed in the case of gallium–rich NWs, even though both were grown in the same T_G range. As mentioned above, similar deposition was observed in GaAs grown at 650 °C, but it was eliminated above 700 °C. The formation or absence of particle–like depositions can be distinguished by the growth temperature, namely, whether it is below or above T_{GC}.

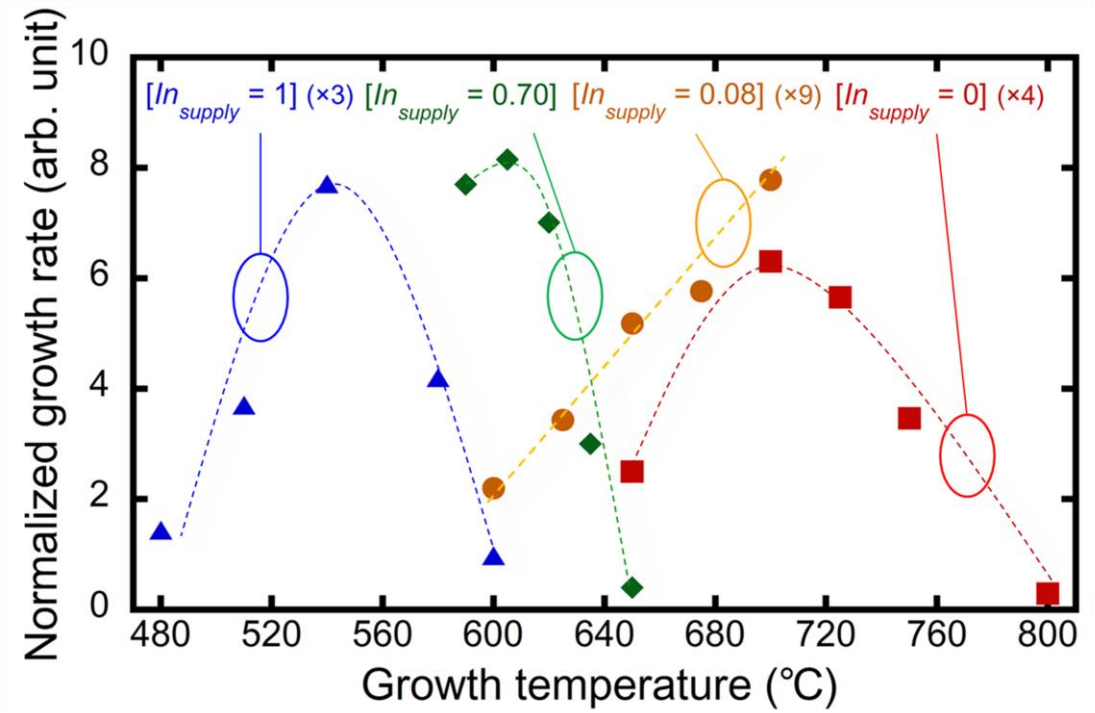

Figure 5–5

Comparison of temperature dependence of normalized axial growth rate. From the left side of the Figure, closed triangles, closed diamonds, closed circles, and closed squares, represent InAs NWs [11] (d_0 = 150 nm; a = 400 nm; t = 20 min), In–rich InGaAs NWs (present study, d_0 = 100 nm; a =1000 nm; t = 30 min), Ga–rich InGaAs NWs [23] (d_0 = 200 nm; a = 1000 nm; t = 30 min), and GaAs NWs [10] (d = 200 nm; a = 2000 nm; t = 10 min), i.e., In_{supply} = 1, 0.70, 0.08, and 0, respectively.

5.4.2 Optimum Growth Temperature for InGaAs Nanowires

As summarized in **Section 5.4.1**, axial growth rate of a NW depends both on T_G and group–III supply ratio, In_{supply}. This dependence is thought to be correlated with to the optimum growth temperature for InGaAs NW grown under any group–III supply condition. More specifically, it is expected that the optimum growth temperature for obtaining highly uniform and thinner NWs would be in a slightly higher temperature range than T_{GC}, where the axial growth rate is maximum, for the following reasons. For growth of NWs, it is important to achieve reasonably high growth rate. In addition, lateral growth should be suppressed to obtain sufficiently thin NWs. Furthermore, we have to avoid anomalous growth such as particle–like depositions or hillocks. The first requirement can be satisfied by employing a T_G close to T_{GC}, and the second and third ones require higher T_G. The result shown in Fig. 3 strongly suggests that it is possible to form NWs with sufficient length without lateral growth (i.e., d = 100 nm and h = 3 μm), so long as growth time (thus, h) is not long. In fact, the results of Fig. 3 are obtained for T_G = 635 °C, which is slightly above T_{GC}. Moreover, it was concluded empirically that optimum growth temperature for InAs and GaAs is the similar or higher than T_{GC} [10][11]. This fact also validates the present discussion on the relationship between T_{GC} and optimum growth temperature in NWs.

As shown in **Section 5.3.4**, indium composition decreases as T_G increases. In addition, composition also depends on mask pitch, a [21]. Further experiments are thus necessary for obtaining NWs with the desired alloy composition of InGaAs. Other growth conditions, such as V/III ratio, might also give some effect on the growth. Nevertheless, we expect that the qualitative trends summarized in **Section 5.4.1** does not alter and offer a good guiding principle to find the optimum growth conditions for InGaAs NWs across the whole alloy composition range.

5.5 Summary

Growth of InGaAs NWs under an indium–rich supply condition by SA–MOVPE was investigated, and highly uniform and non–tapered NWs were thereby formed. By comparison with previous reports on InAs, gallium–rich InGaAs, and GaAs NWs, it was found that the axial growth rate of InGaAs NWs becomes maximum at a certain temperature, T_{GC}, which decreases as group–III supply ratio, In_{supply}, increases. Furthermore, it is expected that the optimum growth temperature range for InGaAs NWs lies slightly above T_{GC}, where reasonable axial growth rate is guaranteed and lateral growth is negligible. To confirm this expectation, more systematic study on, for instance, dependences on V/III ratio, mask opening size, and opening pitch are required. In addition, temperature also affects the alloy composition of NWs; thus, more accurate assessment of growth condition is required to obtain InGaAs with desired composition.

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Chapter 6

Composition–Dependent Effect of V/III Ratio on Selective–Area Growth of InGaAs Nanowires

We grew gallium–rich (x > 0.50) and indium–rich (x < 0.50) $In_{1-x}Ga_xAs$ nanowires by catalyst–free selective–area metal–organic vapor–phase epitaxy (SA–MOVPE), and compared their growth dynamics dependence on V/III ratio. It was found that the growth dynamics of $In_{1-x}Ga_xAs$ nanowires is clearly dependent on the alloy composition x. Specifically, for gallium–rich nanowire growth, the axial growth rate of nanowires initially increased with decreasing V/III ratio, and then started to decrease when the V/III ratio continues to decrease below a critical value. On the other hand, axial growth rate of indium–rich nanowires monotonically decreased with decreasing V/III ratio. In addition, the alloy composition was strongly dependent on the V/III ratio for gallium–rich nanowire growth, while it was relatively independent of the V/III ratio for indium–rich nanowire growth. We discuss the origin of dissimilarity in the growth dynamics dependence on V/III ratio between gallium–rich and indium–rich InGaAs nanowire growth, and conclude that it is due to the inherent dissimilarity between GaAs and InAs. Our finding provides important guidelines for achieving precise control of the diameter, height, and alloy composition of nanowires suitable for future nanowire–based electronics.

6.1 Introduction

Interest in semiconductor nanowires (NWs) has been growing continuously because of their superior material properties as building blocks of novel electronic/photonic devices, such as field–effect transistors (FETs) and solar cells [1]–[4]. In particular, InGaAs NWs are very promising for various device applications [5]–[9] because of their high electron mobility, wide

tunability of bandgap energy, and good interface properties [10]. In addition, it is possible to grow high–quality $In_{1-x}Ga_xAs$ NWs ($0 \leq x \leq 1$) even in high–lattice–mismatch systems, such as $In_{1-x}Ga_xAs$ /GaAs [11] and $In_{1-x}Ga_xAs$/Si [5] owing to their small footprints [12]. To fully utilize these unique features of InGaAs NWs, precise control of their diameter, height, and alloy composition is essential. For example, thin NWs having high indium composition are required for FET applications [5], while thick NWs having high gallium composition are important for application to multijunction solar cells [9].

Recently, NWs grown by selective–area metal–organic vapor–phase epitaxy (SA–MOVPE) and their applications have been intensively reported [5][6][13][14]. SA–MOVPE is a versatile method of growing NWs and, compared with a catalyst–assisted vapor–liquid–solid (VLS) method [15][16], it offers the advantage of facilitating the growth of NWs at suitable predetermined positions without any assistance of catalysts. As for the growth of InGaAs NWs in SA–MOVPE, we have studied their growth dynamics [17]–[21]. For instance, the growth rate and alloy composition of InGaAs NWs were investigated as a function of group–III supply ratio at a fixed growth temperature [17][18].

On the other hand, it has been found that thereare some dissimilarity in the growth dynamics of GaAs [22][23] and InAs [24] NWs grown by SA–MOVPE. Specifically, the optimum growth temperature of GaAs and InAs NWs are different by about 200 °C. Moreover, the effect of V/III ratio is also clearly different between these NWs, where the higher V/III ratio results in the decrease and increase of axial growth rate of GaAs and InAs NWs, respectively. These results strongly suggested that the growth dynamics dependence on the growth temperature and V/III ratio of $In_{1-x}Ga_xAs$ NWs is directly connected with the alloy composition x and study of this issue is important to control their size and alloy composition.

In our previous paper, we have reported systematic studies on growth dynamics dependence on growth temperature of gallium–rich ($x > 0.50$) [19] and indium–rich ($x < 0.50$) [20] $In_{1-x}Ga_xAs$ NWs, and found out that the growth behavior and optimum growth temperature are clearly dependent on alloy composition of $In_{1-x}Ga_xAs$ NWs [20]. However, the growth dynamics dependence on the V/III ratio is not clear yet. In this report, we grew gallium–rich (x

> 0.50) and indium–rich (x < 0.50) $In_{1-x}Ga_xAs$ NWs by SA–MOVPE under various V/III ratios and compared their growth dynamics. It was found that the growth dynamics dependence on V/III ratio is clearly connected with the alloy composition. We discuss the origin of the dissimilarity in the growth dynamics on the V/III ratio between gallium–rich and indium–rich NW growth, and concluded that it originates from the inherent dissimilarities in the growth properties of GaAs and InAs. Our finding provides important guidelines for achieving precise control of the size and alloy composition of InGaAs NWs suitable for future NW–based electronics.

6.2 Experimental Details

The procedure of SA–MOVPE for fabricating InGaAs NWs is as follows. After the deposition of a 10–nm–thick SiO_2 film on a GaAs or InP substrate by RF sputtering, a periodic pattern of openings in a SiO_2 mask was defined by electron–beam lithography and reactive ion etching. The pattern consisted of circular holes with diameter, d_0, ranging from 100 to 300 nm and mask pitch, a, ranging from 200 nm to 5 μm. NWs were then formed by a horizontal MOVPE system operated at 0.1 atm with trimethylgallium (TMGa), trimethylindium (TMIn), and 20% arsine (AsH_3) diluted in hydrogen supplied as source materials. The total partial pressure of the group–III materials, [TMGa]+[TMIn] [25], of 2.33×10^{-6} atm and the growth time, t, of 30 min were constant. The partial pressure [AsH_3] of AsH_3 was varied from 0.63×10^{-4} to 5.0×10^{-4} atm, giving V/III ratios from 27 to 214.

The group–III supply (or gallium–supply) ratio was defined as Ga_{supply} = [TMGa]/([TMGa]+[TMIn]). For gallium–rich growth (i.e., Ga_{supply} = 0.87), we used a GaAs(111)B substrate and a growth temperature, T_G, of 695 °C. For indium–rich growth (i.e., Ga_{supply} = 0.30), we used an InP(111)B substrate and T_G of 635 °C. Different substrates were adopted for gallium–rich and indium–rich growth because of the large difference of T_G between these two cases. This large difference in T_G is required because the optimum T_G for obtaining highly uniform NWs is essentially dependent on Ga_{supply} [20]. Aside from the effect of adopting different growth temperatures, we believeconsider that the use of different substrates does not

significantly change the growth dynamics of InGaAs NWs, since the lattice mismatch between the substrate and InGaAs is less than about 2.5% and 2.2% for gallium–rich and indium–rich NWs, respectively in the present study, and their effect can be considered even less important because of the small footprint of NWs [12]. It is also worth mentioning that the exploration of composition–dependent growth dynamics is possible with NW growth but is not straightforward with planar layer growth, because the lattice mismatch between the substrate and epitaxial layer is a critical issue in the latter case.

The alloy composition of InGaAs NWs was estimated by micro–photoluminescence (μ–PL) measurements at 4.2 K [18]–[20],[26].

6.3 Experimental Results

6.3.1 Growth of Gallium–Rich InGaAs Nanowires

Figure 6–1 shows a SEM image of InGaAs NWs for Ga_{supply} = 0.87, d_0 = 100 nm, a = 1 μm, and V/III = 107. Their diameter, d, and height, h, were 250 nm and 2.7 μm, respectively. We obtained highly uniform NWs owing to precise tuning of T_G to the optimum value [20]. InGaAs NWs have with six {–110} side facets normal to the (111)B plane [17]–[24], as well as NWs obtained under other growth conditions.

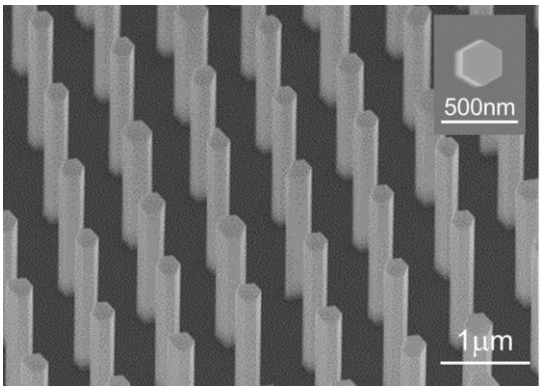

Figure 6–1
30°–tilted SEM image of gallium–rich InGaAs nanowires (Ga_{supply} = 0.87, d_0 = 100 nm, a = 1 μm, V/III = 107). The inset shows an enlarged view of the top of a nanowire.

Figure 6–2(a) and **Figure 6–2(b)** show the dependence of *d* and *h* on the V/III ratio for various mask pitches, *a*. We can see that *d* monotonically decreased to d_0 as the V/III ratio decreased. It is likely that the reduction of adsorption sites for gallium and indium on the {–110} facet was promoted by reducing the arsenic supply in relatively high temperature growth [27]. On the other hand, *h* increased to a maximum value as the V/III ratio decreased, and then decreased with subsequent decreasing of the V/III ratio. A similar trend was observed for the other values of d_0 (not shown here). In addition, the V/III ratio with the maximum *h* depended

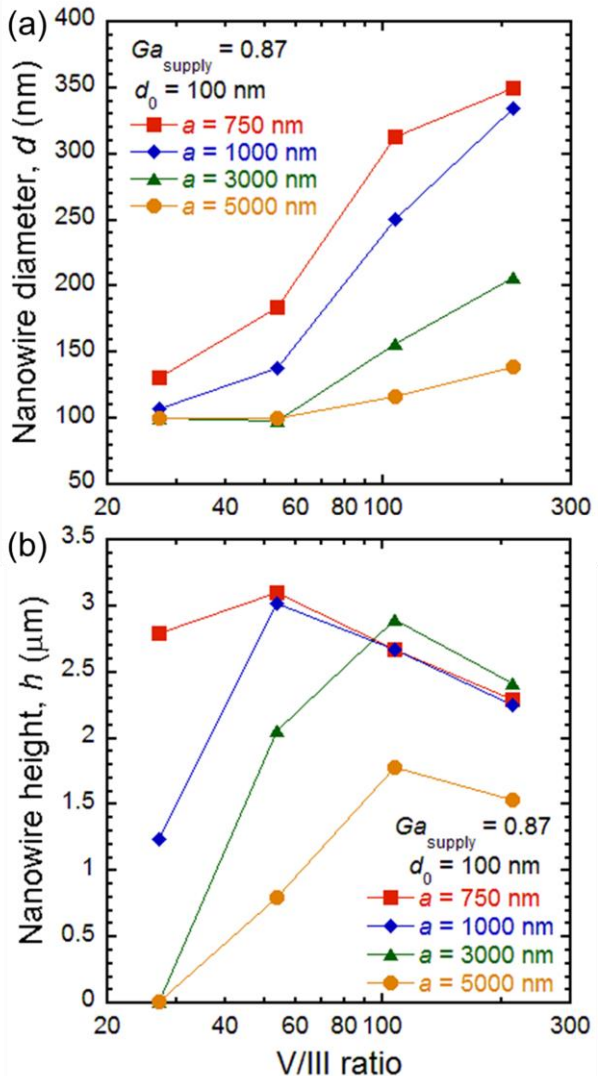

Figure 6–2

V/III ratio dependence of (a) nanowire diameter, *d*, and (b) nanowire height, *h*, for gallium–rich InGaAs nanowires for various mask pitches, *a* (Ga_{supply} = 0.87).

on *a*, i.e., it was approximately 54 for small *a* (i.e., *a* = 750 nm and 1 μm) and approximately 107 for large *a* (i.e., *a* = 3 and 5 μm).

Figure 6–3 shows the alloy composition of gallium–rich InGaAs NWs estimated from μ–PL measurements plotted as a function of V/III ratio. It was found that the gallium composition of NWs increased with decreasing V/III ratio for various values of *a*. The gallium composition increased from 71% to 82% as the V/III ratio decreased from 214 to 54 for *a* = 1000 nm. The gallium composition was nearly independent of d_0 (not shown here), which is consistent with our previous report [19]. In addition, when *a* became larger, the gallium composition increased more rapidly with decreasing V/III ratio. As a result, the trend of the relationship between the gallium composition and *a* was changed by modulating the V/III ratio, as shown in the inset of **Figure 6–3**. Note that these trends confirmed for V/III = 27 and 54 are opposite to those obtained in previous reports [18][19], where the gallium composition increased as *a* decreased.

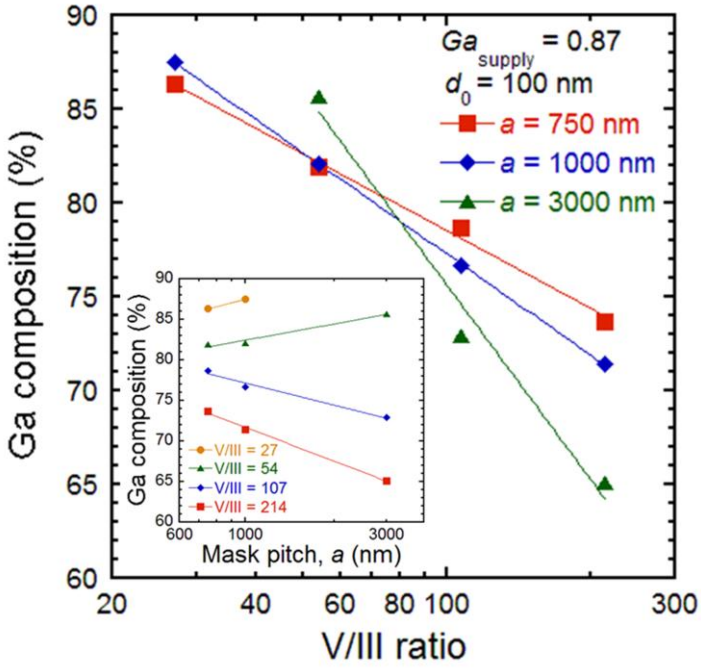

Figure 6–3

V/III ratio dependence of estimated gallium (Ga) composition of gallium–rich InGaAs nanowires (Ga_{supply} = 0.87). The inset shows the Ga composition of nanowires re–plotted as a function of mask pitch, *a*.

6.3.2 Growth of Indium–Rich InGaAs Nanowires

Highly uniform NWs with six {–110} side facets normal to the (111)B plane were obtained for indium–rich growth, as shown in **Figure 5–1(c)** (Ga_{supply} = 0.30). Their diameter, *d*, and height, *h*, were 190 nm and 6.3 μm, respectively.

Figure 6–4(a) shows the V/III ratio dependence of *d* and *h* for indium–rich growth. Both *d* and *h* monotonically decreased with decreasing V/III ratio, and similar trends were

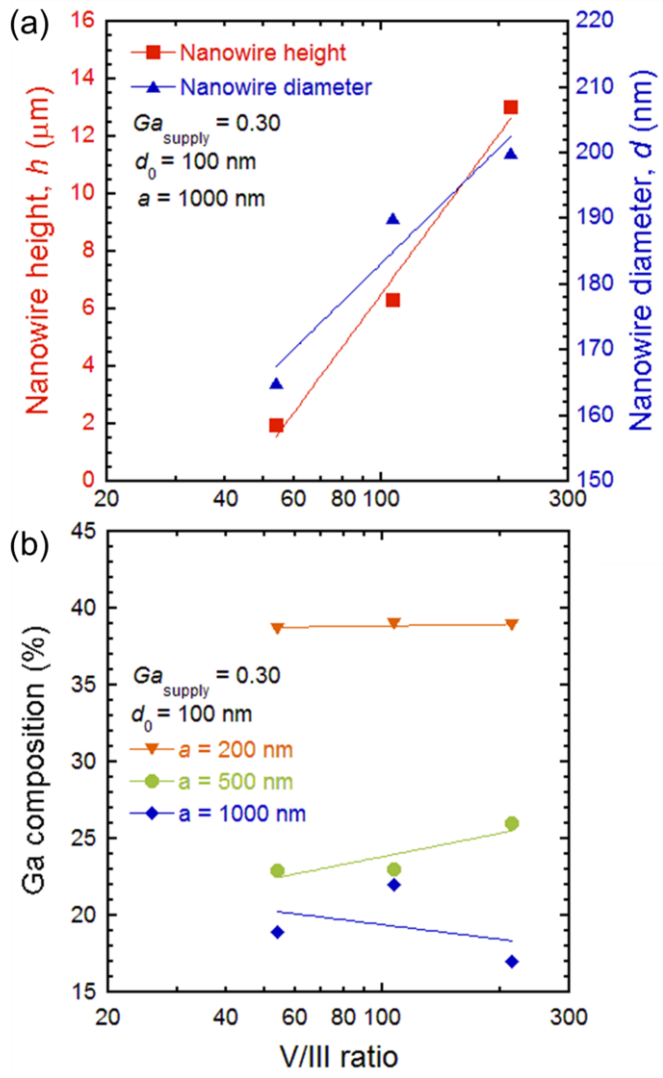

Figure 6–4

V/III ratio dependence for indium–rich InGaAs nanowires (Ga_{supply} = 0.30). (a) V/III ratio dependence of nanowire height, *h*, and nanowire diameter, *d*. (b) V/III ratio dependence of the alloy composition.

confirmed for the other *a* (not shown here). This is probably due to the reduced incorporation of growth species upon reducing the V/III ratio. Note here that this trend of *h* is different from that observed for gallium–rich growth described in the previous section, where *h* increases to a maximum value as the V/III ratio decreases, and then decreases with decreasing V/III ratio.

Figure 6–4(b) shows the gallium composition of indium–rich InGaAs NWs plotted as a function of the V/III ratio. It was found that the gallium composition varied less than 5% with modulating the V/III ratio from 214 to 54 for a = 1000 nm. This variation is less than that for gallium–rich NW growth, where the variation of gallium composition is 11 % for gallium–rich case. In addition, we could not confirm clear dependence of the gallium composition on V/III ratio for indium–rich growth. It is different from that for gallium–rich growth, where the gallium composition is strongly dependent on the V/III ratio, and the relationship between gallium composition and *a* changed with the V/III ratio.

6.4 Discussions

6.4.1 Effects of V/III Ratio on InGaAs Nanowire Growth

We have shown the composition–dependent growth dynamics on the growth temperature of InGaAs NWs [19][20]. The present study also revealed that dissimilarity in the effect of the V/III ratio between gallium–rich and indium–rich NW growth. In this section, to clarify the origin of this dissimilarity, we firstly discuss the effect of the V/III ratio, focusing on the case of gallium–rich growth, because *h* and the alloy composition of NWs exhibited distinctive trends.

For this purpose, we estimated the contributions of GaAs and InAs included in InGaAs NWs based on *d*, *h*, and the gallium composition shown in **Figure 6–2** and **Figure 6–3**. The results are summarized in **Figure 6–5(a)** and **Figure 6–5(b)**, and these show contributions of GaAs and InAs for *d* (d_{GaAs} and d_{InAs}) and those for *h* (h_{GaAs} and h_{InAs}), respectively, for d_0 = 100 nm and a = 1000 nm. Both d_{GaAs} and d_{InAs} monotonically increased as the V/III ratio increased. On the other hand, these contributions for *h* showed unique trends. That is, h_{InAs} showed monotonic increase with increasing V/III ratio, whereas h_{GaAs} started to decrease above a critical

V/III ratio. A similar trend was also found for other values of *a* in NW growth.

We separate the above dependence into regime A and regime B as shown in **Figure 6–5**. The boundary is set at the V/III ratio where *h* or h_{GaAs} is maximum, that is, the V/III ratio of 54 for *a* = 1000 nm. As **Figure 6–2(b)** shows, the critical V/III ratio increases as *a* increases. The difference in the V/III ratio dependence of the contributions of GaAs and InAs in each regime is explained as follows.

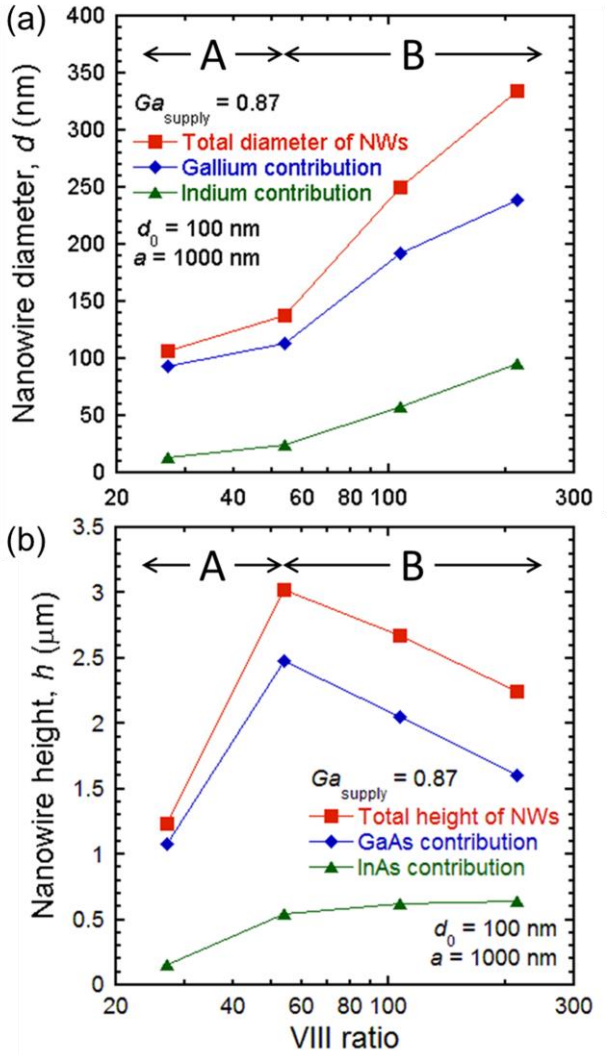

Figure 6–5

Contributions of GaAs and InAs included in total (a) diameter and (b) height of gallium–rich InGaAs NWs for Gasupply = 0.87, d_0 = 100 nm and *a* = 1000 nm.

In regime A, d_{GaAs}, d_{InAs}, h_{GaAs}, and h_{InAs} decreased as the V/III ratio decreased, whereas the gallium composition of NWs increased. Let us recall that T_G was 695 °C in the present study, and regime A is the region where the V/III ratio is lower than 54 for a = 1000 nm. This value of T_G is very high for InAs NW growth, and the V/III ratio is low for both InAs and GaAs NW growth [22][24]. In these conditions, desorption of indium and gallium takes place easily. In particular, the desorption of indium atoms is more enhanced than that of gallium atoms as the V/III ratio decreases due to relatively high T_G [28][29]. Consequently, d and h decreases and the gallium composition increases upon reducing the V/III ratio in regime A.

In regime B, both d_{GaAs} and d_{InAs} decreased as V/III ratio decreased, and this can be explained simply by the desorption from {–110} NW side facets. On the other hand, h_{GaAs} increased upon reducing the V/III ratio, and h_{InAs} slightly decreased or was nearly independent of the V/III ratio. This can be explained by the coverage of arsenic trimers on the (111)B surface [30][31], and its different effects on the adsorption of gallium and indium, as suggested by Yoshimura *et al* [19].

In planar GaAs growth, the stable arsenic trimers on GaAs(111)B prohibit the incorporation of gallium atoms [30], and their coverage increases at a low T_G and high V/III ratio [31]. This is also true for GaAs NW growth; thus, the axial growth rate decreases when T_G is low and the V/III ratio is high [22][23]. On the other hand, the axial growth rate of InAs NWs was not suppressed with increasing arsenic supply or V/III ratio [24]. This result suggested that the arsenic trimers are thought to have less effect on the incorporation of InAs. Rather, desorption of indium becomes more important with decreasing V/III ratio owing to the relatively high T_G. Thus, even with the increase in h_{GaAs}, the indium composition in InGaAs NWs monotonically decreases with decreasing V/III ratio in regime B.

The transition from regime A to B with increasing V/III ratio indicates on increase in gallium desorption or a decrease in gallium adsorption and incorporation. This transition is thought to take place continuously with modulation of the V/III ratio, and the boundary is determined by the balance between these two competing phenomena for gallium. Thus, the critical point should be dependent on the growth temperature or other growth parameters.

On the bases of the above understanding, the effect of *a* on the axial growth rate and gallium composition can be explained as follows. Because the re–evaporation of the supplied group–III elements was more prominent for larger *a* owing to the relatively high growth temperature, the effective V/III ratio at a single mask opening is high when *a* is large [21]. Thus, when the V/III ratio is modulated, the magnitude of change in the effective V/III ratio is larger for larger *a*. Because of the smaller amount of group–III elements and the higher sensitivity to a change in the V/III ratio for larger *a*, the desorption of adatoms occurs easily, resulting in a higher critical V/III ratio, and the gallium composition changes by a larger magnitude for larger *a*.

6.4.2 Composition–Dependent Growth Dynamics

In this section, we explain the origin of dissimilarity in the growth dynamics on V/III ratio between gallium–rich and indium–rich NW growth. The most distinct difference between these NW growths is the presence of regime B, where arsenic trimers play an important role in the incorporation of gallium and indium. In other words, the reason for the absence of regime B for indium–rich NW growth is thought to be due to the reduced Ga_{supply}, that is, the growth behavior becomes closer to that of InAs NWs [24] in indium–rich growth [20].

To be more specific, the stability of the arsenic–terminated surface and arsenic trimers is dependent on the composition of $In_{1-x}Ga_xAs$, and the difference in the strength of adsorption to arsenic between gallium and indium is also composition–dependent. It is not clear how the strength of the interatomic bonding between arsenic, which is necessary to form arsenic trimers, changes with the presence of gallium and indium. Nevertheless, since all of our experimental results suggest that indium reduces the binding strength of As–As, it is natural to consider that arsenic trimers have less effect on gallium incorporation into the (111)B surface of indium–rich InGaAs.

Another difference in the growth dynamics between gallium–rich and indium–rich NW growth is gallium composition dependence on V/III ratio. It showed strong dependence for former case, while we could not confirm clear dependence on V/III ratio for latter case. These

can be explained on the basis of aforementioned different adsorption natures of gallium and indium on an arsenic–terminated (111)B surface and stability of arsenic–trimers depending on Ga_{supply}. In addition, we can also consider that this dissimilarity originates from the difference in T_G. Because the optimum T_G for obtaining highly uniform NWs is essentially dependent on Ga_{supply} [20], T_G for indium–rich growth is lower than that for gallium–rich growth. Under the low T_G, the incorporation of indium atoms should be enhanced, and thus it can be expected that the alloy composition is less affected by the V/III ratio in indium–rich NW growth [32][33].

Note that the above dissimilarity in the growth dynamics on V/III ratio between gallium–rich and indium–rich InGaAs NWs originated from inherent dissimilarities between the material properties of GaAs and InAs. Although both GaAs and InAs are III–V semiconductors with the zincblende crystal structure and, they thus have similar faces, there are large differences in their atomic and material properties, such as atomic radii and the bonding strength between Ga–As and In–As [34]. One of the largest differences is in the bonding length or lattice constant, which is about 7%. This makes the growth of high–quality InGaAs thin films with an arbitrary alloy composition difficult. For NWs, such constraints originating from lattice mismatch are more or less relieved, but there is still the problem of a large difference in the T_G and properties of growth surface of NWs. This, in turn, means that our series of studies on the growth of InGaAs NWs under various growth conditions is vital in order to obtain precisely size– and composition–controlled NWs required for applications such as FETs and solar cells. Thus, knowledge of the composition–dependent growth dynamics in terms of the V/III ratio will also provide important guidelines for achieving future NW–based electronics and understanding the growth mechanism of other mixed crystal semiconductor NWs.

6.5 Summary

Gallium–rich and indium–rich InGaAs NWs were grown by SA–MOVPE under various V/III ratio conditions, and the growth dynamics of these NWs was compared. It was found that the growth dynamics on V/III ratio is clearly dependent on the alloy composition of InGaAs and/or Ga_{supply}. In particular, *d*, *h*, and the alloy composition of NWs were strongly affected by V/III ratio, and exhibited distinctive trend for gallium–rich growth. This likely originates from the difference in effect of the arsenic–terminated (111)B NW top facet on the incorporation of gallium and indium, and/or difference in adsorption/desorption nature of these atoms in high growth temperature. Furthermore, these growth dynamics are dissimilar from those of indium–rich growth. It was suggested that the growth dynamics on V/III ratio depends on Ga_{supply} and is due to the inherent dissimilarity of GaAs and InAs. Understanding such composition–dependent growth dynamics will provide important guidelines for achieving future NW–based electronics and understanding the growth mechanism of other mixed crystal semiconductor NWs.

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Chapter 7

Pitch–Independent Realization of 30–nm–Diameter InGaAs Nanowires by Two–Step Growth Method

Control of the diameter and pitch of InGaAs nanowire arrays in selective–area metal–organic vapor–phase epitaxy was investigated. It was found that their nucleation was strongly dependent on the geometry of the mask, resulting in the difficulty of nucleation for a larger mask pitch, particularly for an opening diameter of less than 50 nm. Precise adjustment of the V/III ratio enabled us to control the nucleation independently of the mask pitch for smaller openings, and we successfully obtained 30–nm–diameter InGaAs nanowires independently of the mask pitch by the proposing V/III–ratio–controlled two–step growth method.

7.1 Introduction

Free–standing semiconductor nanowires (NWs) show promise for use in future electronic/photonic devices, such as field–effect transistors (FETs), light emitting diodes, single–photon sources, and so forth [1]–[3]. To realize such device applications, the reduction of NW diameter is particularly important to avoid introducing misfit dislocations in lattice–mismatched systems as well as to improve the performance of devices [4]. In addition, it is necessary to freely control the position and spacing of NWs depending on the application. For instance, FET applications require small pitch (or spacing) between the NWs for designing the integrated circuit, while for single–photon source applications, larger pitch (e.g., pitch $\geq$ 3 μm) is required to utilize pure single–photon by driving the single NW including single quantum dot.

Recently, NWs grown by catalyst–free selective–area metalorganic vapor–phase epitaxy (SA–MOVPE) and their device applications have intensively been reported [5]–[12]. Among them, InGaAs NWs are a very promising for various applications because of their high electron mobility and good interface properties [9]–[12]. These properties as well as the bandgap energy can be controlled by adjusting the alloy composition of InGaAs. However, previously reported InGaAs NW arrays in SA–MOVPE were limited to NW diameters of larger than 50 nm [9]–[12], and further reduction of the NW diameter is required, for instance, to suppress short–channel effects for FET applications or to form a single quantum dot in NWs with strong lateral quantum confinement. In addition, the growth of thin NWs with diameter of ~ 30 nm and control of their pitch have not been reported. In this letter, we report on the reduction of the diameter of InGaAs NWs to close to 30 nm and control of their pitch in SA–MOVPE. It was found that the nucleation and growth of NWs are strongly dependent on the geometry of the mask for SA–MOVPE, that is, the opening diameter, d_0, of the mask openings, and their pitch, a, as well as V/III ratio. In particular, when $d_0 < 50$ nm and $a > 1$ μm, nucleation was strongly suppressed for high V/III ratio, while the growth rate is very low at low V/III ratio. We discuss the origin of these growth behaviors and clarify the procedure for growing 30–nm–diameter InGaAs NWs independently of the mask pitch.

7.2 Experimental Details

The SA–MOVPE procedure for fabricating InGaAs NWs is explained as follows. After a 10–nm–thick SiO_2 film was deposited on a GaAs (111)B substrate by RF sputtering, a periodic pattern of openings in a SiO_2 mask was defined by electron–beam lithography and reactive ion etching. d_0 and a were varied from 30 to 100 nm, and from 750 nm to 5 μm, respectively. NWs were then formed using a low–pressure horizontal MOVPE system, supplying trimethylgallium (TMGa), trimethylindium (TMIn), and 20% arsine (AsH_3) diluted in hydrogen as source materials. The partial pressures of TMGa [TMGa] and TMIn [TMIn] were 2.03×10^{-6} and 0.30×10^{-6} atm [13], respectively, giving a [TMGa] to [TMIn] ratio of 87:13, and the growth time, t, was 30 min unless otherwise specified. The partial pressure of AsH_3, [AsH_3] was varied from 0.63×10^{-4} to 5.0×10^{-4} atm, giving a V/III ratio of 27 to 214. The growth

temperature, T_G, was 695 °C and kept constant throughout the experiment to minimize the variation of the alloy composition in InGaAs [9].

7.3 Experimental Results

7.3.1 Conventional Optimum Growth Condition

Figure 7–1 shows SEM images of InGaAs NWs with d_0 = 50 nm and a = 3 μm. The V/III ratio was 107, which, according to our previous reports, is the optimum value for obtaining highly uniform NWs while minimizing radial growth [9]. We can observe highly uniform NWs having six {–110} side facets normal to the (111)B plane. The height of the NWs, h, is 3.5 μm, and their gallium composition was 77%, estimated by micro–photoluminescence measurements at 4.2 K [12]. The NW diameter, d, was larger than d_0 and was 120 nm. This is due to radial growth, which becomes prominent above a critical growth time or height [9]; d can be reduced to close to d_0 when an appropriate growth time is used.

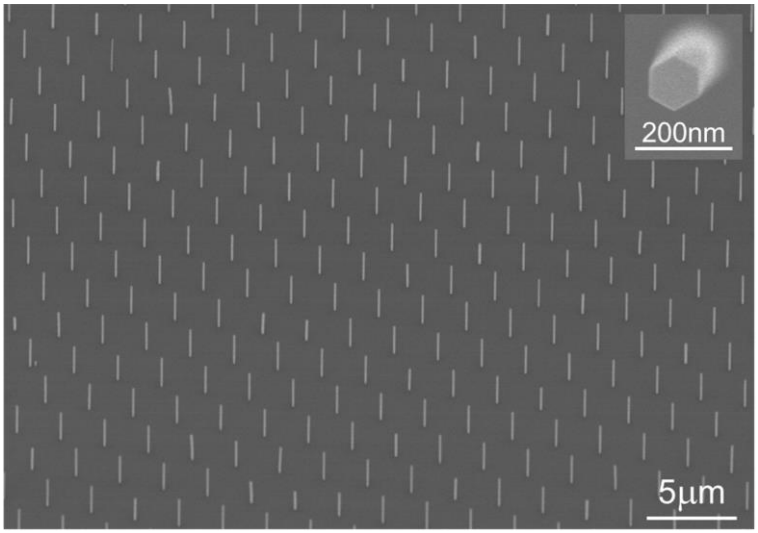

Figure 7–1

30°–tilted SEM images of InGaAs nanowires grown on GaAs (111)B substrate (d_0 = 50 nm, a = 3μm, V/III = 107, t = 30 min). The inset shows an enlarged view of the top of a nanowire.

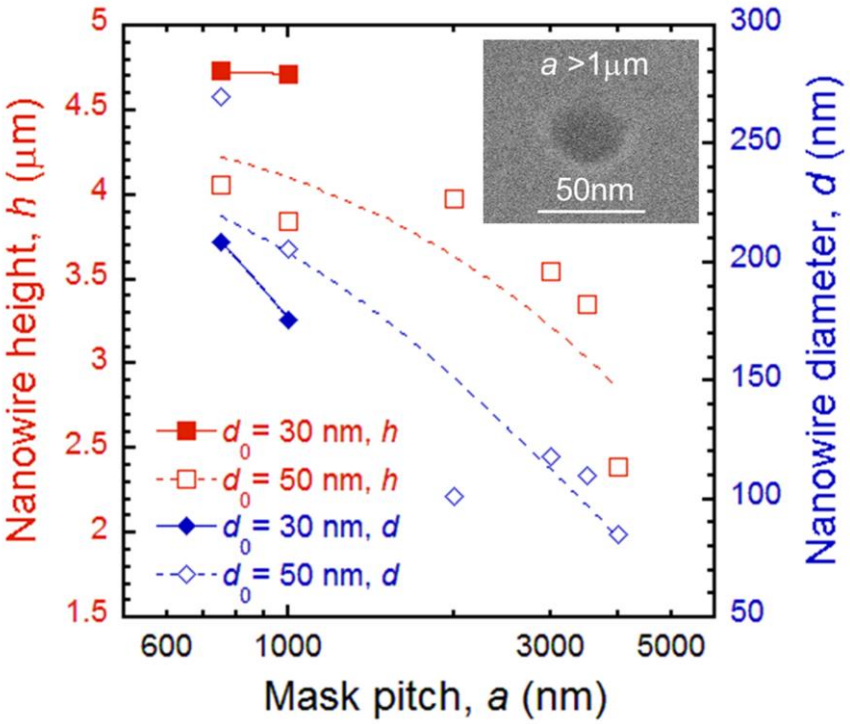

Figure 7–2

Mask pitch dependence of nanowire height, h, and nanowire diameter, d, (d_0 = 30, 50 nm, V/III = 107, t = 30 min). The inset is an SEM image of one example of a mask opening after the InGaAs growth (d_0 = 30 nm, a > 1μm).

Figure 7–2 shows the mask pitch dependence of d and h for d_0 = 30 and 50 nm and V/III = 107. NW growth was confirmed to be independent of a when d_0 was 50 nm except when a was 5 μm. In addition, for d_0 = 50 nm, both h and d decrease as a increases, namely, the volume of InGaAs NWs was also reduced for larger a. Such growth behavior has been reported for GaAs NWs and InP NWs in SA–MOVPE [14][15], and the present InGaAs NW growth is in the synergetic growth mode [16]. That is, the re–evaporation of precursors (or desorption of atoms) is important owing to the relatively high growth temperature [15], but they are re–incorporated and contribute more to the axial and radial growth of NWs for higher–density NW arrays or for the case of a smaller a. On the other hand, for d_0 = 30 nm, there was no growth of InGaAs when a exceeded 1 μm as shown in the inset of **Figure 7–2**. Note that when d_0 was 100 nm, NW growth was confirmed for a = 5 μm (not shown here). These results indicate that the nucleation and growth of InGaAs are clearly dependent on a as well as d_0.

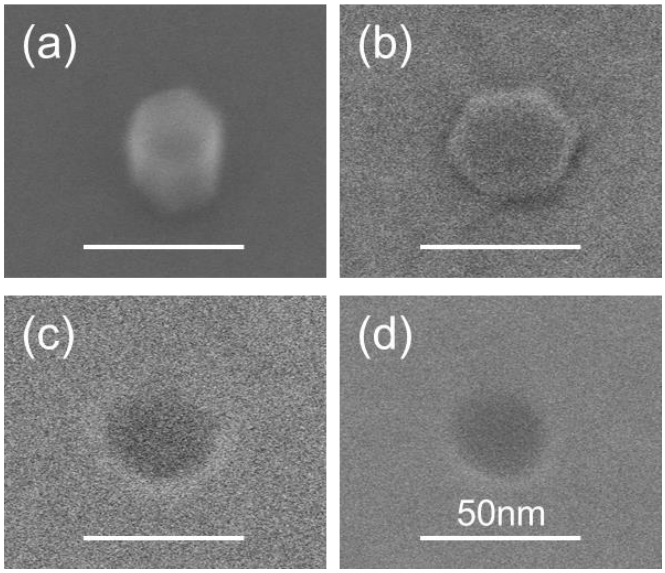

Figure 7–3

(a), (b), (c), and (d) show 30°–tilted SEM images of a patterned substrate after the growth of InGaAs. The V/III ratios were (a) 27, (b) 54, (c) 107, and (d) 214, respectively (d_0 = 30 nm, a = 3μm, t = 30 min).

7.3.2 Effects of V/III Ratio on Nucleation

To control the nucleation and axial/radial growth rate of InGaAs, we investigated the V/III ratio dependence for d_0 = 30 nm and a = 3 μm, and the results are summarized in **Figure 7–3**. The growth of InGaAs with high uniformity was confirmed in almost all the mask openings for a V/III ratio of up to 54. In addition, the amount of growth of InGaAs slightly increases as the V/III ratio decreases. Similar growth behavior was also confirmed for a = 2, 4, and 5 μm. Note, however, that the growth height of InGaAs is very low even after the 30 min growth.

7.4 Discussions

7.4.1 Effects of V/III Ratio on Axial Growth Rate

Aforementioned results can be explained as follows. Firstly, the nucleation of InGaAs in the mask openings is less probable for smaller d_0. Secondly, the effective supply of gallium and indium at a mask opening is dependent on a. Thirdly, the nucleation is also influenced by the effective V/III ratio at a mask opening. Because the growth temperature was relatively high, the group–III supply from the masked area to a mask opening was reduced as a result of re–evaporation [15], and the reduction of group–III supply was more prominent for larger a. Thus, the effective V/III ratio increases for larger a, while a higher effective V/III ratio prevents nucleation owing to the increased coverage of the arsenic–trimer on the GaAs (111)B surface [17]. These factors result in the difficulty of nucleation as d_0 becomes smaller and a becomes larger.

To study the effect of the V/III ratio on the axial growth rate, we plotted h and d for d_0 = 30 nm and a = 750 nm and 1 μm as a function of V/III ratio, as shown in **Figure 7–4**. The value of d decreases as the V/III ratio decreases. In addition, the axial growth rate was greatest when the V/III ratio was 107, which is thought to be optimum for $d_0 \geq 50$ nm and $a \sim 3$ μm. However, the axial growth rate rapidly decreased for V/III $\leq$ 54, and the NW height also becomes short, as shown in **Figure 7–3(a)**. This suggests that the desorption of InGaAs from the (111)B NW top facet was significantly enhanced upon reducing the V/III ratio, while enhancing the nucleation on the GaAs (111)B surface, and this effect is enhanced for smaller d_0. Consequently, it is difficult to obtain NWs of sufficient length with $d \sim 30$ nm by the simple manipulation of the V/III ratio.

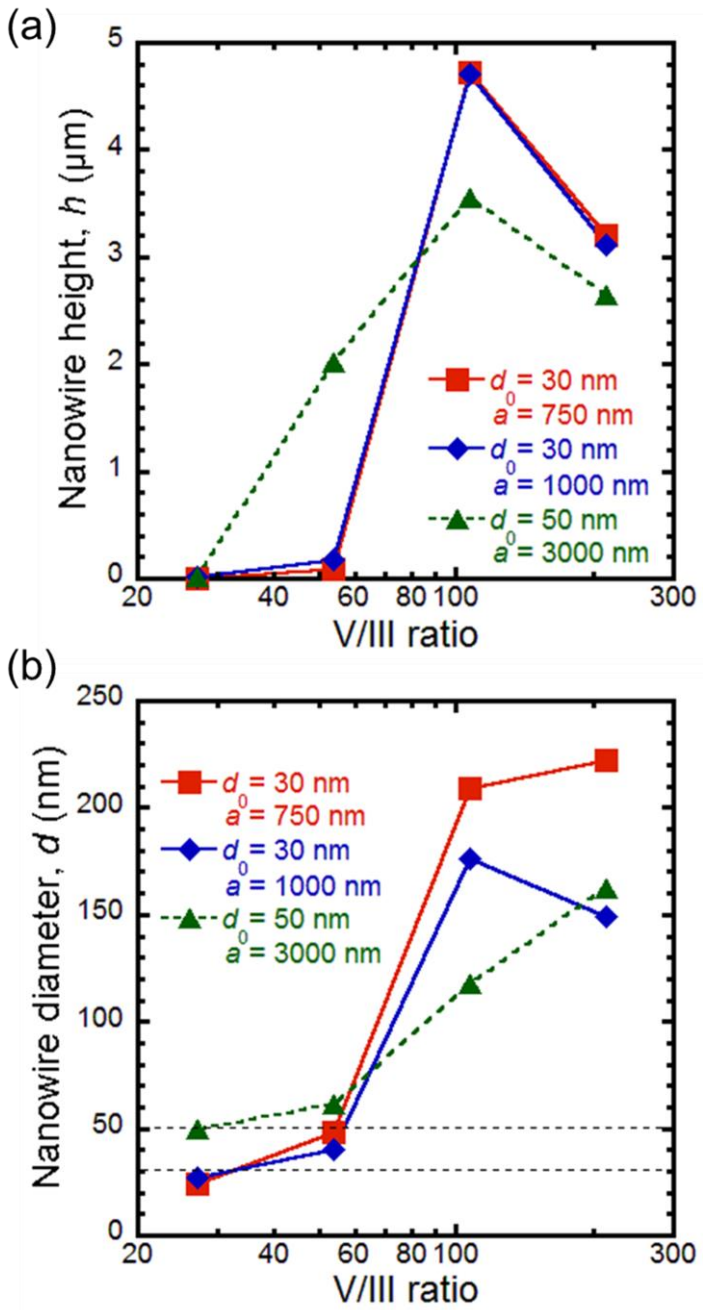

Figure 7–4

(a) and (b) show the V/III ratio dependence of nanowire height, h, and diameter, d, for d_0 = 30 nm and t = 30 min with various mask pitch, a (data for d_0 = 50 nm and a = 3 μm are shown as a reference.). The upper and lower dashed lines in (b) show d_0 = 50 and 30 nm.

7.4.2 Two–Step Growth Method

On the basis of the above understanding, we grew NW arrays with d ~ 30 nm by adopting the two–step growth sequence shown in **Figure 7–5**. Here, the V/III ratio for the first step was set to 9.1 to enhance the nucleation in the initial stage, and it was set to 107 for the second step to enhance the axial growth and minimize the radial growth. The result is shown in **Figure 7–6**. We successfully obtained highly uniform NWs without any radial growth with d_0 = 30 nm and a = 3 μm. Similar NWs were also obtained for other values of a, where radial growth was limited to a few nm as shown in **Figure 7–7**. These results suggest that the nucleation and axial/radial growth rate can be controlled independently of a by using our two–step growth method.

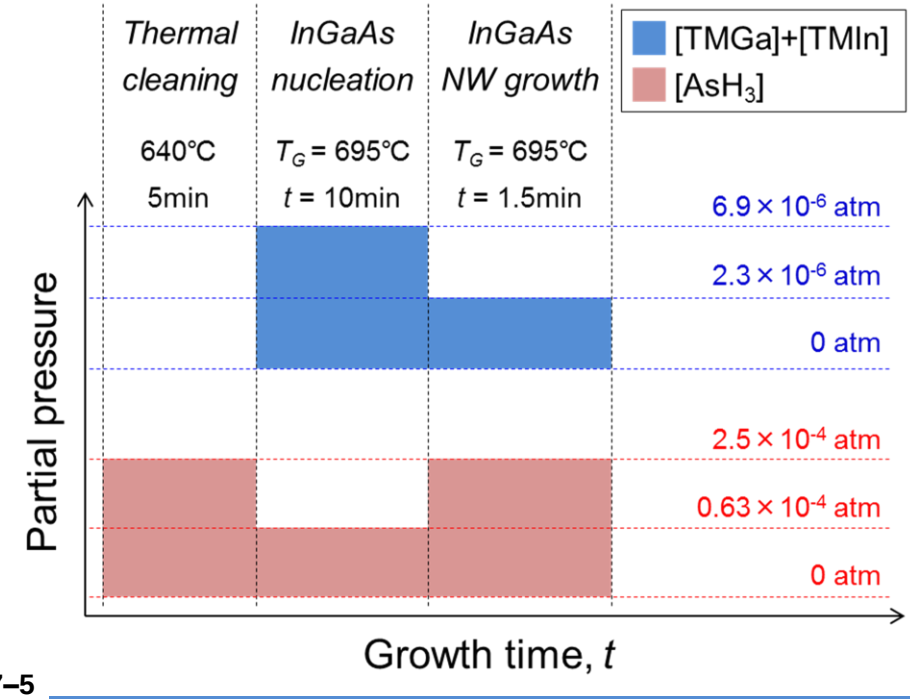

Figure 7–5

Schematic diagram of the two–step growth sequence.

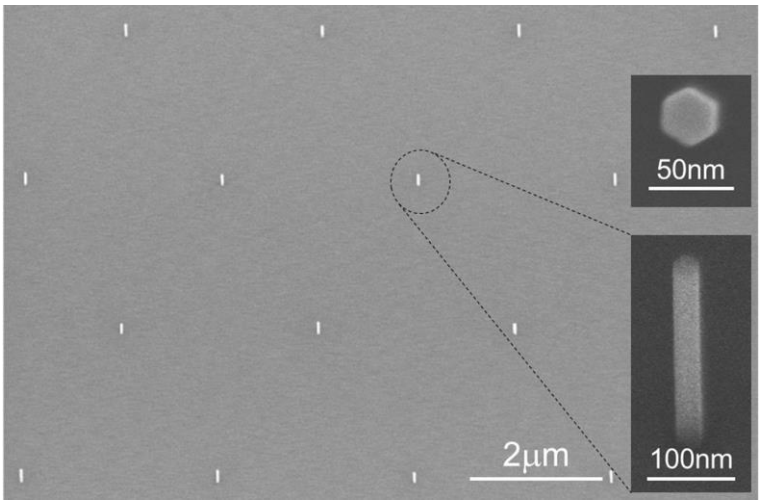

Figure 7–6

30°–tilted SEM images of InGaAs nanowires grown by the two–step growth method (d_0 = 30 nm, a = 3 μm). The upper and lower insets show an enlarged view of the nanowire top and a 30°–tilted image of a nanowire, respectively.

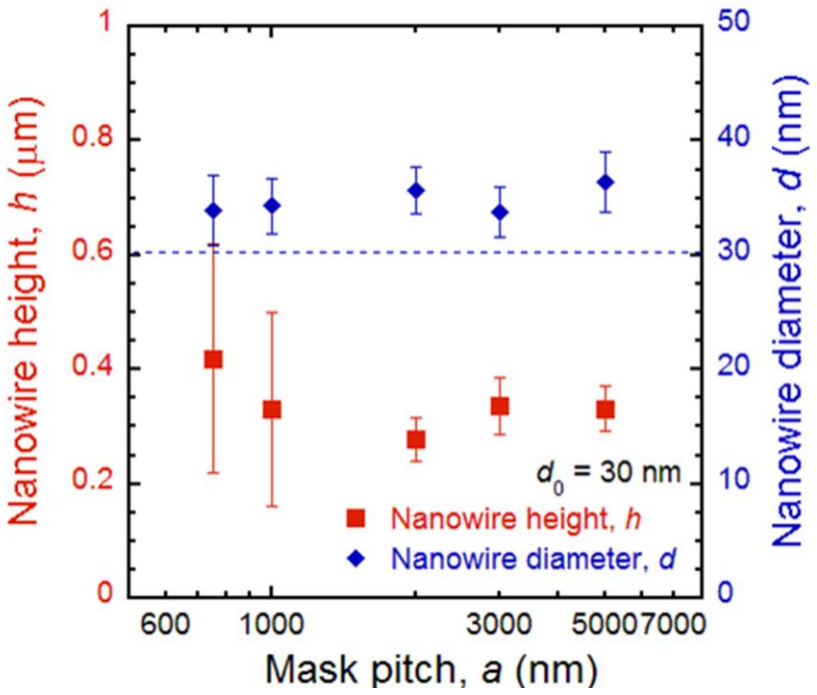

Figure 7–7

Nanowire height, h and nanowire diameter, d, are plotted as a function of mask pitch, a, for d_0 = 30 nm. The error bars show standard deviation of h and d. The blue dashed line shows d = 30 nm.

7.5 Summary

In summary, the control of the diameter and pitch of InGaAs NW arrays on a GaAs (111)B substrate in SA–MOVPE were investigated. We found that the nucleation and growth were strongly dependent on d_0 and a, especially for $d_0 < 50$ nm. Our V/III–ratio–controlled two–step growth method enabled us to control the nucleation and axial/radial growth rate. As a result, we successfully obtained 30–nm–diameter InGaAs NW arrays independently of the mask pitch. These results are expected to contribute to realizing much finer and various high–quality axial heterostructure NWs independently of their location.

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Chapter 8

Lateral Metal–Insulator–Semiconductor Field–Effect Transistors using Selectively–Grown Single InGaAs Nanowire

We report on electrical characterization of single InGaAs nanowire channel metal–insulator–semiconductor field–effect–transistors fabricated by gate–last and gate–dielectric–first process. Unintentionally–doped InGaAs nanowires were grown by selective–area metal–organic vapor–phase epitaxy, and horizontally scattered InGaAs nanowires were used as a channel of transistors. The transistors fabricated by gate–last process exhibited maximum drain current ($I_{DS,max}/w_G$), 87 mA/mm, and this value is much larger than those of previously reported *n*–InGaAs nanowire metal–semiconductor field–effect–transistors and InAs vertical surrounding–gate transistors. However, we could not obtain completely off behavior for the transistors fabricated by gate–last process. This is probably because of process–induced damages at the surface of nanowire channel. For improving off behavior of transistors, we attempted alternative fabrication process (i.e., gate–dielectric–first process). The transistors fabricated by gate–dielectric–first process exhibited better gate controllability than that fabricated by gate–last process, and this improvement is thought to be due to the precise protection of the nanowire channel surface by proposed fabrication process. These transistors also exhibited superior electrical properties, such as drain current, maximum transconductance ($g_{m,\ max}/w_G$), and ON–OFF ratio ($I_{ON/OFF}$) of 38 mA/mm, 21 mS/mm, 10^4, respectively.

8.1 Introduction

Epitaxially grown semiconductor nanowires (NWs) have attracted much attention for their unique electrical and optical properties for future device applications, such as in field–effect transistors (FETs), laser diodes, solar cells, and so on [1]–[9]. Among them, free–standing vertical surrounding–gate (VSG) FETs has intensively been demonstrated [10]–[20], because of their excellent gate controllability and effective suppression of short channel effects. To date, catalyst–assisted vapor–liquid–solid (VLS) growth method have frequently been used for growing NWs [21][22]. In this method, however, the precise position–control of NWs is relatively difficult and it is concerned that incorporation of catalyst into NWs can deteriorate the crystalline quality [23]. We have already reported on an alternative method, that is, catalyst–free selective–area metal–organic vapor–phase epitaxy (SA–MOVPE) for forming NWs [24]–[29]. This method is capable of growing NWs at adequately predetermined positions without any assistance of catalysts. We have already demonstrated the characterization of NW–VSGFETs using selectively–grown InAs NWs on Si substrate and it has been exhibited good electrical properties [15]. However, the fabrication process and structure of VSGFETs are relatively complicated, and it is not easy to characterize electrical properties of single NW, such as resistivity and capacitance [11][30]–[32]. In this sense, lateral NW–FETs [33]–[53], which are easier to fabricate, are more adequate for electrical measurements of single NWs to study and to demonstrate their intrinsic performance.

So far, we have already reported the electrical properties of lateral InGaAs–NW–channel schottky–gate metal–semiconductor (MES) FETs [33]. InGaAs has superior properties as a channel material of transistors, because it has high electron mobility and good interface properties [54]–[59]. However, sufficiently good output characteristic and InGaAs NW–channel lateral metal–insulator–semiconductor (MIS) FETs has not been demonstrated. In this study, we fabricated lateral InGaAs NW–MISFETs by using gate–last and gate–dielectric–first process. As a result, these MISFETs exhibited good output characteristics. In particular, gate–dielectric–first process showed better turn–off behavior of MISFETs as compared to gate–last process, due to the protection of MIS interface from the process–induced damages.

8.2 Experimental Details

8.2.1 Selective–Area Growth of InGaAs Nanowires

Unintentionally–doped InGaAs NWs were grown by following procedure. First, after the deposition of a 20nm–thick SiO_2 film on an InP (111)B substrate by RF sputtering, an array of holes with diameter, d_0, of 100 nm, and mask pitch, a, of 1 μm was defined on SiO_2–masked substrate by electron–beam lithography (EBL) and wet chemical etching. Then, InGaAs NWs were formed by the low–pressure horizontal–MOVPE system, supplying trimethylgallium (TMGa), trimethylindium (TMIn), and 5% arsine (AsH_3) diluted in H_2 as source materials. The partial pressures of TMGa, [TMGa], and TMIn, [TMIn] were 5.68×10^{-7} atm and 9.15×10^{-7} atm [60], respectively, giving a [TMGa] to [TMIn] ratio of 38 : 62. The partial pressure of AsH_3, [AsH_3] was 6.0×10^{-4} atm, and giving a V/III ratio of 270. The growth temperature was 650 °C. The growth time was 70 min. Free–standing NWs with hexagonal cross sections (six NW side facets are {–110}) were selectively formed in the circular opening holes of the mask. A scanning electron microscopy (SEM) image of InGaAs NWs is shown in **Figure 8–1**. The length of each NW, h, was 8 μm. The NW diameter, d, was larger than d_0 and was 200 nm. This is due to radial growth, which becomes prominent above a critical growth time or height [24]; d can be reduced to close to d_0 when an appropriate growth time is used.

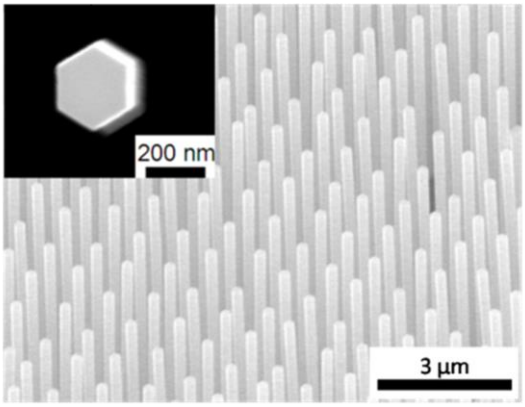

Figure 8–1

45°–tilted SEM image of unintentionally–doped InGaAs nanowires (d_0 = 100 nm, a = 1 μm). The inset shows an enlarged view of the top of a nanowire.

8.2.2 Estimation of Alloy Composition of InGaAs Nanowires

Micro–photoluminescence (μ–PL) measurements were carried out at 4.2 K. Excitation light from $TiAl_2O_3$ laser operating at 773 nm was focused on NW arrays by ×20 microscope objectives with a numerical aperture of 0.40, which was also used to collect the PL from the NWs. **Figure 8–2** shows PL spectra of InGaAs NWs. The peak energy of photoluminescence from InGaAs NWs is around 0.7 eV. From this result, we estimated the alloy composition of InGaAs NWs [24]–[26], by using following equation, *E*g [61],

$$E_g(x,T) \cong 0.42 + 0.625x - \left(\frac{5.8}{T+300} - \frac{4.19}{T+271}\right) \cdot 10^{-4} T^2 x - 4.19 \cdot 10^{-4} \cdot \frac{T^2}{T+271} + 0.475x^2$$

where *E*g is the bandgap, *x* is gallium composition, and *T* (= 4.2 K) is measurement temperature. Estimated gallium (indium) composition was 0.35 (0.65), and this alloy composition is suitable for FET application [5][59]. In present estimation, we did not take into account the effect of lattice mismatch between the substrate and NWs, and corresponding strain effect in NWs. We think that their effect can be considered even less important because of the small footprint of NWs [62], and it does not qualitatively alter our main conclusion.

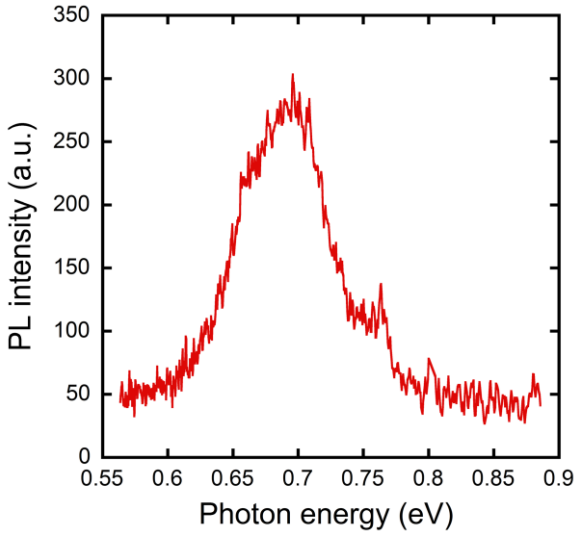

Figure 8–2

PL spectra of unintentionally–doped InGaAs nanowires (d_0 = 100 nm, a = 1 μm).

8.2.3 Gate–Last Process for MISFET Fabrication

Figure 8–3 shows schematic of gate–last process for fabrication of top–gate NW–MISFETs with single NWs. In this process, gate dielectric of Al_2O_3 was formed after the fabrication of ohmic contacts. Fabrication procedure is as follows. First, the NWs were removed from growth substrates and dispersed in ethanol by sonication, and then NWs transferred to a *p*+ Si substrate with 200 nm–thick SiO_2 overlayer. Next, after the area for ohmic contacts was defined by electron–beam lithography (EBL) and the native oxide on the area for ohmic contacts was removed by wet chemical etching in buffered HF, ohmic metals (i.e., Ti/Al/Ti/Au = 20/170/10/50 nm) for the source and drain contacts were formed by EB evaporation and lift–off technique. The length between source and drain was designed to be 3 μm. Subsequently, Al_2O_3 was formed by the atomic–layer–deposition (ALD) as a high–*k* gate dielectric. The thickness of Al_2O_3 was 10nm (Equivalent oxide thickness, EOT = 4 nm). Finally, the top–gate metals (Ti/Au = 30/230 nm) were formed by EBL, EB evaporation, and lift–off technique. The length of gate–electrode is 1 μm, and that between ohmic contacts and gate–electrode is 1 μm. No thermal treatment was performed before or after the gate formation for comparison between gate–last and gate–dielectric–first process. Electrical characteristics of InGaAs NW–MISFETs were measured by using parameter analyzer (Agilent_4156) at room temperature in the dark.

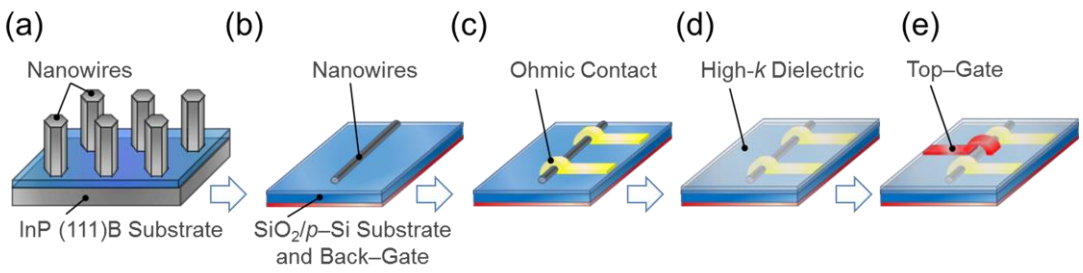

Figure 8–3

Schematics of process flow of gate–last process for fabrication of top–gate NW–MISFETs. (a) Nanowire growth. (b) Transfer of nanowires to SiO_2/Si substrate. (c) Fabrication of ohmic contacts. (d) Formation of high–*k* (Al_2O_3) dielectric. (e) Fabrication of top–gate electrode.

8.2.4 Gate–Dielectric–First Process for MISFET Fabrication

Figure 8–4 shows schematic of gate–dielectric–first process for fabrication of top–gate NW–MISFETs with single NWs. In this process, gate dielectric of Al_2O_3 was formed to cover all the periphery of NWs by depositing Al_2O_3 on free–standing NWs with precise removing the native oxide on NWs. Fabrication procedure is as follows. First, after a removal of the native oxide by wet chemical etching using alkali solution, whole surface and NWs were covered with Al_2O_3 formed by the ALD as a high–*k* gate dielectric. The thickness of Al_2O_3 was 10nm (EOT = 4 nm). Next, the NWs were removed from growth substrates and dispersed in ethanol by sonication, and then NWs transferred to a *p*+ Si substrate with 200 nm–thick SiO_2 overlayer. Area for ohmic contacts was defined by EBL, followed by the removal of the Al_2O_3 on NWs from defined area for ohmic contacts using wet chemical etching in buffered HF (i.e., BHF, NH_4F : HF = 5 : 1). Subsequently, ohmic metals (i.e., Ti/Al/Ti/Au = 20/170/10/50 nm) for the source and drain contacts were formed by EB evaporation and lift–off technique. The length between source and drain was designed to be 3 μm. Finally, the top–gate metals (Ti/Au = 30/230 nm) were formed by EBL, EB evaporation, and lift–off technique. The length of gate–electrode is 1 μm, and that between ohmic contacts and gate–electrode is 1 μm. No thermal treatment was performed before or after the gate formation for comparison between gate–last and gate–dielectric–first process. Electrical characteristics of InGaAs NW–MISFETs were measured by using parameter analyzer (Agilent_4156) at room temperature in the dark.

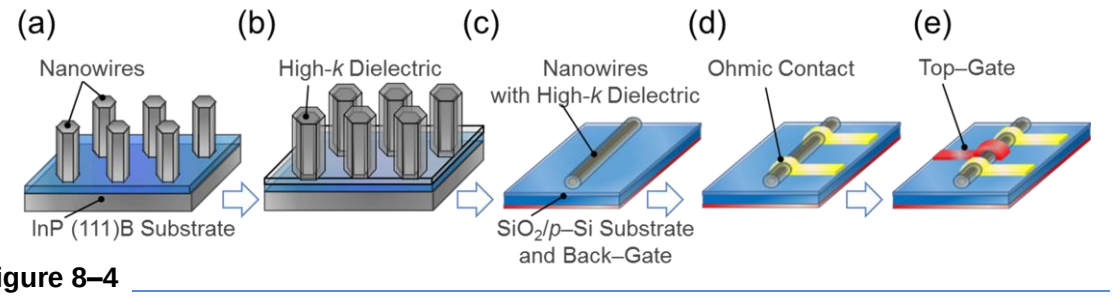

Figure 8–4

Schematics of process flow of gate–dielectric–first process for fabrication of top–gate NW–MISFETs. (a) Nanowire growth. (b) Formation of high–*k* (Al_2O_3) dielectric. (c) Transfer of nanowires to SiO_2/Si substrate. (d) Fabrication of ohmic contacts. (e) Fabrication of top–gate electrode.

8.3 Experimental Results

8.3.1 Structural Characterizations of InGaAs NW–MISFETs

Typical SEM images of typical top–gate InGaAs NW–MISFETs are shown **Figure 8–5(a)** and **Figure 8–5(b)**. Both NW–MISFETs were precisely fabricated as designed by EBL and lift–off technique. Here, it was found that the ohmic contacts (i.e., source and drain contacts) of NW–MISFETs fabricated by gate–last process were alloyed (see **Figure 8–5(a)**). On the other hand, NW–MISFETs fabricated by gate–dielectric–first process were not alloyed. This is probably because the difference in fabrication process. Namely, because the fabrication of the ohmic contacts is carried out before the deposition of Al_2O_3 by ALD at 300 °C (30 min) in the gate–last process, ohmic metals were automatically annealed by high temperature during the ALD process in this process. Meanwhile, in the gate–dielectric–first process, the ohmic contacts were fabricated after the ALD process, and ohmic contacts were not annealed. This difference in the process flow affects the electrical characteristics of NW–MISFETs, and we discuss this issue in a next section.

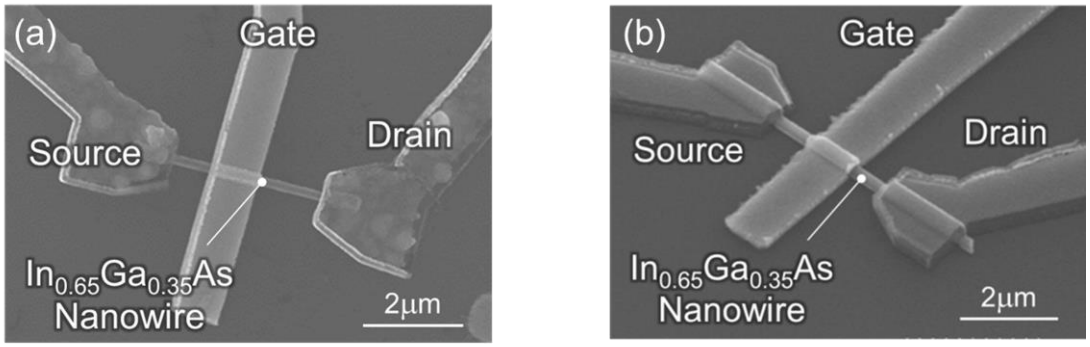

Figure 8–5

SEM images of top–gate InGaAs NW–MISFETs. (a) MISFETs fabricated by gate–last process. (b) MISFETs fabricated by gate–dielectric–first process.

8.3.2 Electrical Characterizations of InGaAs NW–MISFETs

8.3.2.1 Gate–Last process

Figure 8–6 shows output characteristics of a top–gate InGaAs NW–MISFET fabricated by gate–last process. It was found that the NW–MISFETs were *n*–type depression mode as similar to previously reported *n*–InGaAs NW–MESFETs and InAs VSGFETs [15][33]. In addition, maximum drain current per gate width ($I_{DS,max}/w_G$) were 87 mA/mm, at voltage between the gate and source electrodes, V_{GS} = 0 V, and voltage between the gate and source electrodes, V_{DS} = 1 V, where w_G is $\pi \cdot d_{NW}$ (d_{NW} : diameter of NWs). This value of maximum drain current is much larger than those of aforementioned previously reports. This result is promising for FETs if one considers that the present NWs are unintentionally–doped ones. Furthermore, the gate leakage current of NW–MISFETs were the level of pA. This is also better and much lower than that for *n*–InGaAs NW–MESFETs, and this is due to the adoption of MIS structure. However, the NW–MISFETs did not turn off completely, and the other NW–MISFETs fabricated by gate–last process were exhibited similar characteristics. This is probably because the process–induced damages, that is, the damages in transfer process (see **Figure 8–3(b)**) when none–coated NWs directly transferred to the *p*+ Si substrate. In addition, the native oxide on the channel area of NWs was not precisely removed, because the wet chemical etching for removal of native oxide by BHF simultaneously etches the ohmic contacts. We think that those process–induced damages caused the increase of interface state density, and this inhibited the gate electric–field control [56].

8.3.2.2 Gate–Dielectric–First process

Next, we measured the electrical properties of top–gate NW–MISFETs fabricated by gate–dielectric–first process. Results are shown in **Figure 8–7**. We found that the NW–MISFETs were *n*–type depression mode as similar to those fabricated by gate–last process. The threshold voltage is –2.3 V at V_{DS} = 1 V. In contrast to NW–MISFETs fabricated by gate–last process, that for gate–dielectric–first process exhibited good saturation characteristics, turn–off behavior. We think this improvement in saturation and turn–off behavior is due to the improvement of the property of dielectric–NW interface. That is, by depositing Al_2O_3 just after

the chemically treated NW surfaces, interfacial disorders or impurities which lead to the interface states was reduced. The maximum transconductance per gate width ($g_{m,max}/w_G$) was 21 mS/mm at V_{DS} = 1V. Furthermore, $I_{DS,max}/w_G$ was 38 mA/mm, at V_{GS} = 0 V, and V_{DS} = 1 V, and ON–OFF ratio ($I_{ON/OFF}$) was 10^4. These values of $I_{DS,max}/w_G$ and $I_{ON/OFF}$ are larger than those obtained in previously reported *n*–InGaAs NW–MESFETs [33]. These are probably because the precise surface treatment of NWs and adoption of MIS structure.

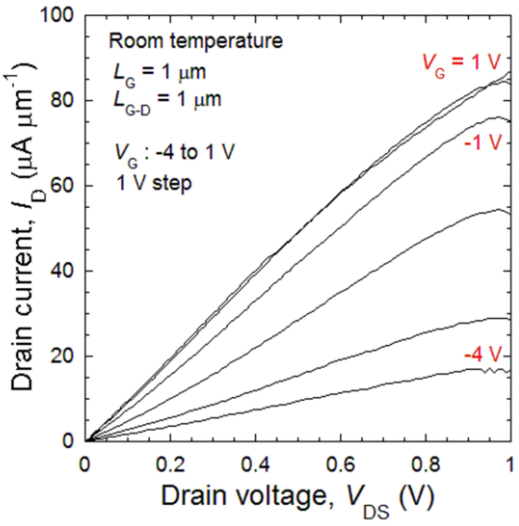

Figure 8–6

Output characteristic of NW–MISFET fabricated by gate–last process.

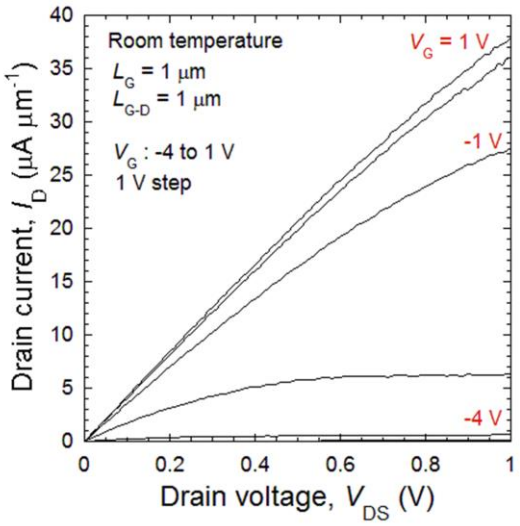

Figure 8–7

Output characteristic of NW–MISFET fabricated by gate–dielectric–first process.

8.4 Discussions

For unintentionally–doped InGaAs NW–MISFETs fabricated by gate–last process, maximum drain current per gate width ($I_{DS,max}/w_G$) was 87 mA/mm, and it was comparable value to that of InAs VSGFETs with gate length of 300 nm [15]. This is thought to be due to the reduction of contact resistance between ohmic metals and NWs, because the NWs were directly contacted to the ohmic metals and the contact area of ohmic metals were relatively large. This result is promising for FET applications. However, these NW–MISFETs did not turn off completely, probably because of process–induced damages.

On the other hand, for unintentionally–doped InGaAs NW–MISFETs fabricated by gate–dielectric–first process, we obtained good electrical properties, such as saturation characteristics and turn–off behavior, because of precise treatment of NW surface. However, their $I_{DS,max}/w_G$ is 38 mA/mm, and it is smaller than that for gate–last process (i.e., $I_{DS,max}/w_G$ = 87 mA/mm). This is probably because the unintentionally annealing of ohmic metals in the case of gate–last process, as we mentioned in **Section 8.3.1.** In other words, $I_{DS,max}/w_G$ for gate–dielectric–first process can also be improved to the comparable value to that for gate–last process by additional annealing process for alloying of ohmic metals. Next, we discuss their subthreshold property. The subthreshold swing of NW–MISFETs for gate–dielectric–first process was estimated by their output characteristic (see **Figure 8–7**), and it was 1 V/dec. This value is much larger than that of previously reported *n*–InGaAs NW–MESFETs and InAs VSGFETs [15][33]. One of the reasons why MISFETs exhibited large subthreshold swing is large diameter of NWs, and it causes the increase of depletion layer capacitance [63]. Here, the subthreshold swing can be approximated by following equation,

$$S = \frac{kT}{q} \cdot ln10\left(1 + \frac{C_d}{C_{OX}}\right)$$

where S is subthreshold swing, k is boltzmann coefficient, T is absolute temperature, q is elementary charge, C_d is depletion layer capacitance, and C_{OX} is gate–oxide (dielectric) capacitance. Consequently, when depletion layer capacitance is increased by increasing NW

diameter, subthreshold swing becomes larger. To reduce the subthreshold swing, reduction of NW diameter is important. Subsequently, we estimated field–effect mobility of top–gate InGaAs NW–MISFETs fabricated by gate–dielectric–last process. The field–effect mobility is given by following equation,

$$\mu_{\mathrm{FE}} = \frac{g_m \cdot L_G \cdot \ln(1 + 2t_{ox}/d_{NW})}{2\pi \cdot \varepsilon_0 \cdot \varepsilon_{high\text{-}k} \cdot V_{DS}}$$

where μ_{FE} is field–effect mobility, L_{G} is the width of gate electrode, g_{m} is transconductance, t_{ox} is the thickness of high–*k* dielectric, ε_0 is dielectric constant of vacuum, $\varepsilon_{high\text{–}k}$ is dielectric constant of high–*k* dielectric, and V_{DS} is the supplied voltage between the drain and source electrode. Estimated field–effect mobility, μ_{FE}, is 24 $\mathrm{cm^2/V{\cdot}s}$, and this value is much smaller than that for bulk InGaAs [55][64]. One of the reasons why μ_{FE} was low is less transconductance of MISFETs, and this is probably because of large contact resistance, where it is due to the no–alloyed ohmic contacts. The other reason is the inhibition of carrier transport by interface states. This is thought to be improved by post–deposition–annealing (PDA).

Although we still need further optimization of the NW diameter and the processing for devices, present lateral MISFETs are very promising. In particular, those fabricated by gate–dielectric–first process will be useful to investigate and optimize interfacial properties between NW and dielectrics, because it is possible to systematically perform surface treatment for a bunch of NWs.

8.5 Summary

We report on electrical characterization of lateral MISFETs using single InGaAs NWs fabricated by gate–last and gate–dielectric–first process. The NW–MISFETs fabricated by gate–last process exhibited $I_{DS,max}/w_G$ = 87 mA/mm, and this value is promising for FET applications. However, these NW–MISFETs could not turn–off completely. This is probably because of process–induced damages at the surface of NWs. For improving turn–off characteristics, we attempted alternative fabrication process (i.e., gate–dielectric–first process). The transistors fabricated by gate–dielectric–first process exhibited better gate controllability and turn–off behavior than that fabricated by gate–last process, and this improvement is thought to be due to the precise protection of the NW surface and removal of native oxide. These transistors also exhibited superior electrical properties, such as $I_{DS,max}/w_G$ = 38 mA/mm, $g_{m,\,max}/w_G$ = 21 mS/mm, and $I_{ON/OFF} = 10^4$. Although we still need further optimization of the NW size and the processing for devices, present lateral MISFETs are very promising. In particular, those fabricated by gate–dielectric–first process will be useful to investigate and optimize interfacial properties between NW and dielectrics, because it is possible to systematically perform surface treatment for a bunch of NWs.

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Chapter 9

Summary and Conclusions

9.1 Summary

The purpose of this work is to understand and control the growth of $In_{1-x}Ga_xAs$ nanowires having any alloy composition ($0<x<1$), and to achieve the high–performance device applications using InGaAs nanowires formed by selective–area metal–organic vapor–phase epitaxy (SA–MOVPE). Summary and conclusions of the present work are the following:

In **Chapter 5**, we investigated the growth of InGaAs nanowires under an indium–rich supply condition by SA–MOVPE, and highly uniform and non–tapered nanowires were thereby formed. By comparison with previous reports on InAs, gallium–rich InGaAs, and GaAs nanowires, it was found that the axial growth rate of InGaAs nanowires becomes maximum at a certain temperature, which decreases as group–III supply ratio increases. The knowledge on the composition–dependent effects of growth temperature on the growth of InGaAs nanowires offers important guidelines for precisely controlling the size and alloy composition of InGaAs nanowires.

Furthermore, it is expected that the optimum growth temperature range for InGaAs nanowires lies slightly above a certain growth temperature, where reasonable axial growth rate is guaranteed and lateral growth is negligible. To confirm this expectation, more systematic study on, for instance, dependences on V/III ratio, mask opening size, and opening pitch are required. In addition, temperature also affects the alloy composition of NWs; thus, more accurate assessment of growth condition is required to obtain InGaAs with desired composition.

In **Chapter 6**, we described about composition–dependent effects of V/III ratio for selectively–grown $In_{1-x}Ga_xAs$ nanowires, and discussed the experimental results in detail. Gallium–rich ($x > 0.5$) and indium–rich ($x < 0.5$) InGaAs nanowires were grown by SA–MOVPE, and the effect of the V/III ratio on these nanowires was investigated. It was found that the diameter, height, and the alloy composition of nanowires were strongly affected by the V/III ratio, particularly in gallium–rich nanowire growth. This is thought to originate from the effect of the arsenic–terminated (111)B nanowire top facet on the incorporation of gallium and indium, as well as the adsorption/desorption of growth species. Furthermore, these growth behaviors are different from those of indium–rich growth. It was suggested that the growth dynamics depends on group–III supply ratio. Understanding such composition–dependent growth dynamics will provide important guidelines for achieving future nanowire–based electronics and understanding the growth mechanism of other mixed crystal semiconductor nanowires.

In **Chapter 7**, we described about the proposed growth method for realizing quite thin InGaAs NWs independently of the geometry of the mask used for SA–MOVPE. Control of the diameter and pitch of InGaAs nanowire arrays was investigated. It was found that their nucleation was strongly dependent on the geometry of the mask, resulting in the difficulty of nucleation for a larger mask pitch, particularly for an opening diameter of less than 50 nm.

Precise adjustment of the V/III ratio enabled us to control the nucleation independently of the mask pitch for smaller openings, and we successfully obtained 30–nm–diameter InGaAs nanowires independently of the mask pitch by the proposing V/III–ratio–controlled two–step growth method. These results are expected to contribute to realizing much finer and various high–quality axial heterostructure NWs independently of their location.

In **Chapter 8**, we described about the electrical characterization of lateral single InGaAs nanowire–MISFETs fabricated by gate–last and gate–dielectric–first process. The NW–MISFETs fabricated by gate–last process exhibited $I_{DS,max}/w_G$ = 87 mA/mm, and this value is promising for FET applications. However, these nanowire–MISFETs could not turn off completely. This is because of process–induced damages at the surface of nanowires.

For improving turn off characteristics, we attempted alternative fabrication process, that is, gate–dielectric–first process. The transistors fabricated by gate–dielectric–first process exhibited good turn–off behavior compared with that fabricated by gate–last process, and this improvement is thought to be due to the precise protection of the nanowire surface and removal of native oxide. These transistors also exhibited superior electrical properties, such as $I_{\mathrm{DS,max}}/w_G$ = 38 mA/mm, $g_{\mathrm{m,\ max}}/w_G$ = 21 mS/mm, and $I_{\mathrm{ON/OFF}}$ = 10^4. Although we still need further optimization of the NW size and the processing for devices, present lateral MISFETs are very promising. In particular, those fabricated by gate–dielectric–first process will be useful to investigate and optimize interfacial properties between nanowire and dielectrics, because it is possible to systematically perform surface treatment for a bunch of nanowires.

9.2 Outlook for Nanowire Fabrication and Application

This work clarified an origin of composition–dependent growth dynamics of selectively–grown InGaAs nanowires, and explored the device application using nanowires.

Research on the synthesis of semiconductor nanowires has been begun from over half a century ago, and has become intensive since a quarter–century ago. First demonstration of the synthesis of Si nanowires via catalyst–assisted vapor–liquid–solid technique was reported in 1964 by Wagner and Ellis. This early works on nanowires were popularized as promising materials for emerging future device applications in the following decade, and became one of the most active research fields within the nanotechnology and material science community. This can be seen from the vast number of papers published on nanowires over the past two decades, which has increased exponentially. The research on synthesis of III–V compound semiconductor nanowires and their applications have become an interest topic since 2000, and the importance of ternary alloy nanowires, (e.g., InGaAs nanowires discussed in this thesis) and their application is now growing continuously. In this situation, further detailed discussions on their growth dynamics and demonstration of novel device applications are really required for achieving future nanowire–based electronics and photonics. We are hoping the continuous progress of the research on the nanowire synthesis and applications in the future.

List of Publications/Presentations

1. Publications Related to This Work

[1] Y. Kohashi, T. Sato, K. Ikejiri, K. Tomioka, S. Hara, and J. Motohisa, "Influence of Growth Temperature on Growth of InGaAs Nanowires in Selective–Area Metal–Organic Vapor Phase Epitaxy", *Journal of Crystal Growth*, Vol. **338** (2012) pp. 47–51.

[2] Y. Kohashi, S. Sakita, S. Hara, and J. Motohisa, "Pitch–Independent Realization of 30–nm–Diameter InGaAs Nanowire Arrays by Two–Step Growth Method in Selective–Area Metalorganic Vapor–Phase Epitaxy", *Applied Physics Express*, Vol. **6** (2013) No. 2, Article No.: 025502.

[3] Y. Kohashi, S. Hara, and J. Motohisa, "Composition–Dependent Growth Dynamics of Selectively Grown InGaAs Nanowires", *Materials Research Express* (2013) Accepted.

2. Publications Related to Other Work

[1] Y. Kobayashi, Y. Kohashi, S. Hara, and J. Motohisa, "Selective–Area Growth of InAs Nanowires with Metal/Dielectric Composite Mask and Their Application to Vertical Surrounding–Gate Field–Effect Transistors", *Applied Physics Express*, Vol. 6 (2013), No. 4, Article No.: 045001.

3. Presentations Related to This Work

International Conferences

[1] Y. Kohashi, T. Sato, K. Tomioka, S. Hara, T. Fukui, J. Motohisa, "Electrical Characterization of InGaAs Nanowire MISFETs Fabricated by Dielectric–First Process", 2010 International Conference on Solid State Devices and Materials (SSDM 2010), Tokyo, Japan, September, 2010. [Oral]

[2] Y. Kohashi, T. Sato, K. Tomioka, S. Hara, T. Fukui, J. Motohisa, "Electrical Characterization of InGaAs Nanowire MISFETs Fabricated by Dielectric–First Process",29th Electronic Materials Symposium, shizuoka, Japan, July, 2010. [Poster]

[3] Y. Kohashi, T. Sato, S. Hara, T. Fukui, J. Motohisa,"Composition–Dependent Growth

Dynamics of InGaAs Nanowires in Selective–Area MOVPE", 38th International Symposium on Compound Semiconductors (ISCS 2011), Berlin, Germany, May, 2011. [Oral]

[4] Y. Kohashi, S. Hara, J. Motohisa,"Study on the Growth of In–rich InGaAs Nanowires by Selective–Area Metal–Organic Vapor Phase Epitaxy", 2011 International Conference on Solid State Devices and Materials (SSDM 2011), Aichi, Japan, September, 2011. [Oral]

[5] Y. Kohashi, S. Hara, J. Motohisa, "Effect of Growth Temperature on the Growth of InGaAs Nanowires in Selective–Area MOVPE", International Symposium on Advanced Nanodevices and Nanotechnology (ISANN 2011), Hawaii, USA, December, 2011. [Poster]

[6] Y. Kohashi, Y. Kobayashi, M. Yatago, S. Hara, J. Motohisa, "Fabrication of Highly Uniform InGaAs Nanowires in 30nm–Diameter Openings with Lower Density in Selective–Area Metalorganic Vapor Phase Epitaxy", 31st Electronic Materials Symposium (EMS 31), Shizuoka, Japan, July, 2012. [Poster]

[7] Y. Kohashi, S. Sakita, S. Hara, J. Motohisa, "Control of Diameter and Pitch of InGaAs Nanowire Arrays in Selective–area Metalorganic Vapor Phase Epitaxy", 2012 International Conference on Solid State Devices and Materials (SSDM 2012), Kyoto, Japan, September, 2012. [Oral]

[8] Y. Kohashi, S. Sakita, S. Hara, J. Motohisa, "Selective–Area Growth of Highly Uniform and Thin InGaAs Nanowires by Two–Step Growth Method", 2012 Materials research society Fall Meeting (2012 MRS Fall Meeting), Boston, USA, November, 2012. [Poster]

[9] Y. Kohashi, S. Hara, J. Motohisa, "Influence of V/III Ratio on the Growth of InGaAs Nanowires in Selective–Area MOVPE", 40th International Symposium on Compound Semiconductors (ISCS 2013), Kobe, Japan, May, 2013. [Oral]

[10] Y. Kohashi, S. Hara, J. Motohisa, "Composition–Dependent Growth Dynamics of InGaAs Nanowires in Selective–Area Metal–Organic Vapor–Phase Epitaxy", International Symposium on Advanced Nanodevices and Nanotechnology (ISANN 2013), Hawaii, USA, December, 2013. [Oral]

Domestic Conferences

[1] **小橋 義典**, 佐藤 拓也, 冨岡 克広, 原 真二郎, 福井 孝志, 本久 順一, "誘電体ファ–ストプロセスによる InGaAs ナノワイヤMISFETの作製と評価", 秋季第71回応用物理学関連連合講演会, 長崎大学, 2010年9月

[2] **小橋 義典**, 佐藤 拓也, 原 真二郎, 福井 孝志, 本久 順一, “MOVPE 選択成長法による高 In 供給下における InGaAs ナノワイヤ形成と成長メカニズムの変化”, 春季第58回応用物理学関係連合講演会, 神奈川工科大学, 2011年3月

[3] **小橋 義典**, 佐藤 拓也, 池尻 圭太郎, 冨岡 克広, 原 真二郎, 本久 順一, “MOVPE 選択成長法によるInGaAs ナノワイヤ成長におけるIII族供給比に依存した成長温度依存性の変化”, 秋季第72回応用物理学関係連合講演会, 山形大学, 2011年8月

[4] **小橋 義典**, 崎田 晋哉, 原 真二郎, 本久 順一, “2 段階 MOVPE 選択成長による極微細・位置制御 InGaAs ナノワイヤの形成”, 秋季第73回応用物理学関連連合講演会, 松山大学, 2012年9月

[5] **小橋 義典**, 原 真二郎, 本久 順一, “InGaAs ナノワイヤの選択成長におけるV/III比の影響”, 第60回応用物理学会春季学術講演会, 神奈川工科大学, 2013年3月

4. Presentations Related to Other Work

International Conferences

[1] Y. Kobayashi, Y. Kohashi, S. Hara, and J. Motohisa, “Fabrication and Characterization of InAs Nanowire Vertical Surrounding–gate FETs”, 24th International Microprocesses and Nanotechnology Conference (MNC 2011), Kyoto, Japan, October, 2011. [Oral]

[2] Y. Kobayashi, Y. Kohashi, S. Hara, and J. Motohisa, “Fabrication and Characterization of InAs Nanowire Vertical Surrounding–Gate FETs”, International Workshop on Quantum Nanostructures and Nanoelectronics (QNN 2011), Tokyo, Japan, October, 2011. [Poster]

[3] Y. Kobayashi, Y. Kohashi, S. Hara, and J. Motohisa, “Fabrication and Characterization of InAs Nanowire Vertical Surrounding–gate FETs”, International Symposium on Advanced Nanodevices and Nanotechnology (ISANN 2011), Hawaii, USA, December, 2011. [Poster]

[4] J. Motohisa, S. Maeda, Y. Kohashi ,“Far–Field Emission Patterns in InP Nanowire LEDs”, 31st International Conference on the Physics of Semiconductors (ICPS 2012), Zurich, Switzerland, July, 2012. [Poster]

[5] S. Yanase, Y. Kohashi, K. Ikejiri, S. Hara, J. Motohisa, “Selective growth and characterization of InP Nanowires by Metal Organic Vapor–Phase Epitaxy”, 31st Electronic Materials Symposium (EMS 31), Shizuoka, Japan, July, 2012. [Poster]

[6] T. Wada, Y. Kohashi, S. Hara, J. Motohisa, “Study on the lateral growth on GaAs Nanowires”, 32nd Electronic Materials Symposium (EMS 32), Shiga, Japan, July, 2013. [Poster]

[7] S. Yanase, Y. Kohashi, S. Hara, J. Motohisa, “A New Growth Mode of InP Nanowires in Selective–Area Metal–Organic Vapor–Phase Epitaxy”, International Symposium on Advanced Nanodevices and Nanotechnology (ISANN 2013), Hawaii, USA, December, 2013. [Poster]

Domestic Conferences

[1] 小林 悠太, **小橋 義典**, 原 真二郎, 本久 順一, “縦型 InAs ナノワイヤ FET の作製と評価”, 秋季第72回応用物理学関係連合講演会, 山形大学, 2011年8月

[2] 柳瀬 祥吾, **小橋 義典**, 池尻 圭太郎, 原 真二郎, 本久 順一, “(111)A 面上への SA–MOVPE 成長における InP ナノワイヤの 3 方向成長モ–ド”, 秋季第 73 回応用物理学関連連合講演会, 松山大学, 2012 年 9 月

[3] 和田 年弘, **小橋 義典**, 原 真二郎, 本久 順一, “横方向成長させたGaAsナノワイヤの評価”, 第 74 回応用物理学会秋季学術講演会, 同志社大学, 2013 年 9 月

5. Awards

[1] **小橋 義典**, 原 真二郎, 本久 順一, “InGaAs ナノワイヤの選択成長におけるV/III比の影響”, ポスターアワード, 第60回応用物理学会春季学術講演会, 神奈川工科大学, 2013年3月