A Three-Valued D-Flip-Flop and Shift Register Using Multiple-Junction Surface Tunnel Transistors

Tetsuya Uemura and Toshio Baba

***Abstract*—A three-valued D-flip-flop (D-FF) circuit and a two-stage shift register built from InGaAs-based multiple-junction surface tunnel transistors (MJSTT) and Si-based metal-oxide-semiconductor field effect transistors (MOSFET) have been demonstrated. Due to the combination of the MJSTTs latching function and the MOSFETs switching function, the number of devices required for the D-FF circuit was greatly reduced to three from the thirty required for the FET-only circuit.**

***Index Terms*—D-FF, multiple-valued logic, NDR, shift register, tunnel transistor.**

I. Introduction

MULTIPLE-VALUED logic (MVL) has a strong potential as a means to overcome the problems associated with the complexity of wiring and the amount of power dissipation in ULSI systems. The success of the MVL approach, however, depends heavily on the availability of devices that are suitable for MVL operation. Especially devices in which the operation of a multiple level quantization and a switching between them can easily be obtained are desired.

The negative differential resistance (NDR) device shows promise for use in MVL circuits, since multiple threshold values can easily be obtained by connecting such devices in series. Many MVL circuits using the resonant tunneling diode (RTD), which is the most mature NDR device, or resonant tunneling transistors including the combination of RTD and FET have been reported [1]–[3].

We have recently developed a novel tunneling transistor that we call the multiple-junction surface tunnel transistor (MJSTT) [4]. The MJSTT has several n^+/p^+ interband tunneling junctions connected in series between source and drain, and produces a gate-controlled multiple NDR characteristic. We have demonstrated several MVL circuits, in which the unique characteristics of this transistor are used, including a three-valued memory cell [4], a three-valued inverter [5], a literal gate [6], and a T-gate [7].

In this paper, we demonstrate a novel three-valued D-flip-flop (D-FF) circuit and a two-stage shift register, both of which are very important units in sequential logic circuits, using a combination of the MJSTT and the Si metal-oxide-semiconductor field effect transistor (MOSFET). Due to the multiple NDR characteristics of the MJSTT, the number of devices as well as of interconnections can be greatly reduced as compared to equivalent FET-only circuits.

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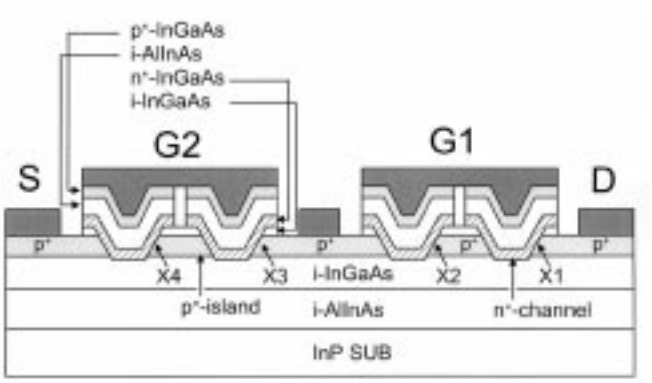

Fig. 1. Device structure of the InGaAs/AlInAs-based MJSTT.

II. Device Structure

Fig. 1 shows the structure of an MJSTT fabricated by InGaAs/AlInAs material system, lattice matched to an InP substrate. The fabrication process is as follows. First layer structures consisting of a 500-nm i-$Al_{0.48}In_{0.52}As$ buffer, a 50-nm i-$In_{0.53}Ga_{0.47}As$ subchannel, a 80-nm p^+-$In_{0.53}Ga_{0.47}As$ $(Be = 8 \times 10^{19}\ cm^{-3})$ source-island-drain layer, and a 30-nm i-$In_{0.53}Ga_{0.47}As$ blocking layer were grown on a (100) InP substrate by molecular beam epitaxy (MBE) at 460°C. The source, p^+-island and drain regions were formed by wet chemical etching using a SiN_x/SiO_2 mask. After removal of the surface oxides from the substrate by hydrogen radical cleaning at 420°C, a 15-nm n^+-$In_{0.53}Ga_{0.47}As$ $(Si = 6 \times 10^{18}\ cm^{-3})$ channel, a 50-nm i-$Al_{0.48}In_{0.52}As$ insulator layer, and a 30-nm p^+-$In_{0.53}Ga_{0.47}As$ $(Be = 7 \times 10^{19}\ cm^{-3})$ gate layer were grown. Each gate was formed by wet chemical etching with the cutting the channel layer at the top of the blocking layer to eliminate the direct current path between the source and the drain. AuZn/Ni alloy contacts were used for the source, p^+-island and drain electrodes, and Cr/Au nonalloy contacts were used for the gate electrode. The p^+-island length and channel length between p^+-regions were 10 and 4 μm, respectively. When three p^+ islands are embedded in the n^+ channel, eight interband tunneling junctions are formed between the source and the drain. When the drain voltage is applied, a half of the junctions were reverse biased, and the other half were forward

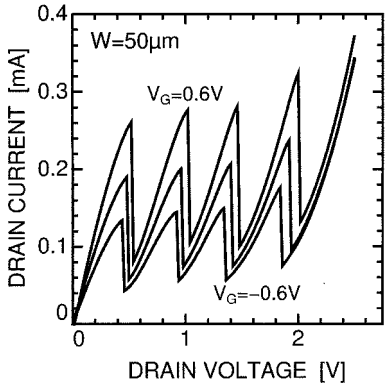

Fig. 2. Transistor characteristics of fabricated MJSTT.

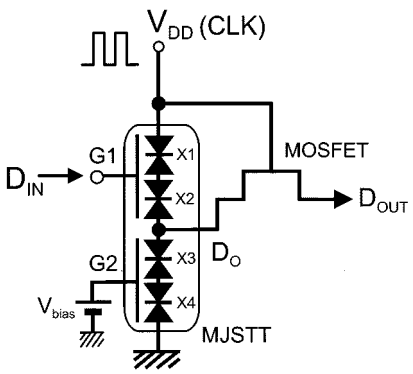

Fig. 3. Three-valued D-FF circuit.

biased. Since the resistances of the reverse biased tunneling junctions are much lower than those of the forward biased junctions, the MJSTT has four series-connected NDR device elements, with tunneling junctions labeled X1, X2, X3, and X4, respectively, in Fig. 1. The gate region was split into two parts at the middle p^+ island.

Fig. 2 is a plot of the room-temperature transistor characteristics of the fabricated MJSTT. The drain voltage was swept from 0.0 to 2.5 V, and a gate voltage was applied to both gate electrodes, G1 and G2, from 0.6 to -0.6 V, in steps of 0.6 V. Four-NDR characteristics arising from the four forward biased tunneling junctions, X1 to X4, can be seen clearly. The maximum gate leakage current at $V_G = 0.6$ V reaches as much as 0.5 μA.

III. Circuit Implementation

A. Three-Valued D-FF

A three-valued D-FF circuit consisting of the MJSTT and Si-MOSFET was demonstrated. Its circuitry is shown in Fig. 3. It is a very simple structure in which the source of the MOSFET is connected to the middle p^+ islands of the MJSTT. The clock signal is applied to both the drain terminal of the MJSTT and the gate terminal of the MOSFET. The input signal, $D_{\rm IN}$, is applied to the G1 terminal of the MJSTT.

The principle of the D-FF operation is based on monostable-multistable transition logic (MML) [2]. As described previously, four NDR device elements created by the junctions, X1 to X4,

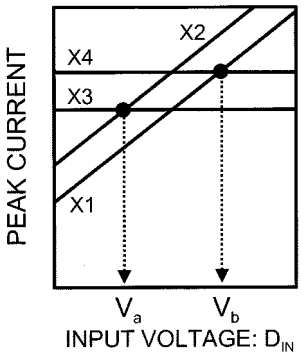

Fig. 4. Relationship of peak currents in four tunnel junctions.

were connected in series between the source and the drain of the MJSTT. The device structure is designed such that the peak current in each element versus input voltage $D_{\rm IN}$ satisfies the relation shown in Fig. 4. Since the peak currents depends on both the junction width and gate voltage, they were given by

$$\begin{aligned} I_P^{X1} &= (J_0 + g_m D_{\rm IN}) W_{X1} \\ I_P^{X2} &= (J_0 + g_m D_{\rm IN}) W_{X2} \\ I_P^{X3} &= (J_0 + g_m V_{\rm bias}) W_{X3} \\ I_P^{X4} &= (J_0 + g_m V_{\rm bias}) W_{X4} \end{aligned} \tag{1}$$

where I_P^{Xi} and W_{Xi} $(i = 1, 2, 3, 4)$ are peak current and width of junction Xi, $V_{\rm bias}$ is a bias voltage applied to the gate G2, J_0 is a peak current density per unit width at the gate voltage of 0 V, and g_m is a transconductance. From Fig. 2, the J_0 and g_m are about 4 μA/μm and 2 μS/μm, respectively. It should be noted that only X1 and X2 are modulated by the input voltage. In order to set the peak current of each tunnel junction, both junction widths and $V_{\rm bias}$ were controlled.

As the drain voltage is increased, the element with the lowest peak current switches to its high voltage state, followed by the element with the second lowest peak current, and so forth. When the drain voltage was swept from 0 V to the value at which two of the four junctions were switched from the low resistance on-state to the high resistance off-state, the voltage at the middle p^+ island, D_O has three possible final states according to the value of the input signal voltage. The relation is given by

$$D_O = \begin{cases} 2V_L & D_{\rm IN} < V_a \\ V_L + V_H & V_a < D_{\rm IN} < V_b \\ 2V_H & D_{\rm IN} > V_b \end{cases} \tag{2}$$

where V_a and V_b are threshold voltages determined by the intersection points indicated by the solid circles in Fig. 4, and V_L and V_H are the junction voltages in the on- and off-states, respectively.

Fig. 5 shows the voltage transfer characteristics of the MJSTT. The drain voltage was monotonically swept from 0 to 0.88 V, while the input voltage was varied from 0 to 0.9 V in 0.1 V steps. The voltage D_O was sampled at the drain voltage of 0.88 V. The three output states of 0.07, 0.42, and 0.80 V were obtained and correspond to the values given by (2).

Although the output signal of the MJSTT (D_O) is latched during the clock signal (or the drain voltage) is 0.88 V, it is reset to 0 V when the clock signal returns to 0. It is therefore difficult to transfer the output signal to the next stage. A pass

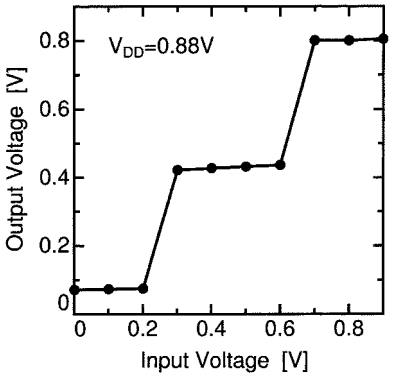

Fig. 5. Voltage transfer characteristics of MJSTT.

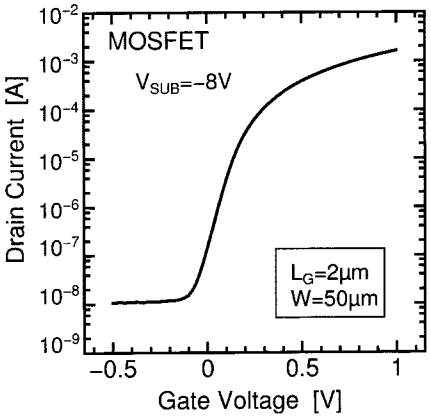

Fig. 6. Voltage transfer characteristics of Si-MOSFET.

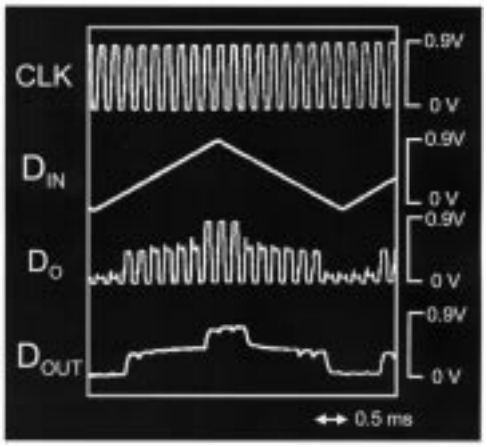

Fig. 7. Input output traces of three-valued D-FF circuit.

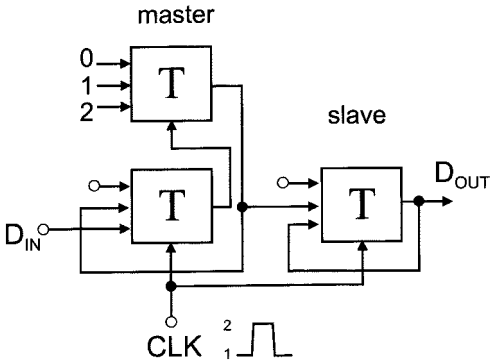

Fig. 8. Master–slave D-FF circuit consisting of three T-gates.

TABLE I
COMPARISON OF DEVICE COUNTS FOR THREE-VALUED D-FF CIRCUITS

	FET-*only* [7]	previous work [6]	this work
Number	30	6	2

transistor was used to avoid having to reset the output voltage. By applying the clock signal to the gate electrode of the pass transistor, D_O is transferred to the output terminal of the pass transistor during the clock high. When the clock is reset to 0, the output terminal voltage $D_{\rm OUT}$ is dynamically maintained, because the pass transistor simultaneously goes into its cutoff state. A similar circuit combining a pass transistor and an NDR device, such that ON and OFF of the pass transistor is controlled by the NDR device was demonstrated by Tang *et al.* [3].

A Si MOSFET instead of an InGaAs-based heterojunction FET (HJFET) was used as the pass transistor, because the gate-to-source voltage of the pass transistor must be larger than the voltage swing in D_O, that is, in this case, 0.8 V. A large gate leakage current flows in case for the HJFET when the gate-to-source voltage exceeds the built-in voltage of the Schottky gate. A large voltage swing can, on the other hand, be applied to a Si-MOS gate. Fig. 6 shows the voltage transfer characteristics of the MOSFET. The thickness of the gate oxide is 8 nm, and the gate length and width are 2 μm and 50 μm, respectively. The substrate was biased at -8 V to adjust the threshold voltage to almost 0 V. A good cut-off characteristic with a drain leakage current of about 0.1 μA was obtained at a gate voltage of 0 V.

A bread-board type three-valued D-FF circuit was constructed by using the MJSTT and MOSFET. The input–output traces for the D-FF circuit are shown in Fig. 7. A ramped voltage varying between 0 and 0.9 V was used as an input signal ($D_{\rm IN}$). The return-to-zero (RZ) type signal was obtained for the output voltage of the MJSTT (D_O), while non-return-to-zero (NRZ) type signal was obtained for the output voltage of the MOSFET ($D_{\rm OUT}$). The edge-triggered D-FF operation was successfully confirmed.

The same three-valued D-FF operation can be formed by a master–slave D-latch, which consists of three T-gates, as shown in Fig. 8 [8]. This circuit constructed with conventional FETs alone requires as many as 30 transistors, while the MJSTT-based circuit requires only three devices. We previously demonstrated another D-FF circuit with three-MJSTTs and three-FETs [7]. Table I summarize the comparison of the device counts for the D-FFs with different circuitry. The MJSTT has a great advantage in terms of reducing the number of devices required as well as the amount of interconnection in the circuit.

B. Three-Valued Shift Register

A multiple-valued shift register can be constructed from cascade-connected D-FFs. Fig. 9 shows circuitry for a two-stage shift register. As explained in Section III-A, the input voltage at

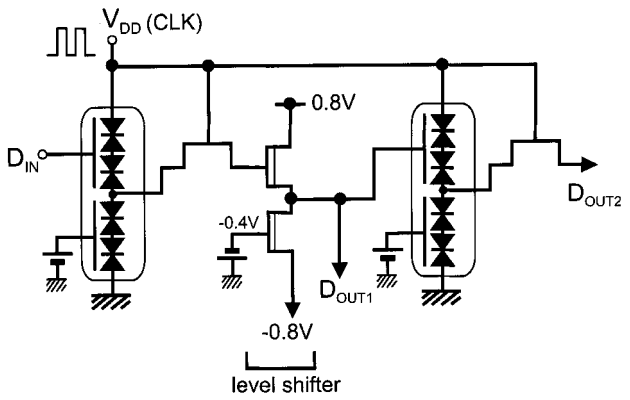

Fig. 9. Three-valued shift register.

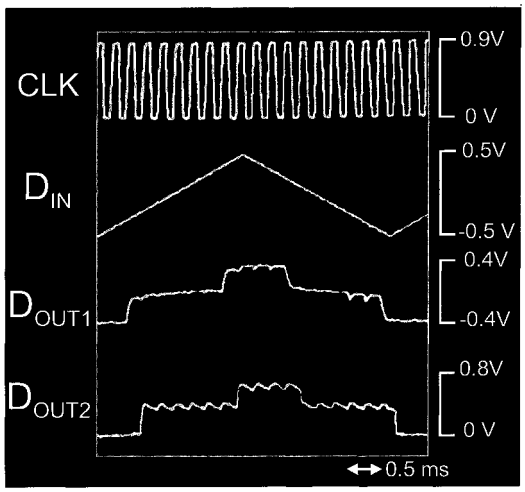

Fig. 10. Operation for three-valued shift register.

each stage needs to be maintained dynamically when the clock signal is 0. Voltages of more than 0.6 V, however, cannot be maintained due to the large gate leakage current of the next stage MJSTT. Therefore, a level shift circuit of the source-follower type, consisting of two depletion-type HJFETs, was inserted between the two D-FF circuits. This was used to shift the output level of the first-stage D-FF circuit by -0.4 V. As a result, the input gate voltage of the second MJSTT ranges from -0.4 to $+0.4$ V, and the gate leakage current can be suppressed over this range.

The operation of the shift register was shown in Fig. 10. A ramped voltage varying between -0.5 and 0.5 V was applied as the input signal to the first stage. The first D-FF works as a three-level quantizer and the second D-FF works as a shifter, where D_{OUT2} is obtained by shifting D_{OUT1} by one clock period.

C. Discussion

Although the D-FF and shift register circuits demonstrated in this study were constructed as a combination of InGaAs-MJSTT and Si-MOSFET, the same material system for the MJSTTs and FETs is desirable for a future large scale integrated circuit. As the number of MVL levels increases, the voltage swing increases. The InGaAs-based MJSTT and HJFET cannot deal with such large voltage swings due to their large gate leakage currents. The Si-based MOS system, on the other hand, can even deal with the large voltage swings required for more than four-valued system. Moreover, both the level shift circuit and negative voltage supply $(-0.8\ \mathrm{V})$ shown in Fig. 9 will not be needed in the Si-based system. The drawback of the Si system lies in the difficulty of forming an STT with a large current drive capability. The peak current density of the NDR characteristic for an Si-STT as reported recently was only about 1 A/cm^2, insufficient for high-speed operation [9]. In order to increase the tunneling current, the n^+/p^+ junction with high carrier concentration and abrupt doping profile is necessary. The conventional doping techniques, such as an ion implantation or diffusion, would be difficult to form such junctions. The crystal growth techniques, such as MBE or chemical vapor deposition (CVD), on the other hand, allows a formation of atomically controlled interface. In fact, the high peak current density of 4.7×10^4 A/cm^2, has recently been obtained from an MBE-grown Si Esaki tunnel diode, and this is a promising figure for high-speed operation [10]. Thus, Si-STTs with a large current drive capability will also be made possible by optimization of the device structure and/or fabrication method.

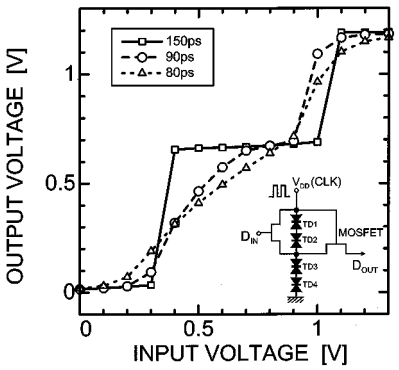

Fig. 11. Simulated input versus output characteristics of three-valued D-FF circuit for different clock rise time.

In order to estimate the operation speed, we made the SPICE simulation of the Si-based D-FF circuit shown in the inset of Fig. 11. For simplicity, the Si-STT was replaced by the combination of the MOSFET and Esaki tunnel diodes. The peak current density and junction capacitance value of the Si Esaki tunnel diode were assumed to be 1.26×10^4 A/cm^2 and 13.8 fF/μm^2, respectively [11]. As for the MOSFET, the 0.1 μm technology was assumed. One of the most critical parameter in this circuit on the speed performance is the rising time of the clock pulse. Fig. 11 indicates the simulated input versus output characteristics of the D-FF circuit for various rising time. When the rising time is more than 90 ps, clear three output levels were obtained. While it becomes less than 80 ps, no distinctive output levels appeared. The rising time of 90 ps corresponds to the clock frequency of 5.5 GHz. The normal operation is expected in this frequency regime. Here we assumed that the circuit operates normally if the output signal shows clear distinct three levels.

IV. Conclusion

A three-valued D-flip-flop (D-FF) circuit and a two-stage shift register using an InGaAs-based multiple junction surface

tunnel transistor (MJSTT) and Si-based metal-oxide-semiconductor field effect transistor (MOSFET) have been demonstrated. The number of devices required for the D-FF circuit can be greatly reduced to three from the thirty required for an FET-only circuit. The SPICE simulation suggests that Si-based three-valued D-FF and shift register can operate at more than 5-GHz clock frequency.

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REFERENCES

[1] S. Sen, F. Cappasso, A. Y. Cho, and D. Sivco, "Resonant tunneling device with multiple negative differential resistance: Digital and signal applications with reduced circuit complexity," *IEEE Trans. Electron Devices*, vol. ED-34, pp. 2185–2191, 1987.

[2] T. Waho, K. J. Chen, and M. Yamamoto, "Resonant tunneling diode and HEMT logic circuits with multiple threshold and multilevel output," *IEEE J. Solid-State Circuits*, vol. 33, pp. 268–274, 1998.

[3] H. Tang and H. C. Lin, "Multi-valued decoder based on resonant tunneling diodes in current tapping mode," in *Proc. 26th Int. Symp. Multiple-Valued Logic*, Santiago de Compostela, Spain, 1996, pp. 230–234.

[4] T. Baba and T. Uemura, "Multiple-junction surface tunnel transistors for multiple-valued logic circuits," in *Proc. 27th Int. Symp. Multiple-Valued Logic*, Nova Scotia, Canada, 1997, pp. 41–46.

[5] ——, "Development of InGaAs-based multiple-junction surface tunnel transistors for multiple-valued logic circuits," in *Proc. 28th Int. Symp. Multiple-Valued Logic*, Fukuoka, Japan, 1998, pp. 7–12.

[6] T. Baba, "Development of quantum functional devices for multiple-valued logic circuits," in *Proc. 29th Int. Symp. Multiple-Valued Logic*, Freiburg, Germany, 1999, pp. 2–8.

[7] T. Uemura and T. Baba, "Demonstration of a novel multiple-valued T-gate using multiple-junction surface tunnel transistors and its application to three-valued data flip-flop," in *Proc. 30th Int. Symp. Multiple-Valued Logic*, Portland, OR, 2000, pp. 305–310.

[8] T. Higuchi and M. Kameyama, *Multiple-Valued Digital Processing System* Syokodo, Japan, 1989.

[9] J. Koga and A. Toriumi, "Three-terminal silicon surface junction tunneling device for room temperature operation," *IEEE Electron Device Lett.*, vol. 20, pp. 529–531, 1999.

[10] M. W. Dashiell, R. T. Troeger, S. L. Rommel, T. N. Adam, P. R. Berger, C. Guedj, J. Kolodzey, A. C. Seabaugh, and R. Lake, "Current-voltage characteristics of high current density silicon esaki diodes grown by molecular beam epitaxy and the influence of thermal annealing," *IEEE Trans. Electron Devices*, vol. 47, pp. 1707–1713, 2000.

[11] R. Duschl, O. G. Schmidt, and K. Eber, "Epitaxially gwown Si/SiGe interband tunneling diodes with high room-temperature peak-to-valley ratio," *Appl. Phys. Lett.*, vol. 76, pp. 879–881, 2000.

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