Fabrication and evaluation of series-triple quantum dots by thermal oxidation of silicon nanowire
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Series-connected triple quantum dots were fabricated by a simple two-step oxidation technique using the pattern-dependent oxidation of a silicon nanowire and an additional oxidation of the nanowire through the gap of the fine gates attached to the nanowire. The characteristics of multi-dot single-electron devices are obtained. The formation of each quantum dot beneath an attached gate is confirmed by analyzing the electrical characteristics and by evaluating the gate capacitances between all pairings of gates and quantum dots. Because the gate electrode is automatically attached to each dot, the device structure benefits from scalability. This technique promises integrability of multiple quantum dots with individual control gates. © 2015 Author(s). All article content, except where otherwise noted, is licensed under a Creative Commons Attribution 3.0 Unported License.

I. INTRODUCTION

The fabrication of capacitively coupled quantum dot devices composed of more than two quantum dots have been attractive for quantum information processing.\(^1,\(^2\)\) Realizing quantum computations by extending the number of coupled quantum dots is the ultimate goal. Initially, a single-quantum-dot devices exploiting the two-dimensional electron gas (2DEG) formed within semiconductor heterostructures were studied for single-electron tunneling phenomena\(^3,\(^4\)\) and functional electronic devices, such as single-electron transistors (SETs).\(^5,\(^6\)\) Multiply-coupled quantum dot systems were first investigated in devices for single-electron transfer such as the single-electron pump and turnstile, and fabricated using metal dots.\(^7,\(^8\)\) To fabricate coupled multiple-quantum-dot devices more flexibly, gate-defined quantum dots were formed in the 2DEG by attaching fine gate electrodes on the surface.\(^9,\(^10\)\) The great advantage of this technique is that the configuration and formation of the quantum dots is tunable by adjusting tunnel barriers between the quantum dots by controlling the voltages applied to the gates surrounding the dots. Gate-defined coupled quantum dot devices have revealed details of electron transport of double, triple, and quadruple-quantum-dot coupled systems.\(^13,\(^14\)\) Although the devices are useful in confirming the principle of single-electron transport and quantum computing, complicated structures with many gate electrodes are needed to form the various coupled quantum dots, and in consequence the devices are not sufficiently integrated. Therefore, a new technique is required to fabricate multiply coupled quantum dots into a compact device that has a minimum number of gates attached.

With this in mind, silicon-based quantum dots have attracted interest because of higher operating temperatures and the operation stability.\(^16,\(^17\)\) In addition, by taking advantage of their long spin coherence times, their functioning as a spin-based qubit was demonstrated in a double-quantum-dot device.\(^18,\(^19\)\) Recently, triple-quantum-dot devices have been demonstrated and analyzed for
multiple qubit capability and other applications, such as for turnstile operations. These studies are suggesting the many advantages of silicon-based technology in fabricating coupled nano-dots.

Pattern-dependent oxidation (PADOX) is well known as a very simple technique in single quantum dot fabrication because it automatically converts the one-dimensional silicon nanowire to a single nano-dot along with the tunnel barriers on both sides of the nanowire by using band modulation originating from quantum-size effects and the effects of strain that have accumulated during thermal oxidation. Because thermal oxidation reduces the size of a Si dot from that of the initial nanowire defined by the lithography, PADOX-formed quantum dots are expected to have a high operating temperature because of their smaller size. However, the PADOX technique is suitable only for making a SET with a single dot because it is too sophisticated to form a dot in the middle of the nanowire. Despite the difficulty in controlling the configuration of the quantum dots, some multiple-quantum-dot fabrications have been demonstrated using PADOX to introduce lithographically a modulation in the nanowire width. Manoharan et al. fabricated using this technique an asymmetric triple-quantum-dot device that had a larger central dot and smaller side dots. However, with this technique, it is crucial to modulate the wire width to form the multiple islands. Such patterning is complicated and lacks the flexibility in device design.

Double-quantum-dot devices have previously been fabricated by applying PADOX to a Si nanowire and additional oxidation of the nanowire in the gap between the two fine gates attached on the nanowire. The characteristics of the double quantum dots have been obtained. However, details of the formation of these dots are still unknown as the position of each dot relative to each gate had not been determined. Here, we demonstrated the formation of series-triple quantum dots by attaching three fine gates on the nanowire through the same oxidation process. A 3×3-dimensional capacitance matrix among the three gates and the three dots were evaluated from the stability diagrams for electrons in the dots. The matrix makes it possible to assess the detailed positions of the triple quantum dots relative to the three fine gates. The result shows that each quantum dot was formed beneath a fine gate. The method not only makes the device compact but also self-aligns a gate electrode onto each quantum dot. Self-alignment is desirable when integrating multiple quantum dots with individual control gates.

II. DEVICE FABRICATION

Device fabrication is outlined in a sequence of diagrams [Fig. 1(a)–1(d)]. The triple quantum dots were formed automatically in the Si nanowire under the three fine gates by the two thermal oxidation steps for the nanowire [Fig. 2(a)]. The nanowire was formed by electron-beam lithography and dry etching of the 25-nm-thick Si top layer of a silicon-on-insulator (SOI) wafer with a buried oxide layer of 400-nm thickness [Fig. 1(a)]. The wire width and length were 40 and 220 nm, respectively. Two tunnel barriers at the both ends of the nanowire were formed by PADOX at 1000 °C for 70 min in a dry oxygen atmosphere, and a single long quantum dot was automatically formed between the two wide Si two-dimensional (2D) layers corresponding to the source and drain electrodes [Fig. 1(b)]. To suppress the oxidation of the 2D layers by PADOX, SiN cap layer was used. A scanning electron microscope (SEM) image of the nanowire after the oxidation is shown in Fig. 1(e). Next, the three fine gate electrodes (G1, G2, and G3) made of 200-nm thick phosphorous-doped poly-silicon were attached to the nanowire using electron-beam lithography and dry etching. The width of the fine gate electrodes was 40 nm, and the gaps between the gate electrodes were 70 nm. The additional thermal oxidation of the nanowire was performed in a dry oxygen atmosphere at 700 °C for 270 min and at 1000 °C for 8 min. This oxidizes the Si nanowire more at the gap of the fine gate because the fine poly-silicon gates disturbed the nanowire beneath the gates from the oxidation. This made a constriction in the Si nanowire at the gap just between the fine gates. These constrictions act as tunnel barriers for splitting the quantum dots, and triple quantum dots (QD1, QD2, and QD3) were formed in the nanowire under the gate electrodes of G1, G2, and G3 [Fig. 1(c)]. An SEM image of the nanowire after the formation of the three fine gate electrodes is shown in Fig. 1(f). Finally, a top gate electrode made by phosphorous-doped poly-silicon was attached over the entire area [Fig. 1(f)] after depositing SiO2 gate insulator of 50-nm thick [Fig. 1(d)]. One of the advantages of this technique is that because each of the quantum
FIG. 1. Schematic illustrations of (a) Si nanowire on SOI wafer (S and D mark the source and drain electrodes), (b) a single long quantum dot (light blue) is formed by PADOX, (c) three quantum dots (QD1, QD2, and QD3) formed by additional oxidation of the gaps between the three fine gates (G1, G2, and G3), and (d) final structure of the fabricated device. SEM images of (e) a Si nanowire and (f) three fine gates attached along the nanowire. The pitch of the gates is 110 nm (i.e. 40-nm-wide gate with 70-nm gap).

dots is formed under each of the fine gates, the number of quantum dots can be increased by increasing the number of fine gates.

III. MEASUREMENT OF TRIPLE-QUANTUM DOT DEVICE AND THE METHOD FOR EVALUATION

The configuration of the triple quantum dots was investigated by measuring the charge stability diagrams following the application of three gate voltages ($V_1$, $V_2$, and $V_3$) to the each gate electrode (G1, G2, and G3). In order to open the channel of parasitic metal-oxide-semiconductor field-effect transistors formed in the 2D Si layers at both sides of the nanowire under the top gate, which act as the source and drain electrodes of the triple-quantum-dot device, the top gate and back gate (Si substrate) voltages of 0 V and 20 V were applied, respectively.$^{38}$ The temperature during measurements was about 8 K. The equivalent circuit of the triple quantum dots with three gate voltages is shown in Fig. 2(b). Gate capacitances between Gi ($i = 1, 2, 3$) and QDj ($j = 1, 2, 3$) were defined as $C_{ij}$. In this experiment, we evaluated all the gate capacitances of two sample devices, labeled Device-A and Device-B, by using the measured stability diagrams in the regime where the inter-dot coupling capacitances ($C_{M1}$ and $C_{M2}$) are much smaller than the total capacitance of each quantum dot.
FIG. 2. (a) Schematic cross section of the triple-quantum-dot device. (b) Equivalent circuit for coupled triple-quantum-dot serial device controlled by three gate voltages ($V_1$, $V_2$, and $V_3$). Blue circles (1, 2, and 3) define three dots formed between source (S) and drain (D).

First, the stability diagrams of the double quantum dots as a function of two of the three gate voltages, $V_1$ and $V_2$ or $V_2$ and $V_3$, were evaluated; this avoids the complexity inherent in the triple-quantum-dot stability diagram. In these diagrams, seven of the nine gate capacitances were obtained; $C_{13}$ and $C_{31}$ were not. To achieve the residual two capacitances as well as to confirm the accuracy of the seven capacitances, stability diagrams were drawn in the $V_1$-$V_3$ plane with $V_2$ as a parameter.

IV. RESULTS AND DISCUSSION

We plotted the measured charge stability diagrams of Device-A (Fig. 3). Fig. 3(a) is a contour plot of the drain current ($I_D$) at the drain voltage $V_D$ of 5 mV as a function of $V_1$ and $V_2$ at constant $V_3$. The current peaks form a characteristic checker-board pattern\textsuperscript{21} associated with the stability diagram of the double quantum dot system. Although the current peak modulation in parallel along the direction of $V_2$ axis was appeared because of the coupling between G2 and QD3, the current peaks were observed when the QD1 and QD2 resonate. This is because the effect of the Coulomb oscillation for QD3 is small as the variation in $V_2$ is small and $V_3$ is fixed. In other words, the stability diagram was considered to be the characteristic of double quantum dots composed of QD1 and QD2 when the effect of QD3 was almost ignored. The yellow lines (dot-and-dash lines) and red lines (broken lines) connected the current peaks of a pair of triple-points ignoring anti-crossing characteristics and represent the boundaries of charge transitions in the double quantum dots.\textsuperscript{12,13} The
gradients of the yellow and red lines distinguish the boundaries of the charge transitions as belonging to QD1 and QD2, respectively. Four gate capacitances, \( C_{ij} \) (\( i = 1, 2, j = 1, 2 \)), can be evaluated from the two periods and gradients. Fig. 3(b) shows an enlargement of Fig. 3(a). The periods and gradients of the yellow lines were defined as \( P_{V1} \) and \( dV_1/dV_2 \) [Fig. 3(b)]. The gate capacitances between QD1 and the two gates, G1 and G2, are calculated from the measured area falls within the few-electron regime although the dot has several tens of electrons. Here, these values were obtained by averaging the data evaluated from several lines, because the periods and gradients of the lines are not constant as the measured area falls within the few-electron regime although the dot has several tens of electrons.\(^{37}\)

From the stability diagram as a function of \( V_2 \) and \( V_3 \) [Fig. 3(c)], the effect of QD1 is expected to be negligibly small in this measurement because of small variation of \( V_3 \) and fixed \( V_1 \). Two lines of different gradients can be drawn by connecting the observed current peaks, suggesting a double quantum dots forms from QD2 and QD3. The gradients of the red and green lines distinguish the boundaries of the charge transitions in QD2 and QD3, respectively. Although the gradient of the red line is different from that in Fig. 3(a) as the capacitance ratio of \( C_{22}/C_{12} \) and \( C_{22}/C_{32} \) are different, the periods for the variation of \( V_2 \) are almost the same. The gate capacitances between the dots (QD2 and QD3) and the gates, G2 and G3, were calculated to be \( C_{22} = 3.20 \) aF, \( C_{23} = 1.10 \) aF, \( C_{32} = 0.58 \) aF, and \( C_{33} = 1.58 \) aF from the periods (\( P_{V2} \) and \( P_{V3} \)) and gradients (\( dV_3/dV_2 \) and \( dV_2/dV_3 \)) of the two lines. The slight difference in \( C_{22} \) calculated from the two stability diagrams [Fig. 3(a) and 3(c)] may be attributed to the fluctuation of the effective gate capacitance in the few-electron regime.\(^{37}\) The averaged \( C_{22} \) is 3.42. As the seven gate capacitances can be evaluated from the measurements from double quantum dots formed from QD1 and QD2 or QD2 and QD3, the other capacitances (\( C_{13} \) and \( C_{31} \)) were not evaluated and believed to be much smaller than the other gate capacitances because the spatial separation from the dots is large. The result clearly shows that the gate capacitances \( C_{ij} \) were always the largest among \( C_{1j} \), \( C_{ij} \), and \( C_{ij} \), i.e., each gate \( G_k \) couples more strongly to QD\( k \) (\( k = 1, 2, 3 \)). This fact indicates that each quantum dot was formed beneath a fine gate.

For further analysis, stability diagrams of triple quantum dots were plotted giving \( I_D \) as a function of \( V_1 \) and \( V_3 \) at constant \( V_2 \). Fig. 4(a)–4(c) presents results for various \( V_3 \) in the range \(-0.50 \) V to \(-0.52 \) V. Because of thermalized electron tunneling, the conductance peaks are spread along the charge lines of each dot. Three different lines can be drawn by connecting the current peaks. The yellow (dot-and-dash), red (broken), and green (dotted) lines appear to be consistent with the boundaries of charge transition in QD1, QD2, and QD3, respectively, because the periods

![Fig. 4. Contour plots of the drain current as a function of \( V_1 \) and \( V_3 \) measured at \( V_2 = 5 \) mV and \( V_3 \) of (a) \(-0.50 \) V, (b) \(-0.51 \) V, and (c) \(-0.52 \) V. The large drain current peaks (white areas) are observed only when the triple quantum dots resonate. The boundaries of the charge transition in each quantum dot are shown as three lines: yellow (dot-and-dash) for QD1, red (broken) for QD2, and green (dotted) for QD3. All three boundaries are shifted toward higher \( V_1 \) and \( V_3 \) directions with decreasing \( V_2 \).](image-url)
TABLE I. Averaged gate capacitances ($C_{ij}$ and $C_g$-total) for Device-A.

<table>
<thead>
<tr>
<th></th>
<th>$C_{ij}$ G1 [aF] ($i=1$)</th>
<th>$C_{ij}$ G2 [aF] ($i=2$)</th>
<th>$C_{ij}$ G3 [aF] ($i=3$)</th>
<th>$C_g$-total [aF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>QD1</td>
<td>3.25</td>
<td>2.29</td>
<td>0.03</td>
<td>5.57</td>
</tr>
<tr>
<td>QD2</td>
<td>0.23</td>
<td>3.42</td>
<td>0.58</td>
<td>4.23</td>
</tr>
<tr>
<td>QD3</td>
<td>0.06</td>
<td>1.10</td>
<td>1.41</td>
<td>2.57</td>
</tr>
</tbody>
</table>

of these lines, which correspond to $e/C_{ij}$, agree well with the ones achieved above from the stability diagrams [Fig. 3(a) and 3(c)]. The stability diagram of the triple quantum dots therefore have been successfully measured (Fig. 4). The gate capacitances between the three dots, QD1, QD2, and QD3, and the two gates, G1 and G3, were calculated from the periods and gradients of each line, yielding $C_{11} = 3.20$ aF, $C_{12} = 0.23$ aF, $C_{13} = 0.06$ aF, $C_{31} = 0.03$ aF, $C_{32} = 0.57$ aF, and $C_{33} = 1.23$ aF.

In Fig. 4(a)–4(c), the red lines shift to higher $V_1$ and $V_3$ with decreasing $V_2$ whereas the yellow and green lines remained nearly unchanged. This means that the coupling of G2 with QD2 was stronger than that with QD1 and QD3. The shifts in $V_2$ for each change $\Delta V_2 = 10$ mV were found to be about 5 mV in $V_1$ axis for QD1 ($\Delta V_{3y}$, yellow lines), about 60 mV in $V_3$ axis for QD2 ($\Delta V_{3r}$, red lines), and about 10 mV in $V_3$ axis for QD3 ($\Delta V_{3g}$, green lines). Subscripts, y, r, and g, refer to the yellow, red, and green lines, respectively. The other gate capacitances can be calculated from the equations

$$C_{21} = \frac{\Delta V_1}{\Delta V_2} \times C_{11},$$

$$C_{22} = \frac{\Delta V_3}{\Delta V_2} \times C_{32},$$

$$C_{23} = \frac{\Delta V_{3g}}{\Delta V_2} \times C_{33}.$$  

Note $C_{21}$ is also written as $C_{21} = \frac{\Delta V_3}{\Delta V_2} \times C_{31} = \frac{dV_3}{dV_1} \times \frac{\Delta V_1}{\Delta V_2} \times C_{31}$. The evaluated capacitances were $C_{21} = 1.60$ aF, $C_{22} = 3.42$ aF, and $C_{23} = 1.23$ aF. These capacitances almost correspond with those calculated from the stability diagrams [Fig. 3(a) and 3(c)]. All the gate capacitances of the Device-A are summarized in Table I where the results from Figs. 3 and 4 were averaged. The total
gate capacitances of each quantum dot are also listed in the column headed $C_g$-total, where the gate capacitances of the top and back gates were ignored because these capacitances are believed to be much smaller than the total gate capacitances. An important result from Table I is that $C_{ik}$ ($i = k$) is always largest among $C_{ik}$ ($k = 1, 2, 3$). This means that three quantum dots were formed beneath their respective gates and are mainly controlled by them.

From Table I, the distribution of capacitances are asymmetric and a little irregular. The variation of each capacitances also provides important information about dot sizes and dot positions relative to each fine gate. QD1 has the largest $C_g$-total. The variation of $C_g$-total might be attributed to the misalignment of the fine gates along the nanowire during electron-beam lithography. Fig. 5 schematically presents the positional relationship between the dots (dotted circles), the fine gates (dot-and-dash square with round corner), and the nanowire (broken line), as estimated from the gate capacitances listed in Table I. The fine gates are believed to be shifted toward the direction of the drain electrode, making the size of QD1 bigger and QD3 smaller (Fig. 5). In addition, the tunnel barrier formed between QD1 and QD2 is expected to be shifted toward the QD2 because, from the SEM image [Fig. 1(e)], some narrow parts are present in the nanowire because of fluctuations occurring during lithography. Because the width of nanowire is mainly narrowed by the additional oxidation, the tunnel barrier will be preferentially formed close to the initial structural constriction of the nanowire. For precise control of the size and position of each quantum dot, improving the precision of the structure of the nanowire and the alignment of gates along the nanowire is needed. Achieving this can be done by the improvements in the lithography.

For Device-B, the characteristics of its double quantum dots were confirmed from the measured stability diagrams, Fig. 6(a) and 6(b), as a functions of $V_1$ and $V_2$ and of $V_2$ and $V_3$, respectively. These results clearly shows the formation of the triple quantum dots. Similar to Fig. 3, the boundaries of the charge transition in each quantum dot were drawn by connecting the thermally diffused current peaks, and the gate capacitances were calculated from the periods and gradients of these lines. The stability diagrams as a function of $V_1$ and $V_3$ for various values $V_2$ were also measured and gate capacitances calculated (Table II). Although values of $C_{ij}$ for the Device-B also tend to be large, G3 couples more strongly to QD2 than to QD3. The result is also explained by the fluctuation of nanowire width and slight misalignment of the fine gates attached along the nanowire. From $C_{g}$-total for each quantum dot of the two devices A and B, the size and position of triple quantum dots is found to be different between the devices despite the similarity in design. Differences in dot structure are also believed to occur from imprecisions during lithography.

<table>
<thead>
<tr>
<th>$C_{g}$-total [aF]</th>
<th>$C_{g}$-total [aF]</th>
</tr>
</thead>
<tbody>
<tr>
<td>QD1 ($j = 1$)</td>
<td>1.00</td>
</tr>
<tr>
<td>QD2 ($j = 2$)</td>
<td>0.36</td>
</tr>
<tr>
<td>QD3 ($j = 3$)</td>
<td>0.06</td>
</tr>
</tbody>
</table>
V. CONCLUSION

Triple quantum dot serial devices with control gates attached were successfully fabricated with the PADOX of Si nanowire and an additional oxidation through the gaps between the gates. From the stability diagrams for each of the two devices drawn by using three gate voltages, the formation of triple quantum dots was confirmed and the gate capacitances among the three gates and three quantum dots were evaluated. By evaluating gate capacitances between gates and dots, each quantum dot was found to form almost under a gate. The method demonstrated here enables many quantum dots to be simply fabricated in series with individual control gates attached, providing a new way to integrated coupled Si nano-dots for future single-electron transfer devices and/or quantum-bit devices.

The gate capacitances for the two devices were different although the design of the devices was the same. The variation in capacitances is believed to be attributed to the fluctuation in the initial nanowire width and the misalignment of the gates attached to the nanowire caused by the electron-beam lithography. These problems can be solved with improvements in the lithography in the future.

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