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Recent Progress in Vertical Si/III-V Tunnel FETs: From Fundamentals to Current-Boosting Technology

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Tunnel field-effect transistors (TFETs) with a steep subthreshold-slope (SS) are promising low-power switches for future large-scale integrated circuits (LSIs) with low power consumption and high performance. Recently, we demonstrated vertical TFETs with III-V/Si heterojunctions. This new sort of tunnel junction achieves a steep SS because of its unique figure-of-merit. Here, we report on recent progress on vertical TFETs using Si/III-V heterojunctions and means for boosting on-state current.

Introduction

Investigations of low-voltage switches involving non-classical carrier transport mechanisms have been increasingly in number because future electronics such as LSIs and Internet-of-Things (IoT) must simultaneously have very low power consumption and as much performance as possible (1). The main goal would be achievement of self-powered LSIs and stand-alone IoTs equipment through a combination of energy-harvesting applications. However, miniaturization of conventional field-effect transistors (FETs) is not a way to achieve this goal because of the inherent issues of FETs as regards off-state leakage current, short-channel effect, and physical limits of SS.

The switching mechanism of conventional FETs involves carrier thermal diffusion and drift, and the SS is limited to 2.3 k_BT/q (~ 60 mV/decade at room temperature). This physical limitation would enlarge the power dissipation of LSIs that feature aggressive miniaturization of FETs, because their power consumption is proportional to the square of the supply-voltage of FETs (V_{dd}), which is determined by the on/off ratio of the drain current and SS. If the reduction of the SS is limited to a constant value (60 mV/dec), the power consumption increases with the number of FETs. Further scaling of the power consumption would thus be impossible even if new gate architectures and channel materials were incorporated into Si-CMOS technologies. Steep-slope transistors with SS < 60 mV/decade are therefore required for making further reductions in V_{dd} and power consumption.

Steep-slope transistors such as tunnel FETs (TFETs) (2), impact-ionization FETs (3), mechanical switch (4), negative-capacitance FETs (5), and body-tied silicon-on-insulator (SOI) FETs (6) have attracted a great deal of attentions as possible ways to lower the SS < 60 mV/decade. Among these steep-slope transistors, TFETs whose switching mechanism involves band-to-band tunneling (7) and Zener tunneling (8) are promising millivolt switch structures that could be used as building blocks of future low-power LSIs

because their configurations have good compatibility with conventional Si-based LSIs. Using TFETs with an SS less than 50 mV/decade would reduce the total power consumption of ICs by over 90%, because a reduction in SS decreases V_{dd} as small as 0.20 V (9). In light of this, various TFETs using Si (10, 11), III-V (12-15), and graphene (16,17) have been investigated.

Almost all of these TFETs, however, had difficulties in attaining sufficient steepness (< 60 mV/decade). This is because moderate tunnel junctions and materials are still being investigated for the TFETs with a steep SS. Basically, a tunnel junction should abrupt. In the case of a p-i-n based tunnel junction, an abrupt dopant profile is required for ideal tunneling, and this needs a precise doping technique. In the tunnel junction, the area tunneling process is limited toeing within a few nanometers because of the existence of a depletion layer. On the other hand, the doping technique has difficulty forming a nanometer-scale dopant profile because of segregation of impurities and the long tail of the dopant distribution. In this regard, combining Si and III-V materials in a one-dimensional (1D) nanostructure would provide a decisive solution to the issue, because III-V/Si junctions formed by integration of III-V NWs on Si have an inherently abrupt heterojunction with band discontinuity (18, 19). We have proposed III-V NW/Si heterojunction-type TFETs. Another approach to making an abrupt tunnel junction is to use two-dimensional (2D) materials that can form an atomically flat junction. Recently, 2D-transition metal dichalcogenides (2D TMDs) with p-Ge junction have been demonstrated to have steep SS properties (20).

In this paper, we discuss the serious issues affecting the use of TFETs in future CMOS technologies and describe some new approaches to boosting the on-state current with a lower SS in vertical TFETs.

Challenges to achieving a steep SS with Tunnel FETs

Tunnel field-effect transistors (TFETs) with a steep SS are promising millivolt switches for next-generation nano-electronics. In our estimation, the SS should be less than 30 mV/decade in order to decrease the supply voltage currently 0.50 V of LSIs. TFETs with SS < 30 mV/decade would be able to reduce the total power consumption of LSIs by over 90% because the active power consumption of LSIs is proportional to the square of V_{dd}. However, few steep-slope transistors with SS < 30 mV/decade have been demonstrated (19, 21 – 23). This is because the moderate device architecture and some of the approaches are quite different from those of conventional MOSFETs and CMOS technologies. Before demonstrating vertical TFETs using III-V/Si heterojunctions, we will describe the important challenges of this device.

Series resistance

A large internal electric field should be induced at the tunnel junction under a small gate and drain bias in order to achieve a steep SS, because the SS of TFETs is ideally determined by the gate and drain bias (24). In this regard, the arrangement of series resistances is very important for inducing the internal electrical field. There are three resistances in the TFET architecture: (i) contact resistance, (ii) junction resistance, and (iii) channel resistance. The contact resistance should be small, and the other resistances are obliged to be high enough to localize the internal field at the tunnel junctions.

(i) Contact resistance. The contact resistance can be decreased by using a good Ohmic contact or controlling the contact area. In the case of III-V compound

semiconductors, Mo-related materials are moderate electrodes for lowering the contact resistance (25). For III-V NW/Si TFETs, the drain contact area can be enlarged in order to reduce the effective resistance [Fig. 1(a)] (19).

(ii) Junction resistance. The junction is a tunnel junction at which tunnel transport occurs. In the case of homojunction TFETs, controlling this resistance would be difficult because the junction is of the p-i-n. On the other hand, in the case of heterojunction TFETs, the tunnel junction usually consist of staggered Type-II [Fig. 1(b)] or broken-gap band discontinuities. Thus, the quality of the heterojunction can control the junction resistance. These heterojunctions should possess high resistance. A heterojunction has a lattice mismatch across the tunnel junction; thus, crystal defects such as misfit dislocations affect the junction resistance, as they form defect levels across the junction, which cause trap-assisted tunneling (TAT) (26). The TAT process enhances the tunneling probability while resulting in a small junction resistance. Moreover, it is basically a phonon-assisted process; thus, the SS obtained by a modulation of the TAT process is close to that of the thermoionic process (in conventional MOSFETs). It can never overcome the physical limit of the SS. In this regard, a coherent heterojunction without misfit dislocations, which induce pure band-to-band tunneling (BTBT), is required for increasing the junction resistance. In the case of an InAs NW/Si heterojunction, decreasing the diameter of the NW suppresess formation of misfit dislocations [Fig. 1(c)], as such, a steep SS can be achieved with InAs NW/Si heterojunction TFETs [Fig. 1(d)] (21).

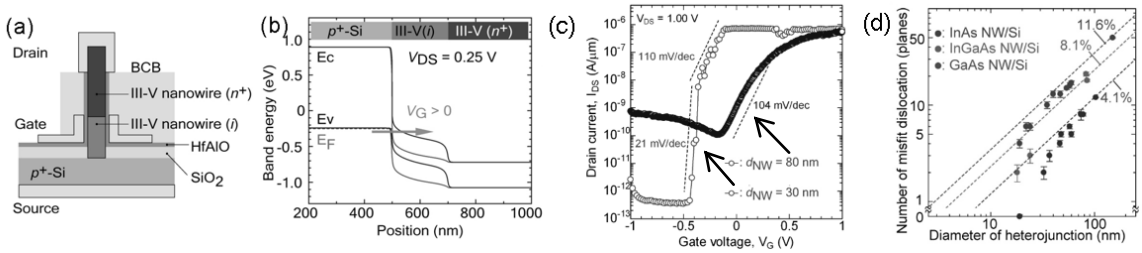

Figure 1. (a) Illustration of vertical TFET using III-V NW/Si junction, (b) Simulation of TFET, (c) Transfer curves of vertical TFET using InAs NW/Si heterojunction. V_{DS} = 0.50 V. (d) Misfit dislocations versus diameter of heterojunction. The dashed line is the number calculated from the lattice mismatch. 11.6% corresponds to InAs/Si.

(iii) Channel Resistance. A pure intrinsic layer increases the channel resistance. In the case of Si-based TFETs, an intrinsic layer can easily be formed. On the other hand, there are some challenges to making an intrinsic layer in III-V materials. III-V materials grown by MOVPE or MBE usually have the problem of unintentional doping. Thus, compensation doping is required for making the intrinsic layer. Yet, the compensation doping is still a challenge for nanostructures. InAs grown in metal-organic vapor phase epitaxy (MOVPE) is unintentionally doped by carbon dopants derived from metal-organic precursors (27), and the degree of doping depends on the condition of the reactor chamber. Typical carrier concentrations of InAs layers grown by MOVPE are $10^{16} – 10^{17}$ cm^{-3} (27), so compensation doping is required for forming an intrinsic layer. Other materials such as InGaAs and GaAs are similar to the case of InAs. Figure 2 depicts the transfer curve for the InAs and InGaAs NW-based surrounding-gate transistors on Si. When an undoped layer is used, the carrier concentrations of the InAs and InGaAs NW-channel are estimated to be 2×10^{17} cm^{-3} and 1×10^{17} cm^{-3}, respectively.

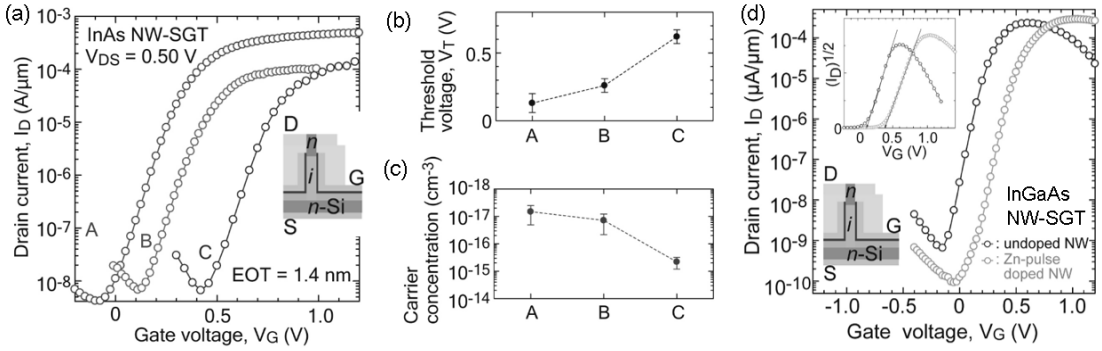

Figure 2. (a) Transfer curves of InAs NW-SGTs on Si. Curve A is for an InAs NW with an undoped channel region. B and C are for InAs NW channels made with the pulsed doping technique. B: Zn-pulse doped channel (1-sec Zn-pulses at 29-sec. intervals) C: Zn-pulse doped channel (2-sec Zn-pulse with 28-sec. intervals) (b) Variation of V_T for InAs NW-SGT for different channel segments. (c) Variation in carrier concentration estimated from V_T. (d) Transfer curves of InGaAs NW-SGTs on Si comparing undoped NW-channel with Zn pulse-doped NW channel.

Compensation with counter dopants has difficulty making an intrinsic layer in a very small NW-volume. For example, one single Zn atom as a counter dopant has an effective carrier concentration of 4.7×10^{17} cm^{-3} when the InAs NW is 30 nm in diameter and 1 nm long. A III-V NW with an even smaller diameter would have a higher net carrier concentration. Thus, the conventional compensation effect changes the conductivity of the NW; i.e., a *p*-type NW is formed. We therefore used a pulse-doping technique (28, 29) for forming a nearly intrinsic III-V NW segment in which the carrier concentration, as estimated from the threshold voltage of InAs NW SGTs on Si, was ~ 2.2×10^{15} cm^{-3} in Fig. 2 (28). In the case of InGaAs NWs, we obtained a nearly intrinsic layer with a carrier concentration of ~ 5×10^{15} cm^{-3} by using the pulse-doping technique.

Figure 3 shows the effect of the Zn-pulse doping on the properties of TFETs. Formation of a nearly intrinsic NW segment shifted the threshold voltage of the TFET from negative to positive V_G. Even at V_{DS} = 0.50 V, the SS was only 30 mV/decade. This indicates that the carrier concentration of the NW-channel segment determines the threshold voltage of the TFET structure.

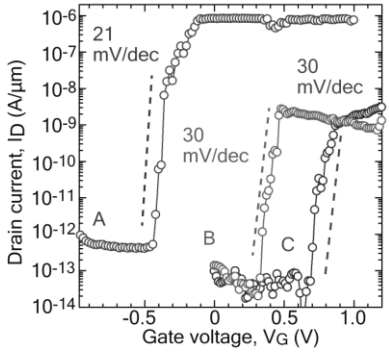

Figure 3. Transfer characteristics of steep-SS transistors using InAs NW/Si heterojunctions. Curve A is the transfer characteristic at V_{DS} = 1.00 V. Curves B and C show steep-SS characteristics at V_{DS} = 0.50 V obtained for InAs NW/Si heterojunctions with a Zn pulse-doped InAs NW-channel segment made with 1-sec pulses delivered at 29-sec intervals or 2-sec pulses at 28-sec intervals (28).

Quality of Metal-Oxide-Semiconductor (MOS) and gate architecture

The quality of the MOS interface plays a key role in achieving a steep SS in TFETs because electrostatic gate control has a dominant in the expression of SS for TFETs. Furthermore, a degraded MOS interface results in a large leakage current and eventually increases the SS. A nearly ideal SS is therefore required as a precondition for obtaining a steep SS in the TFET architecture. The III-Sb based tunnel junction fails to satisfy the precondition D_{it} and the reported broken-gap TFETs showed a very large SS (30).

The quality of the MOS interface should be optimized in a multi-gate architecture for the following reason. In TFETs, double-gate and tri-gate, (i.e., fin-gate) structures have been used to suppress off-state leakage current and the short-channel effect. These multi-gate structures should be changed to gate-all-around (GAA) or surrounding-gate structures, in which the gate-metal is wrapped around the channel to provide the best electrostatic control of the gate-bias and suppress the off-state leakage current and short-channel effect in nano-scale transistors. In addition, the area occupied by the vertical FETs is smaller than that occupied by planar FETs (31). Takato *et al*. were the first to describe the idea of and demonstrate of surrounding-gate transistors (SGTs) (32).

The SGT structure of InGaAs NWs on Si is illustrated in Fig. 4(a) (33) The device has dozens of NWs grown by selective-area growth. A description of the device process was reported elsewhere (34, 35). The In-composition of the NW was 70%. The gate-oxide was varied from 4 to 20 nm. The effective-oxide thickness (EOT) values ranged from 0.75 to 2.75 nm. The gate-length (L_G) was 200 nm. Figure 4(b) shows a representative transfer curve. The NW was 80 nm in diameter, and EOT was 0.75 nm. By using a simple approximation, the interface state density (D_{it}) was estimated to be 1.8 – 3.9 $cm^{-2}eV^{-1}$. The SS for the InGaAs NW-SGTs was almost a constant of EOT. This is because the InGaAs {-110} surface/HfAlO interface has (111)A/B microfacets on the sidewalls of the NW-channel. These microsurfaces form less Ga-oxide, which usually increases D_{it}, and they are chemically stable. Thus D_{it} is low enough to lower the SS. This specific MOS interface inherently improves electrostatic-gate control in vertical TFETs.

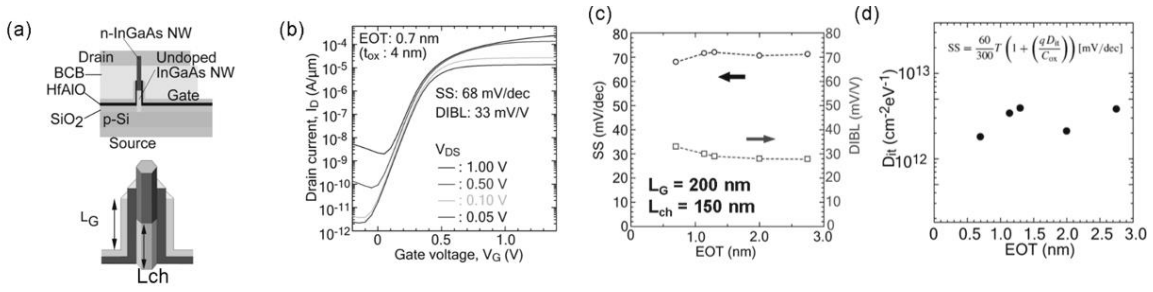

Figure 4. (a) Illustration of SGT structure. The actual device has 10 NWs in parallel with a drain contact. (b) Transfer curves for the InGaAs NW-SGTs on Si with 4-nm-thick gate oxide (EOT = 0.75 nm). (c) SS and DIBL versus EOT. (d) D_{it} estimated from panel (c).

Current-boosting technologies in vertical TFET using III-V/Si junction

TFETs have an inherently in low on-state current because of their structure inevitably has a large series resistance to obtain a steep SS. Furthermore, the tunneling process is a minor phenomenon compared with conventional carrier transport mechanisms such as the thermal diffusion and drift. This is a serious issue for utilization of TFETs in future LSIs.

CMOS researchers seem to favor increasing the carrier concentration in the source region as a way of increasing current flow. However, while this is a simple approach for conventional CMOS devices, the situation is completely different for TFETs. When the source edge is heavily doped, the degeneration of energy band and Urbach tails will occur at the tunnel junction; thus, the quality of the tunnel junction is deteriorates and phonon-assisted tunneling becomes dominant, meaning the SS becomes larger. Furthermore, the Fermi-level on the source side will overlap that of the channel region. This results in increasing the tunneling probability, while the tunneling leakage current from the channel to the source edge is simultaneously increases, resulting in a large SS. The optimum carrier concentration of the source region should empirically be on the order of 10^{18} cm^{-3}, which induces no BTBT (negative differential resistance) under the forward bias condition. Thus, another approach besides increasing carrier the concentration is required for increasing the on-state current. In this section, we discuss current-boosting technics, i.e., scaling the channel-length and exploiting strain effects.

Channel-length scaling

We investigated the effect of channel-length (L_{ch}) scaling in InGaAs NW/Si heterojunction-type vertical TFETs (29). Figure 5 shows the L_{ch} dependence of the transfer curve at a V_{DS} of 0.10 V. L_G was 150 nm. The growth conditions and sequence of the Zn-pulse doping were the same for the different L_{ch} conditions. Figure 5(b) plots SS versus drain current. The steep SS region (< 60 mV/decade) in Fig. 5(b) widens with decreasing L_{ch}. The boundary from sub- to super-60 mV/decade (I_{60}) (36) also increases for shorter L_{ch}. I_{60} was 10^{-12} A/μm for L_{ch} = 50 nm. Thus, an internal electrical field was effectively induced with a short L_{ch} as compared to a long L_{ch}.

Drain current in Figure 5(a) achieved with a short L_{ch} reached 10^{-7} A/μm, which is 100 times that of a long L_{ch}. This indicates that the source edge should be closer to the tunnel junction in order to enhance I_D, since tunneling carriers are influenced by scattering processes in longer channels. In addition, the device structure in this case had no ideal well-gated structure at the heterojunction. The scaling of L_{ch} to increase I_D would likely be effective for L_{ch} < 10 nm because the tunnel distance is usually on the scale of several nm. Thus, scaling L_{ch} has a synergetic effect of increasing both I_{60} and I_D.

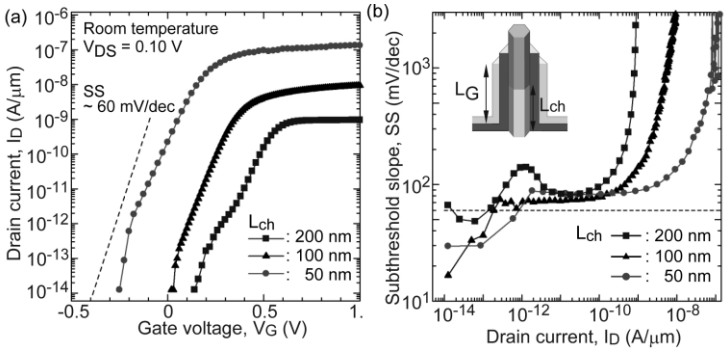

Figure 5. (a) Transfer curves for different values of L_{ch}. V_{DS} = 0.10 V at RT in the dark. The dashed line plots the theoretical limit of carrier thermal diffusion (SS = 60 mV/decade). (b) SS as a function of drain current. The dashed line shows the limit of MOSFETs (= 60 mV/decade). The inset illustrates the NW-channel. Note that the device was different from that of Figure 4.

Exploiting the strain effect

The NW-based vertical TFETs can exploit the strain effect induced by the core-shell (CS) structure of the NW. This CS structure also has a passivation effect on the NW-channel. Here, we formed InGaAs/InP CS NW channels on Si substrate. InGaAs/InP is a lattice mismatched system inducing strain across the InGaAs/InP heterostucture when the InP is pseudomorphically grown.

Figure 6(b) shows the representative transfer properties of the InGaAs-InP core-shell NW/Si TFET at drain-source voltages (V_{DS}) of 0.05 – 1.00 V. L_G and L_{ch} were 200 nm. This switching behavior appeared at a V_{DS} as low as 10 mV. The I_{ON}/I_{OFF} ratio was approximately 10^5 at a V_{DS} of 0.10 V. The threshold voltage, V_T, of I_{DS} was -0.10 V. The dark Zener current of the diode structure was modulated by V_G. I_{ON} was ~ 10 nA/μm at $V_{DS} = V_G - V_T = 0.50$ V. The drain-induced-barrier lowering (DIBL) was 10 mV/V, which is much smaller than that of conventional MOSFETs. This indicates the internal electrical field was applied at the tunneling junction despite the lowering of the surface potential due to V_{DS}.

On-state current for the InGaAs-InP core-shell NW/Si TFET was three times higher than that of the bare InGaAs NW/Si TFET. The benefit of using the InP shell layer is the improvement in SS and enhancement of I_{ON}. The InP shell has a passivation effect on the semiconductor/oxide interface (37), which decreases the interface-state density, and thus results in an electrostatic improvement in SS below 60 mV/dec. The strain effect of the InP shell layer also assists to improve the SS and I_{ON}. The outer InP shell induces biaxial tensile strain against the whole core-InGaAs NW due to the lattice mismatch (-1.16%), and the uniaxial compressive strain is localized to being near the tunneling junction (InGaAs/Si junction) and along the axial direction. The compressive strain possibly lowers conduction band minimum of the core InGaAs NW to adjust the Fermi levels across the junction. Then, it decreases the effective energy gap across the Si and InGaAs junction. Although further characterization of the strain is required, these results show that the strain effect of the CS structure can be used to increase on-state current while maintaining a steep SS.

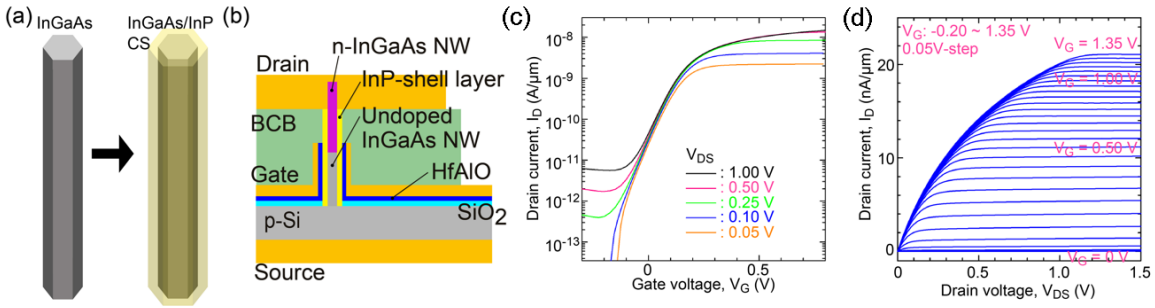

Figure 6. (a) Illustration of InGaAs/InP CS NW. (b) Illustration of device architecture. (c) Transfer properties of the vertical TFET using InGaAs/InP CS NW. (d) Output properties of the TFET.

Conclusion

We reported on recent advances in vertical surrounding-gate TFETs using III-V/InAs NW heterojunctions. We also discussed several milestones for achieving a steep SS with these TFETs and demonstrated that a vertical TFET with an InGaAs/Si junction has a steep SS. In addition, we discussed current-boosting technologies such as channel-length scaling and exploiting the strain effect of the core-shell NW structure. We plan to develop energy-efficient circuits by integrating the TFETs based on Si/III-V heterojunctions into a Si-LSI platform.

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