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<b>Citation</b>	ECS Transactions, 75(5), 265-270 <a href="https://doi.org/10.1149/07505.0265ecst">https://doi.org/10.1149/07505.0265ecst</a>
<b>Issue Date</b>	2016-10
<b>Doc URL</b>	<a href="http://hdl.handle.net/2115/64540">http://hdl.handle.net/2115/64540</a>
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<b>Type</b>	article
<b>File Information</b>	ECS Trans.-2016-Yoshida-265-70-SAG of InGaAs on Ge.pdf



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## Selective-Area Growth of Vertical InGaAs Nanowires on Ge for Transistor Applications

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III-V compound semiconductors and Ge are promising future channel materials because of their high carrier mobility. For example the electron mobility of InAs is about 20 times faster than that of Si at room temperature and hole mobility of Ge is about 5 times faster than that of Si. In this paper, we report direct integration of InGaAs nanowires (NWs) on Ge(111) substrate by selective-area metal organic vapor phase epitaxy (SA-MOVPE) for realization of high carrier mobility InGaAs/Ge hybrid CMOS applications, and characterization of the composition and growth modes of InGaAs NWs by X-ray diffraction (XRD) measurement.

### Introduction

The greatest challenge in future electronics, especially the integrated circuits (ICs), is to realize high performance while reducing power consumption. Thus, several techniques, such as three-dimensional gate structures (1), new channel materials with high carrier mobility (2,3), and higher degree of integration have been reported to lower supply voltages of metal-oxide-semiconductor field-effect transistors (MOSFETs). III-V compound semiconductors and Ge are expected as next-generation channel materials because of their high carrier mobility (4 – 6). However, there has been few reports on cointegration of III-V and Ge. In addition to a difficulty in realizing III-V/Ge hybrid structures, one of the reasons is in the carrier mobility mismatch. That is, if InGaAs n-channel MOSFETs have field-effect mobility of 12000 cm<sup>2</sup>/Vs for electrons and Ge p-MOSFETs have that of 1200 cm<sup>2</sup>/Vs for holes, the channel width of n-MOSFETs must be 10 times smaller than that of p-MOSFETs for the same gate length to overcome current density mismatch and to realize complementary-MOS (CMOS) logic. So rational integrated structure is required to overcome bottleneck due to the mismatch of carrier mobility.

Figure 1 illustrates our targeting hybrid CMOS inverter composed of a III-V nanowire (NW) vertical n-MOSFET and a planar Ge p-MOSFET and its equivalent circuit. This structure can be realized by utilizing selective-area metal-organic vapor-phase epitaxy (SA-MOVPE) of III-V NWs on Ge substrates. In this structure, the mismatch associate with the mobility can be canceled by using wider channel for p-MOSFET and it is possible to match current levels of III-V n-MOSFETs and Ge p-MOSFETs. Furthermore, direct integration of the III-V NWs by SA-MOVPE would

suppress the formation of misfit dislocations at III-V/Ge interface owing to lattice mismatch (7) and reduce occupied area by about one quarter compared with conventional planar Si-MOSFETs (8). Among the III-V NWs, InAs and InGaAs NWs are promising materials as the fast channel of n-MOSFETs because of their small effective electron mass and high electron mobility. Especially, InGaAs NWs with In composition of about 70% are promising because of their good gate controllability as well as their high electron mobility (9), thus it is expected to outperform performance of InAs channel NW n-MOSFETs reported previously (10). However, although InGaAs alloy and InAs seem similar material sharing As, as a common anion, care must be taken for the choice of their appropriate growth conditions. Indeed, as in the case of III-V NW growth on Si substrates, the growth sequence for InAs NWs, particularly at the initial stage, is not directly applicable for InGaAs NWs (11). Control of alloy composition is also an important issue and is known to depend various parameters in the SA-MOVPE growth (12).

In this paper, we report on the growth of InGaAs NWs on Ge(111) substrate by SA-MOVPE towards proposed CMOS structure. We will mainly describe the effect of growth temperature in InGaAs NW growth and characterization of their In-composition by X-ray diffraction (XRD) measurement.

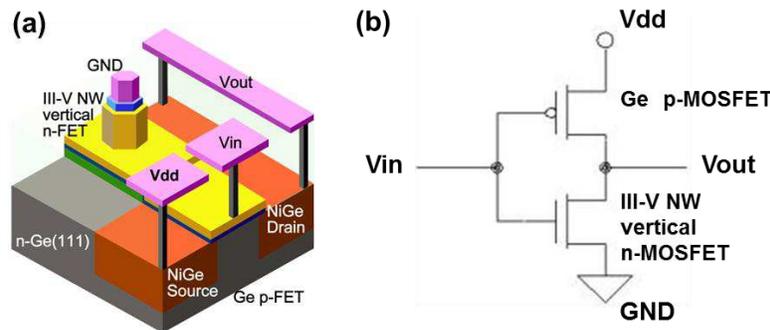


Figure 1. III-V/Ge hybrid CMOS structure. (a) Illustration of a hybrid CMOS inverter composed of a III-V NW vertical n-MOSFET and a Ge p-MOSFET and (b) its equivalent circuit.

## Experimental Details

The procedure of SA-MOVPE growth for InGaAs NW is as follows. A 22 nm-thick SiN film was deposited on a Ge(111) substrate as a mask by plasma enhanced chemical vapor deposition (PECVD). Mask pattern was defined by electron-beam (EB) lithography and wet chemical etching by buffered hydrofluoric acid (BHF). In the present study, we prepared two types of masked substrates. Both consisted of a periodic array of circular openings with the diameter  $d_0$  and pitch  $a$ , but area of the patterned regions were different. In pattern A [Figure 2(a)], the array of openings was defined in 100  $\mu\text{m}$  by 100  $\mu\text{m}$  regions, and the patterned regions having different  $d_0$  and  $a$  were placed by 100  $\mu\text{m}$  apart. Ge surface was exposed in between the patterned regions. In pattern B [Figure 2(b)], the size of a patterned region was 4mm by 4mm with fixed  $d_0$  and  $a$ , and Ge surface was also exposed outside of the patterned region. The pattern A has been used in our previous experiments [see, for instance Ref. (13)], and the pattern B in the present study was for XRD measurements. In the following, results for  $a=1\mu\text{m}$  and  $d_0=100\text{ nm}$  will be described.

Then NWs were grown on both patterned substrates at the same growth run in a horizontal MOVPE system with working pressure of 0.1 atm. The source precursors for the growth were trimethylgallium (TMGa), trimethylindium (TMIn), and arsine ( $\text{AsH}_3$ ). To form (111)B polarity (11, 14) on non-polar Ge(111) surfaces, following procedures were taken (10). After the native oxide on Ge surfaces was removed by thermal cleaning in a hydrogen atmosphere at  $550^\circ\text{C}$  [Figure 4(c)] (15),  $\text{AsH}_3$  was supplied [(1) in Figure 4(c)] for the replacement of outermost Ge with As in order to form As-incorporated  $\text{Ge}^{3+}$  surface. Then, InGaAs layers were grown by supplying TMIn/TMGa and  $\text{AsH}_3$  alternately with hydrogen intervals, that is, by flow-rate modulated epitaxy (FME) [(2) in Figure 4(c)] (16). It should be emphasized that ensuring flat surfaces after taking these procedures was found to critically be important as well as realizing appropriate (111)B polarity. The detail will be described elsewhere. Growth of InGaAs NWs was completed by conventional MOVPE growth at temperature  $T_G$  for 30min. The temperature profile during these processes is shown in Figure 1(c). The composition of TMIn in group III precursors was 70% in the vapor.

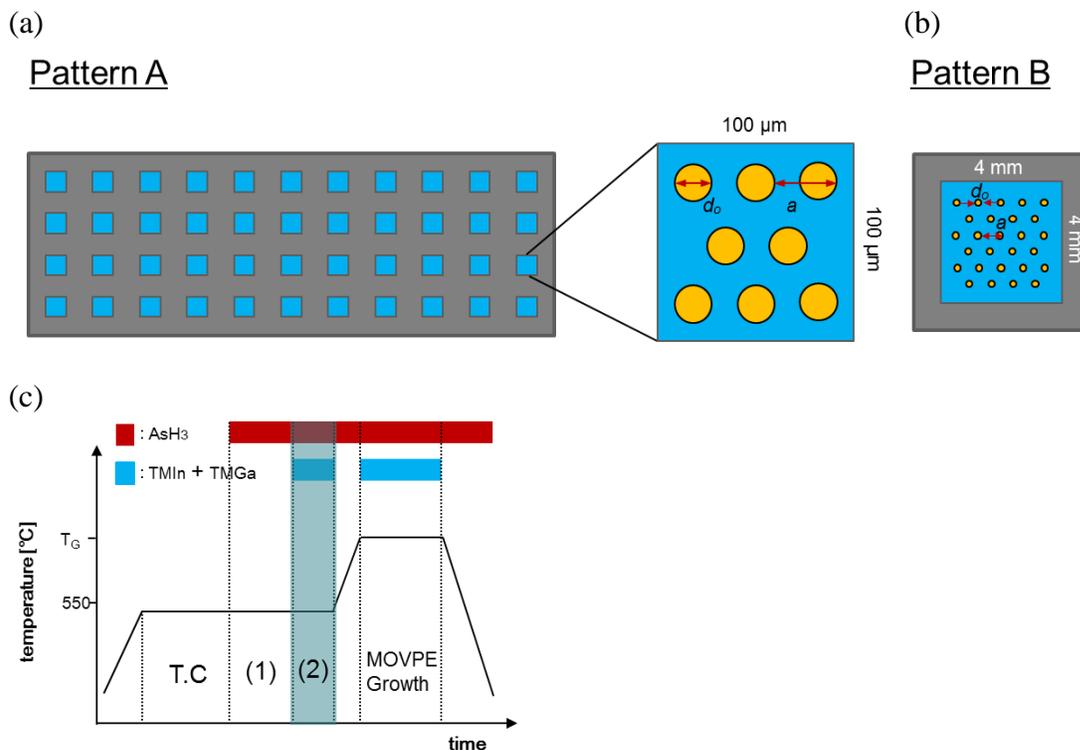


Figure 2. Two types of masked substrates. (a) The array of openings defined in  $100\mu\text{m}$  by  $100\mu\text{m}$  regions (pattern A). (b) The array of openings defined in  $4\text{mm}$  by  $4\text{mm}$  regions (pattern B). (c) Growth sequence of InGaAs NWs. After thermal cleaning (T.C),  $\text{AsH}_3$  treatment (1), and FME growth (2) at  $550^\circ\text{C}$ , conventional MOVPE growth at  $T_G$ .

## Results and Discussions

Figure 3(a) and (b) show  $30^\circ$ -tilted scanning electron microscope (SEM) images of InGaAs NWs on Ge(111) grown by SA-MOVPE at  $T_G = 670^\circ\text{C}$  and  $630^\circ\text{C}$ , respectively. Note that  $T_G$  of  $670^\circ\text{C}$  was successful temperature for InGaAs on Si (11, 17). However, very few NWs were grown on the Ge substrate, and short and wide triangular structures were grown on the opening region of the mask. The formation of these structures will be

discussed later. By lowering the growth temperature to 630°C, the yield of NW growth was enhanced very much, as shown in Figure 3(b).

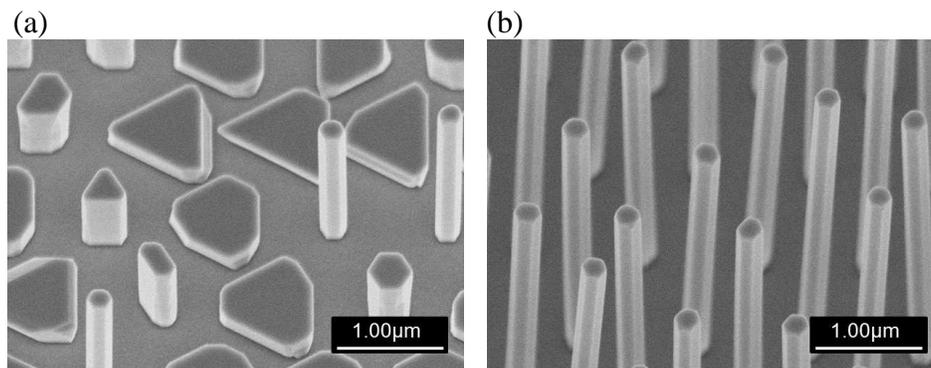


Figure 3. 30°-tilted scanning electron microscope (SEM) images of InGaAs NWs on Ge(111) masked by pattern A grown by SA-MOVPE at (a)  $T_G = 670^\circ\text{C}$  and (b)  $T_G = 630^\circ\text{C}$ .

Figure 4 summarizes the results of the growth on pattern B at  $T_G = 670^\circ\text{C}$  or  $630^\circ\text{C}$ . The SEM images were obtained in the patterned area [Figure 4 (a) and (d)] and outside of the patterned area [Figure 4 (b) and (e)] where no mask was present and bare Ge surface was exposed. We noticed that the yield and the uniformity of NWs were considerably deteriorated on pattern B. That is, more InGaAs layer formed in the mask opening region of the pattern B tended to grow in the lateral direction and showed triangular structures than in the case of pattern A, and only a few InGaAs grew in the vertical direction with  $\{-110\}$  side walls and (111)B top facets and exhibited a NW form. The uniformity of the NW array was slightly improved by decreasing  $T_G$  [Figure 4(d)], but is still worse than on pattern A. If one looks at the outside of the pattern regions [Figure 4(b) and 4(e)], similar triangular or tetrahedral shape were observed. The results of the outside of the patterned regions, or planar regions, are due to a large mismatch between Ge and InGaAs layer, and similar problems associated with lattice mismatch is thought to took place for the triangular structures formed in the patterned regions.

Figure 4(c) and (f) show results of XRD measurement on pattern B and its outside grown at  $T_G = 670^\circ\text{C}$  and  $630^\circ\text{C}$ , respectively. Two peaks, namely, peak (a) and (b), were observed for the patterned area grown at  $670^\circ\text{C}$ . The position of the broad peak [peak (b)] that appears at the higher angle were the same as that from outside of the patterned area. By comparing this with aforementioned SEM images of the two regions, we conclude that these peak are from the laterally grown region on the planar or patterned regions, and peak (a) originates from InGaAs NWs grown in the patterned regions of the pattern B. Based on this, In-composition in InGaAs NWs is 89%, and that in the triangular structures and layers of InGaAs outside of the patterned area is 69%. For  $T_G = 630^\circ\text{C}$ , the XRD spectra looked similar to those for the higher temperature both at patterned regions and outside of the pattern area, except for the lower angular shift, indicating that the higher In composition for the samples grown at  $630^\circ\text{C}$  was 93% for NW and 75% for the planar or laterally grown structures in the patterned area, respectively.

Deterioration of the uniformity in pattern B is often observed in our experiment, and is not limited to the issue of the growth of InGaAs on Ge. We think this is due to the too much effective supply of the group III species in the SA-MOVPE (13). In MOVPE

growth, growth rate is determined by the supply of group III species, and their diffusion in gas-phase and on the surface alters their amount at the mask opening. In general, the less the ratio of the opening region to the masked region becomes, the more the materials diffuse to the opening regions, resulting in the enhancement of the growth. Since the pattern B has less opening regions, the amount of group III species which contribute to the growth is much larger in pattern B than in pattern A. Thus, dynamics of the growth is different between two patterns. Nonetheless, we believe that tendency that In composition in the InGaAs NW is larger than the In composition in the vapor phase, and that it increases with decreasing the growth temperature is the same for both in pattern A and B, because the difference of diffusion due to mask pattern influences both Ga and In and would not change the tendency of their incorporation. The difference of In composition in the solid and vapor implies that incorporation rate of In and Ga is different, and that of In is larger than that of Ga at the present growth conditions. Increase of In incorporation at lower growth temperature is mainly due to the suppression of re-evaporation of In from InGaAs layers and is thought to be a consequence of the nature of In-rich InGaAs NWs (12).

Reference (12) also shows the incorporation of Ga is less dependent on the growth temperature in In-rich InGaAs. If one assumes the incorporation of Ga is independent of the growth temperature  $T_G$ , amount of incorporated In is increased by about 1.3 times and 1.6 times in NWs and planar regions in pattern B, respectively, when the  $T_G$  is lowered from 670°C to 630°C. Thus, to obtain InGaAs with In composition of about 70% at  $T_G=630^\circ\text{C}$ , it is required to reduce the supply amount of In in the vapor by about 30% to 60%, that is, the supply ratio of In in the vapor phase should be reduced from 70% at 670°C to about 64% to 59% at 630°C. Optimization of the growth temperature as well as the In composition for InGaAs NWs will be described elsewhere.

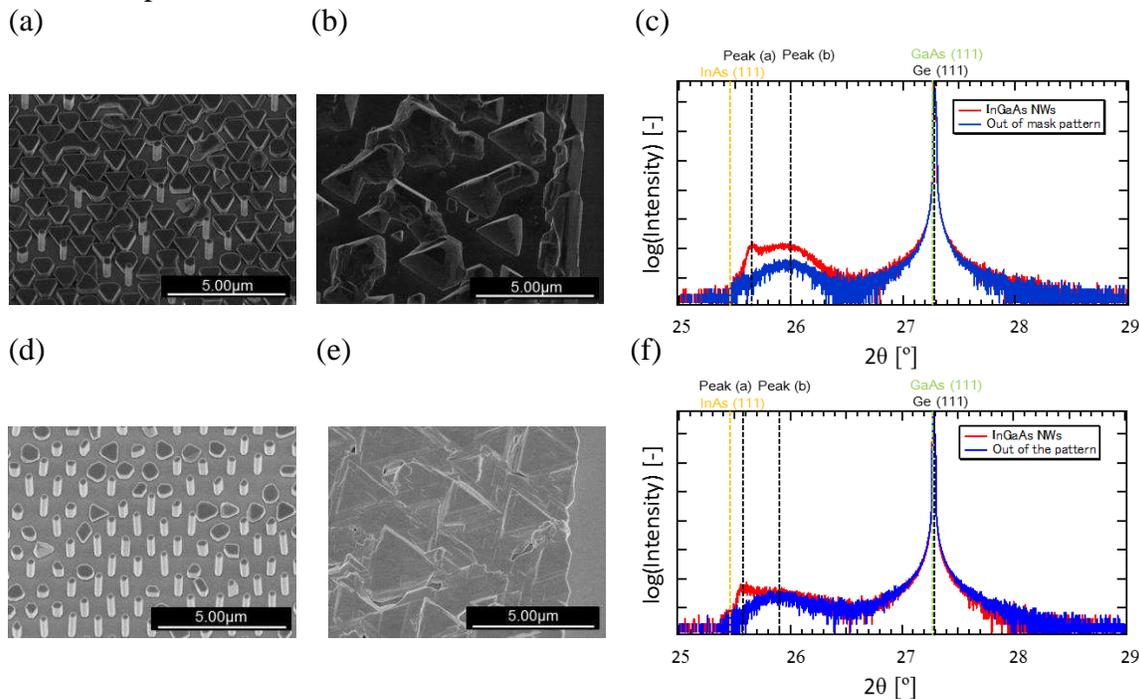


Figure 4. SEM images and XRD spectra of InGaAs on Ge(111) masked by pattern B grown by SA-MOVPE at  $T_G = 670^\circ\text{C}$  (a - c) and  $T_G = 630^\circ\text{C}$  (d - f). (a) and (d) in the patterned area. (b) and (e) outside of the mask pattern. (c) and (f) the results of XRD measurement.

## Summary

We have carried out SA-MOVPE growth of InGaAs NWs on Ge(111) substrates towards their direct integration for III-V/Ge hybrid CMOS structures. By optimizing the preparation scheme prior to the InGaAs NW growth, uniform array of vertical NWs were successfully formed. XRD measurement revealed that the In-composition of InGaAs NWs was larger than those in the vapor phase, and increased with decreasing the growth temperature. Further optimization of the growth is required for more accurate control of In-composition in InGaAs NWs.

## Acknowledgements

The authors would like to thank Mrs. Y. Hiraya for his support of the experiments and Professor T. Fukui and Professor S. Hara for their helpful discussion. This work was financially supported by a Grant-in-Aid for Scientific Research from the Ministry of Education, Culture, Sports, Science, and Technology, Japan Science and Technology Agency (JST), and Murata Science Foundation, which the authors gratefully acknowledge.

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