# Study on Threshold Logic Circuit Implementation Using GaAs-based Nanowire Network and High Precision GaAs Digital Wet Chemical Etching for Nanowire Network Formation

(GaAs ナノ細線網を利用したしきい論理回路実装と細線網形成のための高精度 GaAs デジタル湿式化学エッチングに関する研究)

*A dissertation submitted in partial fulfillment of the requirement for the degree of Doctor of Philosophy (Engineering) to Hokkaido University*

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By

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Dedicated to my parents, Iwao Kuroda and Hiroko Kuroda

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# Contents

# Chapter 1
# Introduction

## 1.1 Background

For the past few decades, a remarkable development of the complemental-metal-oxide-semiconductor (CMOS) large-scale integrated circuit (LSI) technology has been achieved in accordance with Moore's law [1,2]. The strong motivation for the development is in the scaling principle for the field-effect transistor (FET), in which the performance of the FET is improved by reducing the device dimension. Current von Neumann-type computers have received much benefits from the Si CMOS LSI technology. However, the scaling of the Si MOSFETs is facing the physical limit [2]. For example, the channel length of the Si MOSFET reaches sub-10 nm, corresponding to the Si atoms less than twenty. The slowdown of the growth in the computing performance is inevitably arising from such fundamental limitations. To overcome the limitations above, it is necessary to find a novel computing architecture that can efficiently solve the computationally intractable problems, in which the conventional von Neumann type computers cannot solve within a realistic time scale. Here it is also necessary to find a physical implementation scheme which enables to process a huge number of data with high energy efficiency. For such highly energy efficient

and massive data processing capability, a possible approach is to use the integrated nanostructures of the III-V compound semiconductors. Most of III-V semiconductors have higher electron mobility than that of Si [3]. The high carrier mobility offers the electronic circuits the low power consumption. Recent advanced nanotechnology can produce very high density III-V semiconductor nanodot arrays and nanowire networks which have superb electronic and optoelectronic properties. Here an important issue is to find an appropriate logic architecture which can take advantage of the integrated III-V semiconductor nanostructures.

On the other hand, it is also very important to develop the III-V compound semiconductor process technology that can fabricate high density nanostructure in precisely size-controlled and reproducible manner. The properties of the compound semiconductor nanodevices depend greatly on their nanostructure. It is necessary to have an etching technique that can form the structure precisely in nanometer scale without damage. Although the conventional dry etching can precisely control the physical structure dimension, it inevitably causes very high damage on the semiconductor surface [4]. In contrast, the wet chemical etching can achieve very low damage, however this technique has difficulty in the precise control of the etching amount and the cross sectional structure. At present, we do not have the etching technique suitable for the III-V compound semiconductor nanostrcuture formation.

## 1.2 Objective of this work

Based on the background above, the objective of this thesis is the implementation of the threshold logic architecture using GaAs-based nanowire networks and the development of the high precision wet chemical etching technique for formation of the III-V semiconductor nanowire network. The threshold logic [5,6] is one of the representation schemes of Boolean logic function and it is implemented by a threshold device network. The concept of this work is to implement this logical threshold device network structure using a gate-controlled GaAs nanowire network [7,8]. I designed the threshold logic circuit integrating the nanowire FETs, fabricated a two-input threshold logic circuit using the GaAs nanowire network, and demonstrated its logic operation. Then, for implementation of large-scale threshold logic circuit on high density GaAs nanowire network, I investigated the digital wet etching technique using a computer controlled multi spray system. The computer controlled system makes it possible to expose the sample surface to the etchant and rinse solutions in sub-second time scale and in repeated manner. I developed the etching machine and optimized the etching parameters. Then I could achieve atomic-level wet chemical etching of the GaAs, preferable for nanostructure formation.

## 1.3 Synopsis of each chapter

The chapter 1 describes the background and objective of this work.

The chapter 2 describes the basic concept of the threshold logic and possible approaches to electrical circuit implementation.

The chapter 3 describes the formation of the GaAs nanowire network, basic transport properties of the GaAs nanowire field-effect-transistor (FET), and electrical characteristics of the fabricated GaAs nanowire FET.

The chapter 4 describes the circuit design of the threshold logic in this work, implementation of the threshold logic circuit using the GaAs nanowire network, and the results of the characterization of the circuit operation. Logic-gate operation of NOR and NAND were successfully demonstrated in the same circuit.

The chapter 5 describes the reconfiguration of the logic function in the threshold logic circuit. As a possible approach to intentionally shift and hold the threshold, metal-insulator-semiconductor (MIS) GaAs nanowire FET was investigated. I fabricated GaAs nanowire MISFETs and demonstrated the threshold shift and its retention. I also demonstrated the threshold shift on an inverter circuit.

The chapter 6 describes the computer-controlled digital wet chemical etching of GaAs-based materials using $H_2SO_4$-based etchant. The low etching rate of 25 nm/cycle was achieved, which was ten times smaller than the conventional wet etching using the $H_2SO_4$-based etchant [9]. From characterization of the cross section structure, anisotropy etching was confirmed.

The chapter 7 describes the high precision wet etching by separating the oxidation and dissolving the oxide processes [9-11]. By alternating the

oxidation and dissolving in a short time, high accuracy etching with 2 nm/cycle was achieved. Structure formation mechanism based on the reaction dynamics was discussed to understand the observed spontaneous nanostructure formation on the surface.

Chapter 8 summarizes the conclusion of this work.

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# Chapter 2
# Threshold logic and Implementation

## 2.1 Introduction

So far, von-Neumann type computers have been greatly developed and achieved remarkable computing performance. However, there are the computationally intractable problems at which the von-Neumann type computer is weak. The computation time exponentially grows when the number of the variables increases, which is called as "combinational explosion". For solving such intractable problems efficiently, it is necessary to develop an alternative computing architecture and its hard ware implementation scheme. It is expected to implement such architecture using the semiconductor nanostructures because of its unique functions available in nanometer scale, as well as the low power consumption and high density integration capabilities. In this work, I employ the threshold logic as a logic architecture easily implementable using the semiconductor nanostructure.

The threshold logic [1-3] is a simple logic architecture. This basic element of this architecture corresponds to that of the nerve signal system. The threshold logic has been studied since 1960s [1,2]. Several studies have reported about electrical threshold logic circuits. The threshold logic is called

as a majority voting logic. If the summation of the inputs for the node exceeds the threshold value, the output is considered as high, otherwise low. The fundamental logic gates such an AND-gate, an OR-gate, a NAND-gate, and a NOR-gate are represented by a threshold logic circuit. The threshold logic has a very wide range of applications because of its simple operation principle as described above. It is applicable to image processing [4], neural network, and cellular automata calculation [5]. However, except for basic logic gates, circuit applications using the threshold logic were rarely employed commercially, because of the trade-off among power consumption, number of elements, and signal-to-noise ratio. Therefore the issues in the application of the threshold logic is to construct the element as simple as possible and to reduce power consumption. A possible approach to satisfy these requirement is to implement the threshold logic using the III-V compound semiconductor nanodevice.

## 2.2 Concept and architecture

In this subsection, I will explain the basic function of the threshold logic device. A schematic image is shown in Fig.2-1, where $X_i$ is the input, $W_i$ is the weight, $\theta$ is the threshold value, $\Sigma$ is the summation operator, and Y is the output. As mentioned above, the threshold logic consists of a summation and a threshold function.

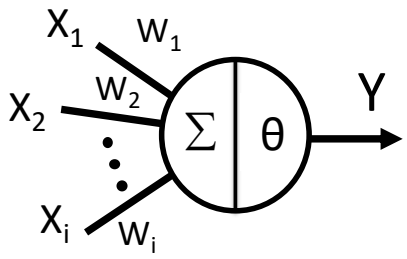


Fig. 2-1 A schematic of threshold logic.

The threshold logic function is represented by Eq. (2.1). The output Y of the element is "1" when the summation of the multiple inputs exceeds the threshold value θ, otherwise it is "0" [1,2]. Namely,

$$\text{If } \sum_i w_i x_i \geq \theta \text{ then } Y = 1 \text{ else } Y = 0. \tag{2.1}$$

In this work a two-variable binary logic, $i = \{0, 1\}$, is considered. As the waveforms shown in Fig. 2-2, the binary inputs are summed up into three levels as Fig.2-2(a). If the threshold value is set between low and middle levels, $\theta = \theta_2$, the circuit operates as an OR gate. On the other hand if the threshold value is set between high and middle levels, $\theta = \theta_1$, it operates as an AND gate as Fig. 2-2(b). The threshold logic circuit is configured without weighting in this study in order to handle only the basic logic gate.

## 2.3 Circuit design and implementation

As mentioned above, the threshold logic has been studied since 1960s. The threshold logic was implemented by the bipolar transistor circuit [5],

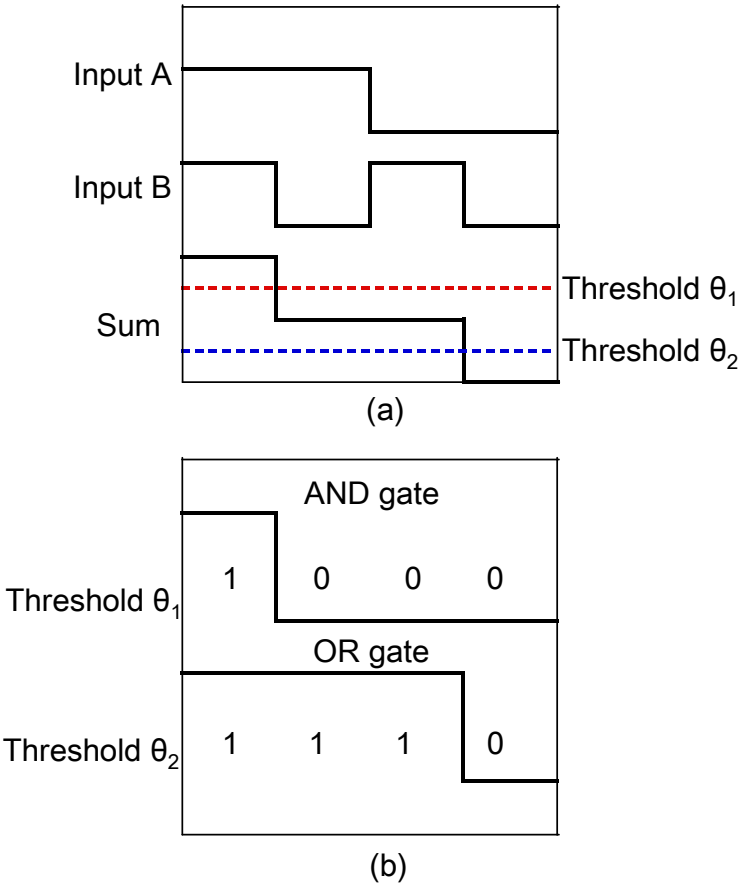


Fig. 2-2 Example of threshold logic operation. (a) The waveform of inputs and summation. (b) The waveform of output when threshold value is $\theta = \theta_1$ or $\theta = \theta_2$.

double gate MOSFETs circuit [7], neuron-MOS transistors [8], resonant tunneling diodes [9-11], switched capacitors [12], nanomagnetic devices [13-15], or SiGe heterostructure bipolar transistor (HBT) [16] has been studied.

To implement of threshold logic, it needs to design the summation circuit and the threshold function circuit. In this work, the threshold logic circuits are utilizing the FETs only in order to implement of the circuit on the III-V compound semiconductor nanowire network. Therefore, the summation

circuit is composed by current summation circuit based on Kirchhoff's low which can be composed by less number of elements. As a threshold function, I employ the inverter circuit.

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# Chapter 3
# Formation and Properties of GaAs Nanowire Network

## 3.1 Introduction

It is expected that the novel computing architecture is implemented using the III-V compound semiconductors. This is because III-V semiconductors have high electron mobility and high saturation velocity, and III-V semiconductor-based nanodevice such a nanowire FET can operate with low power consumption.

GaAs is one of the III-V compound semiconductors. GaAs has high electron mobility and high saturation velocity. In the microwave circuits, it contributes to greatly reduce the channel transit time and achieves the high frequency operation. Because the GaAs and AlGaAs have almost the same lattice constant of 5.653 Å, they can form a good heterointerface. Because of the good heterointerface, the AlGaAs/GaAs high electron mobility transistor (HEMT) which achieves the high speed and low noise operation has been developed. The AlGaAs/GaAs HEMT spatially separates the doping layer and the channel layer, called as a modulation doping. This technique enables the lower noise and higher electron mobility than those of the GaAs bulk

structure [1]. This AlGaAs/GaAs HEMT was innovated by Mimura et al. [2]. Recently the AlGaN/GaN HEMT has attracted the attention of the power electronics [3].

The development of nanotechnology enabled us to form a variety of semiconductor nanostructures. The nanowire structure is one of the semiconductor nanostructures. The nanowire structure can reduce the short channel effect which is a problem in the planer transistor with sub-100 nm gate. The gate controllability of the nanowire FET is increased by wrapping up the nanowire channel with the gate electrode. By wrapping up the nanowire channel with the gate electrode, the drain-source leak current can be reduced. The nanowire transistor is expected for future electric devices.

In this chapter the electron transport of the AlGaAs/GaAs HEMT structure, formation of the GaAs-based nanowire and its network, and the characteristics of the GaAs-based nanowire FET are described. For implementing a threshold logic circuit, it is desired that the nanowire FET which has good gate controllability and positive threshold voltage is integrated on a nanowire network.

## 3.2 Basic properties of GaAs and related materials

GaAs has the electron mobility as high as 8000 $cm^2/V \cdot s$. The saturation velocity of the electron is $6 \times 10^6$ cm/s. The comparison to other semiconductor materials is shown in Table 1. In this study, the High-electron-mobility-transistor (HEMT) wafer was used for the nanowire network and

Table 1 Properties of semiconductors [1]

| Semiconductor | Electron mobility at 300K ($cm^2$/V-s) | Effective mass ($m^*/m_0$) |
|---|---|---|
| Si | 1450 | 0.19 |
| GaAs | 8000 | 0.063 |
| GaN | 400 | 0.27 |

nanowire FET. The wafer structure and band diagram is shown in Fig.3-1. It consists of AlGaAs and GaAs. Due to the same lattice constant between GaAs and AlGaAs, the electronic property is not degraded by defect which is introduced by lattice mismatch. The AlGaAs/GaAs HEMT has a high electron mobility as its name suggests. The electron mobility is 9000 $cm^2/V \cdot s$. The band gap of $Al_{0.33}Ga_{0.67}As$ and GaAs are 1.8 eV and 1.43 eV, respectively.

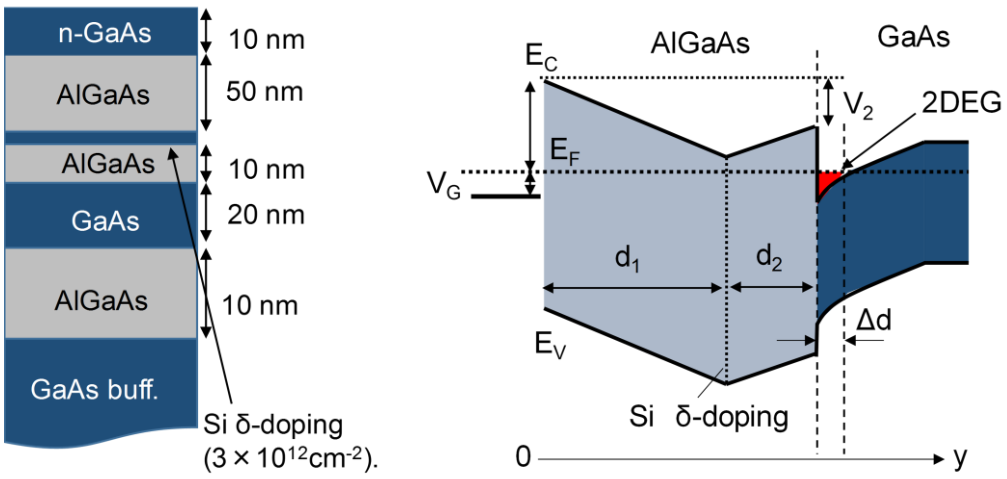


Fig. 3-1. The cross-sectional structure and band diagram of AlGaAs/GaAs HEMT.

## 3.3 Formation of nanowire and its network

There are some methods of fabrication of the nanowire. They are top-down method and bottom-up method. The nanowire structure is demonstrated by Wagner and Ellis as Si whiskers using vapor-liquid solid (VLS) growth [4]. In the VLS growth, the liquid phase seed particle such as a gold is used as a catalyst. The vapor phase precursor impinges on seed particle and nanowire grows up at the seed particle.

The other technique of bottom-up fabrication of nanowire is selective-area metal organic vapor phase epitaxy (SAMOVPE). In MOVPE, alkylation products and hydrides are used, and crystal growth is carried out by using a thermal decomposition reaction. By using the mask pattern, selectively growth is possible. The several III-V nanowire structures were demonstrated for light-emission diode or solar cell [5-9].

The top-down fabrication of nanowire is carried out by the lithography and the etching technique. Especially lithography is carried out by electron beam writer. There are some reports of Si nanowire fabricated by the dry etching or the wet etching [10-14]. The fabrication of nanowire by wet chemical etching is difficult due to side etching under the mask. The top-down fabrication method makes it easier to integrate the circuit because nanowires can be fabricated based on circuit design.

In this study, the GaAs nanowire was fabricated by the top down process with wet chemical etching. The fabrication sequence of the nanowire network and the nanowire FET in this study is shown in Fig. 3-2. A GaAs

nanowire was formed on an AlGaAs/GaAs hetrostructure wafer as shown in Fig. 3-1. The AlGaAs/GaAs wafer was cleaved in the <01-1> and <011> directions into 5 x 5 $mm^2$ chips. These chips were cleaned by acetone, ethanol, and deionized water in supersonic for 5 min, respectively. Then samples were dried by baking at 140 ℃ for 10 min. After cooling down, the Primer and the EB resist of ZEP 520A-7 were spin-coated at 500 rpm for 3 s and 5000 rpm for 30 s. The coated resist thickness was approximately 400 nm. The resist-coated chips were pre-baked at 170 ºC for 1 min and 90 ºC for 5 min. After pre-baking, the nanowire patterns were exposed using electron beam (EB) lithography (JEOL Co. JBX-6300SF). The nanowire FET patterns were exposed along <01-1> direction. Then the resist on the chips were developed by ZED-N50 (Nippon Zeon Co.) for 45 s and rinsed using 2-propanol for 45 s at room temperature. After development, the chips were baked at 140 ºC for 10 min. Then to form the nanowire network structure, they were etched by wet chemical etching. The chips were dipped in $H_2SO_4$-based etchant ($H_2SO_4$:$H_2O_2$:$H_2O$ = 8:1:1) for 1 s at 4 ºC. The etching depth was about 300 nm. The etched nanowire along <01-1> direction had a mesa-shape structure with smooth (111)B facets. Then the resist was removed by the resist remover ZDMAC (Nippon Zeon Co.). Next, the Ohmic electrodes were formed. The primer and EB resist, ZEP 520A (Nippon Zeon Co.), were coated at 500 rpm for 3 s and 5000 rpm for 30 s. The EB resist was coated twice to obtain the thick resist film necessary for the metal lift-off process. The pre-bake was carried out at 170 ºC for 1 min and 90 ºC for 5 min twice. The resist thickness was about 600 ~ 800 nm. The pattern of the Ohmic electrodes were written

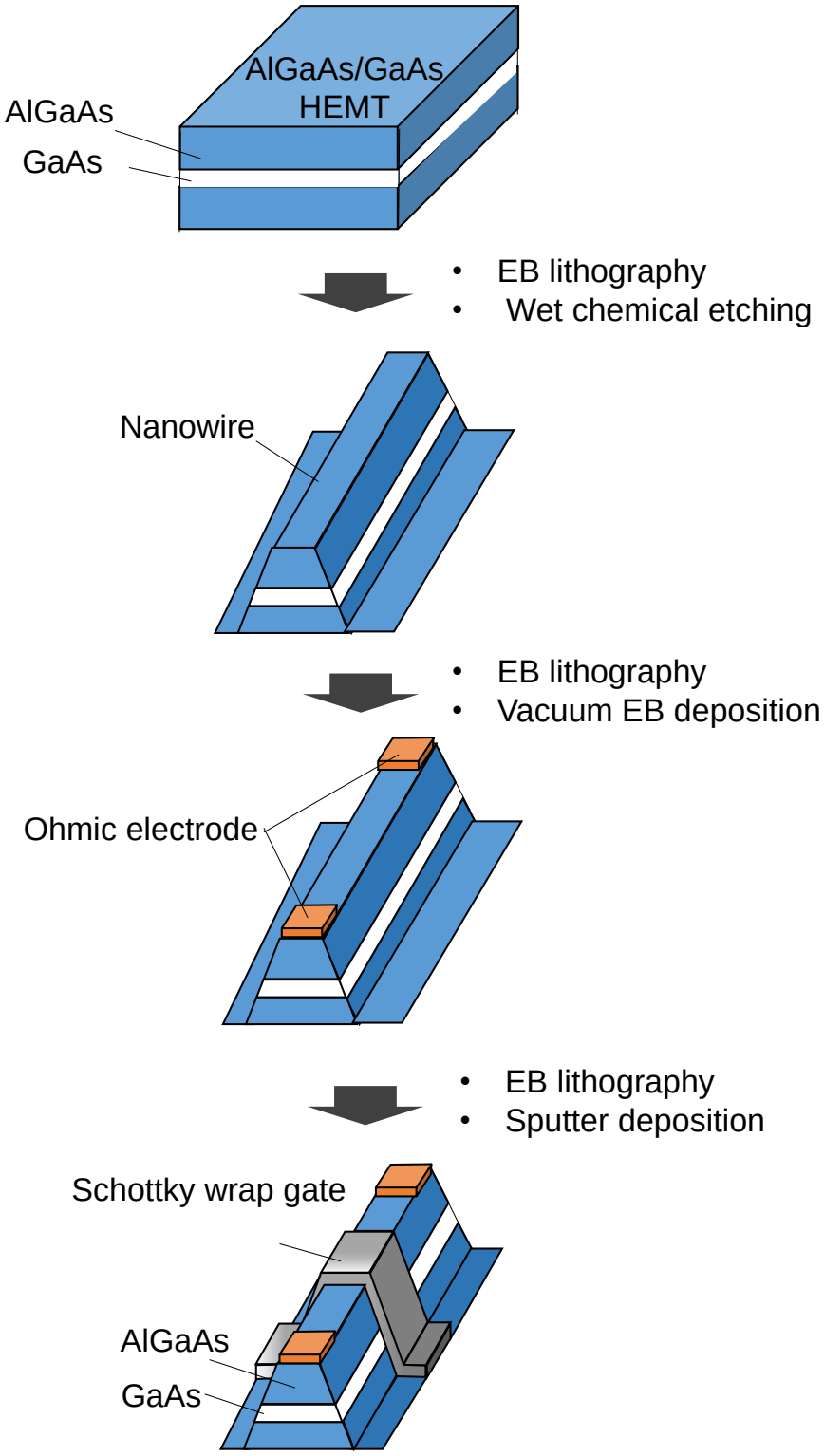


Fig. 3-2. The nanowire FET fabrication process flow.

by the EB writer. After exposure and development, the chip was dipped in 3% HCl solution (HCl:$H_2O$ = 3:97) for 30 s at room temperature in order to remove

the native GaAs oxide of the surface in the mask opened area. The post-baking was not carried out to avoid the deforming of the resist. For the Ohmic electrodes, Ni/Ge/Au/Ni/Au metal layers were deposited by electron beam deposition at 1.0 x $10^{-5}$ Torr. The thickness of each layer was 50, 500, 1000, 350, and 250 Å, respectively. Then the lift-off process was carried out by dipping the chip in the resist remover ZDMAC. The Ohmic electrodes were alloyed at 450 ºC for 5 min in $N_2$ ambient. For the gate of the nanowire FET, the Schottky wrap gate was formed. The EB resist of ZEP520A was coated on the chip and was pre-baked at 170 ºC for 1 min and 90 ºC for 5 min. The Schottky wrap gate patterns were exposed by EB writer. The resist patterns were developed by ZED-N50 and then the Schottky gate metal was deposited by the sputter deposition in Ar ambient. The gate metal was PtPd. The thickness of the PtPd was 10 nm. The fabricated nanowire network without wrap gate was conductive because the AlGaAs/GaAs wafer channel was degenerated. A scanning electron microscope (SEM) image of a fabricated GaAs-based nanowire FET is shown Fig. 3-3(b). The smooth etched surface and sidewalls were obtained.

## 3.4 Electron transport and its gate control

In this subsection the carrier transport in the nanowire FET and characteristics of the fabricated devices are shown. The band diagram of AlGaAs/GaAs HEMT structure is shown in Fig. 3-1 where $\Phi_B$, $d_1$, $d_2$, $E_F$, and $\Delta E_C$ are a Schottky barrier height, the thickness of AlGaAs barrier layer,

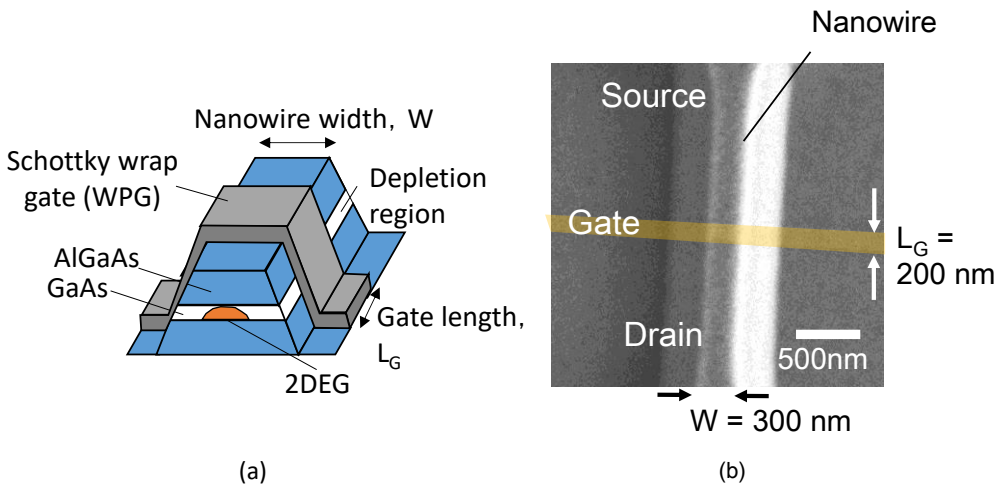


Fig. 3-3. (a) A schematic of nanowire FET and (b) top-view SEM of a fabricated GaAs nanowire FET.

thickness of AlGaAs space layer, Fermi energy in heterointerface, and a conduction band offset between AlGaAs and GaAs, respectively. A static potential in the AlGaAs layer, $V(y)$, is deduced from the following Poisson equation,

$$\frac{d^2V(y)}{dy^2} = -\frac{qN(y)}{\epsilon_{AlGaAs}} \tag{3.1}$$

where, $N(y)$ is the donor density distribution in the AlGaAs layer in depth direction, $y$, and $\varepsilon_{\mathrm{AlGaAs}}$ is the electric permittivity of AlGaAs. The difference of the conduction band potential in the depth direction of AlGaAs, $V_2$ which is referred in Fig. 3-1 is given by integration of Eq. (3.1).

$$V_2 = F_s \cdot (d_1 + d_2) + \frac{qN_d d_2}{\varepsilon_{AlGaAs}} \tag{3.2}$$

where $F_S$ is the electric field of heterointerface, and $N_d$ is the sheet density of the donor. The relationship between $F_S$ and density of two dimensional electron gas (2DEG), $n_s$, is the given by Gauss theorem

$$\mathrm{q}n_s = \varepsilon_{AlGaAs}F_s\,. \tag{3.3}$$

After substituting *Fs* in Eq. (3.3) into Eq. (3.2), the equation becomes,

$$n_s = \frac{\varepsilon_{AlGaAs}}{q(d_1 + d_2 + \Delta d)}(V_G - V_{th}), \tag{3.4}$$

where $V_{th}$ is threshold voltage given by

$$V_{th} = \Phi_B - \Delta E_C - E_{F0} - \frac{qN_d d_2}{\varepsilon_{AlGaAs}}, \tag{3.5}$$

and $\Delta d$ is effective thickness of the 2DEG layer as shown in Fig.3-1, and $E_{F0}$ is Fermi level from conduction band at $V_G = 0$ V.

The 2DEG channel width was controlled by gate voltage from side-gates in Schottky wrap-gate controlled nanowire transistor as shown in Fig. 3-3(a). By the ideal in-plane gate structure [15], the width of the depletion region, $W_{dep}$, is given by

$$W_{dep} = \frac{2\varepsilon_{AlGaAs}}{qn_s}(V_{bi} - V_G), \tag{3.6}$$

where, $V_{bi}$ is built-in potential of the Schottky contact. The effective channel width is determined by

$$W_{eff} = W_{geo} - 2W_{dep}, \tag{3.7}$$

where $W_{geo}$ is the geometrical nanowire width. The effective channel width is linearly changed with the gate voltage. The effective threshold voltage of the wrap gate structure, $V_{th,WPG}$, is defined as the gate voltage when $W_{eff} = 0$. $V_{thWPG}$ is derived from Eqs. (3.6) and (3.7) as

$$V_{thWPG} = V_{bi} - \frac{qn_s}{4\varepsilon_{AlGaAs}}W_{geo}. \tag{3.8}$$

Substituting Eq. (3.4) into Eq. (3.6), $V_{thWPG}$ is rewritten as

$$V_{thWPG} = \frac{1}{1+\alpha}V_{bi} + \frac{\alpha}{1+\alpha}V_{th}, \tag{3.9}$$

where $\alpha$ is the relation between geometrical wire width and the AlGaAs

barrier layer, and given by

$$\alpha = \frac{W}{4d}. \tag{3.10}$$

The theoretical threshold voltage given by Eq. (3.9) is varied by width of the nanowire. In the wrap gate devices, $V_{th}$ strongly depends on $W_{geo}$, and $V_{th}$ increased with decreasing of $W_{geo}$. From Eq. (3.10), $V_{th}$ changes more rapidly when $W_{geo} < 4d$. Therefore the precise control of the nanowire width is crucial for achieving the uniformity of $V_{th}$. Figure 3-4 shows the nanowire width dependence of the threshold voltage in the nanowire FET, where $\Phi_B = 0.8$ eV, $d_2 = 50$ nm, $\Delta d = 8$ nm, $d = 70$ nm, $N_d = 3 \times 10^{12}$ cm$^{-2}$, respectively. When the nanowire width is less than 200 nm, the threshold voltage is quickly changed by changing the nanowire width.

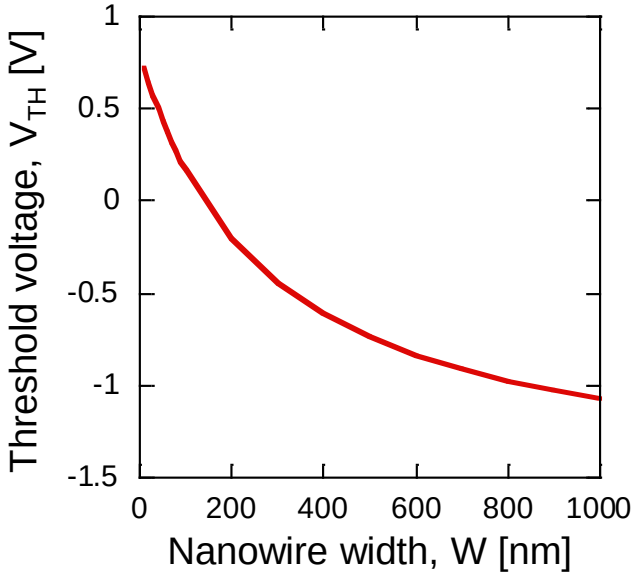


Fig. 3-4. Threshold voltage depending on nanowire width.

The drain current, $I_D$, in the Schottky wrap gate nanowire FET is similarly described with the drain current of HEMT device. $I_D$ of the HEMT is analyzed using the gradual channel approximation [16]. The sheet carrier

density of 2DEG and channel voltage are $n_s(x)$ and $V(x)$, respectively. $V(x)$ in the linear region is given by,

$$V_{eff}(x) = V_G - V_C(x). \tag{3.11}$$

And Eq. (3.4) must be rewritten as

$$Q_s(x) = qn_s(x) = \frac{\varepsilon_{AlGaAs}}{(d + \Delta d)}\{V_G - V_c(x) - V_{tj}\}. \tag{3.12}$$

The channel current $I$ at position $x$ is

$$I = Q_s(x)W_{eff}\upsilon(x). \tag{3.13}$$

Where $\nu(x)$ is the electron velocity at $x$. The electron velocity is limited by the phonon scattering and inter-valley electron scattering. To simplify the model, next two condition are used. When the electric field is small, the electron velocity increases linearly. When the electric field reaches the critical field, $F_C$, the velocity saturates at a constant value. To simply express the electric field dependence of the velocity, I use the equations as following,

$$\upsilon = \mu F, for\ F < F_c$$

$$\upsilon = \upsilon_s, for\ F \geq F_c \tag{3.15}$$

which is well known form for the conventional FET [17]. Then I can obtain an analytical form of the drain current. This approximation is phenomenological and does not care about the dominant scattering mechanism. When the field is smaller than $Fc$, the current, $I$, is given by

$$I = \mu W_{eff}\frac{\varepsilon_{AlGaAs}}{d + \Delta d}\{V_G - V_c(x) - V_{th}\}\frac{dV_c}{dx} \tag{3.16}$$

where $dV_c/dx = F$ is the electrical field between gate edge of a source and a drain. Considering the current continuity and the increase of the channel voltage $Vc(x)$ from source to drain, the electrical field is maximum close to the

drain and the velocity saturation will occur first at the drain side of the gate region. First, in the case of very small drain voltage, $V_D$, which means linear regions of the $I_D$- $V_D$ characteristics, the current is expressed as follows from Eq. (3.16),

$$I = W_{eff}\frac{\varepsilon_{AlGaAs}}{d+\Delta d}\{V_G - V_c(x) - V_{th}\}\frac{V_C(L_G) - V_c(0)}{L_G}. \quad (3.17)$$

$Vc$ does not correspond to the applied source and a drain voltage because of the voltage drops owing to the source and drain parasitic resistances, $R_S$ and $R_D$. The parasitic resistance is mainly determined by the channel resistance of the nanowire in the access region, $R_{NW}$, and the contact resistances of source and drain electrodes, $R_C$. The nanowire resistance in the access region, $R_{NW}$, is expressed by

$$R_{NW} = \frac{1}{en_s\mu}\frac{L_{NW}}{W_{eff}}, \quad (3.18)$$

where, $L_{NW}$ is the nanowire length of the access region. $V_C$ including the effect of $R_S$ and $R_D$ are following.

$$V_C(0) = R_S I. \quad (3.19)$$

$$V_C(L_G) = V_D - R_D I. \quad (3.20)$$

Then, from Eqs. (3.17)-(3.19), drain current in the linear region is given by

$$I_{D\ linear} = \left[R_s + R_D + \frac{L_G(d+\Delta d)}{\mu\varepsilon W_{eff}}\right]^{-1} V_D. \quad (3.21)$$

At drain voltage such that the drain side electric field is less than $F_C$, the integration of Eq. (3.16) gives

$$V_C(x) = V_G - V_{th} - \sqrt{\left(V_G - V_{th} - V_C(0)\right)^2 - \frac{2(d+\Delta d)Ix}{\mu\varepsilon W_{eff}}}. \quad (3.22)$$

The electrical field at $x$, $F(x) = dV_C/dx$, is easily obtained. Substituting the

field in Eq. (3.22) by the critical field value

$$F(\mathrm{L}) = F_C. \tag{3.23}$$

Then the saturated current expression is obtained as

$$I_{Dsat} = \frac{\mu\varepsilon W_{eff}}{d+\Delta d}\left[\sqrt{(V_G - V_{th} - R_S I_{DSat})^2 + F_C^2 L_G^2} - F_C L_G\right]. \tag{3.24}$$

For a long gate HEMT, Eq. (3.23) is reduced to

$$I_{Dsat} = \frac{\mu\varepsilon W_{eff}}{2(d+\Delta d)L_G}(V_G - V_{th} - R_S I_{Dsat})^2 \tag{3.25}$$

And for a short gate HEMT, the $I_{Dsat}$ depends on the gate voltage linearly,

$$I_{Dsat} = \frac{\varepsilon W_{eff}\upsilon_s}{d+\Delta d}(V_G - V_{th} - R_S I_{Dsat} - F_C L_G). \tag{3.26}$$

For $V_G$-$V_{th}$-$R_S I_S$ >> $E_C$L, the expression is valid as

$$I_{Dsat} = \frac{K}{1+KR_S}(V_G - V_{th} - F_C L_G), \tag{3.27}$$

where $K$ is the coefficient,

$$\mathrm{K} = \frac{\varepsilon W_{eff}\upsilon_s}{d+\Delta d}. \tag{3.28}$$

The $I_D$-$V_G$ and $I_D$-$V_D$ characteristics of the fabricated GaAs nanowire FET are shown in Fig. 3-5. The measurement of the current – voltage characteristics were carried out using Agilent B1500A Semiconductor Device Analyzer. The fabricated nanowire width was 300 nm and the gate length was 250 nm. The obtained characteristics showed that the fabricated device operated as a conventional FET. From the $I_D$-$V_G$ characteristics the transconductance, $g_m$, of the fabricated nanowire FET was 45 μS and

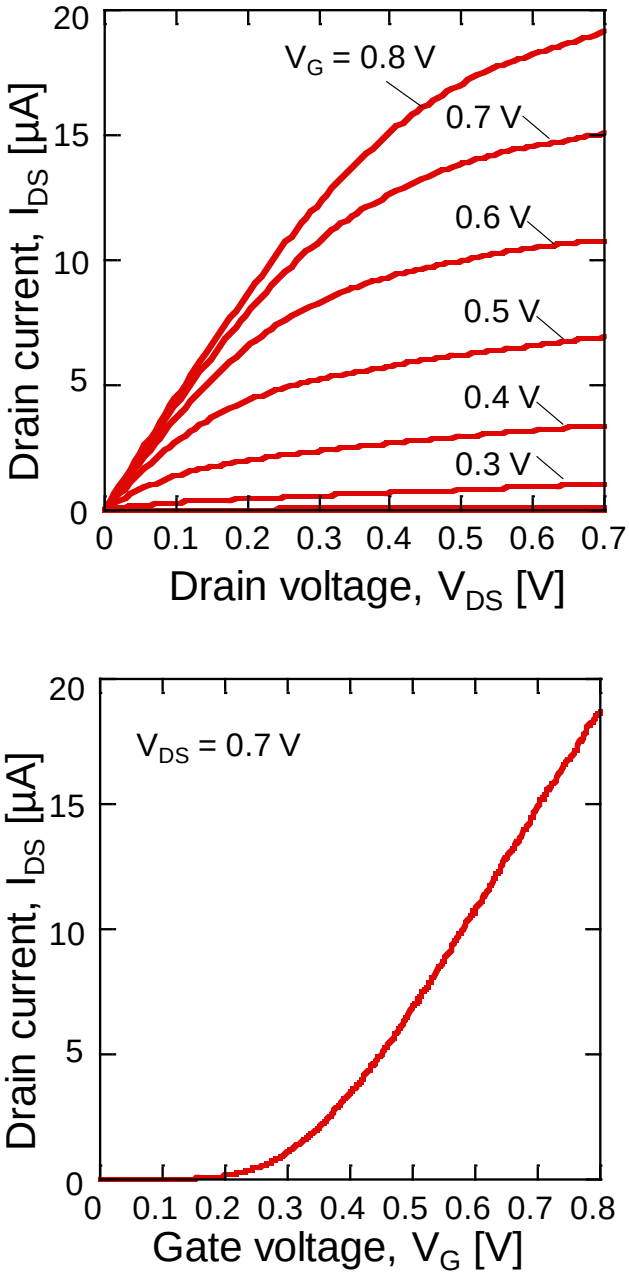


Fig. 3-5. Measured characteristics of a fabricated nanowire FET.

threshold voltage was 0.3 V. Because of nanowire structure and wrap Schottky gate, the nanowire FET has this positive threshold voltage. The positive threshold voltage is necessary for the inverter which has a positive

threshold value. From these results, the nanowire FET could be used to implement of the threshold logic circuit designed in this study.

## 3.5 Summary

In this chapter I described the basic property of GaAs and the fabrication process of the GaAs-based nanowire FET. Then I described the transport property of the nanowire FET and *I-V* characteristics of the fabricated GaAs-based nanowire FET. The *I-V* characteristics of the fabricated nanowire FET confirmed that it operated as a conventional FET. It was found that the GaAs-based nanowire FET could be applied to implement of the threshold logic circuit. By integrating the nanowire FET on a nanowire network, the threshold logic circuit is expected to be implemented using a nanowire network.

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# Chapter 4
# Threshold Logic Circuit on GaAs-based Nanowire Network

## 4.1 Introduction

Recently demand for an information processing that efficiently solves optimization problems is increasing. To solve the optimization problem, usually the solution search is necessary, where the von Neumann computer [1] takes extremely long time to find the solution. A quantum computing system is known as one of the powerful computers for solving such optimization problems. This system efficiently solves the problem using the quantum parallelism. However, it is unclear where the quantum computer can solve the NP complete problem, which is a very important one in the computationally intractable problems, and it is found unrealistic to realize the quantum computing hardware because of so many technological difficulties. Considering the rapid growth of the information, communication technologies, now realistic logic architecture and hardware implementation are strongly required. For hardware implementation, III-V compound semiconductor nanostructure is

attractive, since this offers rich functions with excellent carrier confinement and transport as well as sophisticated nanofabrication technologies. In this chapter, the threshold logic [2,3] is employed as an alternative logic architecture instead of the conventional Si CMOS architecture. The threshold logic is implemented using the GaAs nanowire network in which the nanowire FETs are integrated systematically on a nanowire network. I demonstrate the two inputs threshold logic circuit which is the basic concept of threshold logic circuit. The nanowire is also used as interconnection between FETs so that integrated circuit is composed using only the GaAs nanowire and nanowire FETs.

In this section, first I will explain the circuit design of integrated threshold logic using the GaAs nanowire. And then I will explain about experimental scheme and conditions, results, and then I will summarize this study.

## 4.2 Circuit design

We designed the two-input threshold logic circuit including summation circuit and threshold function circuit as mentioned in chapter 2. The diagram of designed threshold logic circuit is shown in Fig. 4-1. To avoid the increasing the FET numbers, the circuit was a simple composition. Only 5 FETs were integrated. The summation circuit was composed by two diode-connected FETs for input and one load FET for converting the current signal

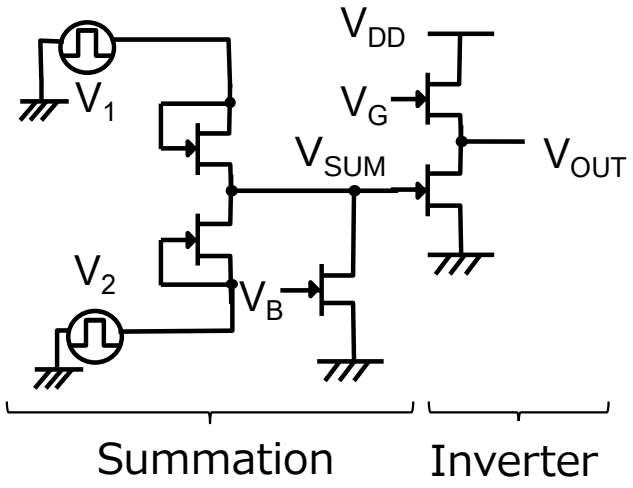



Fig. 4-1. The diagram of two-input threshold logic circuit.

to voltage signal. Input currents were summed up at the node on the basis of Kirchhoff's laws. The threshold function was designed by an inverter circuit with two FETs. The threshold value of this threshold function was determined by gate threshold voltage of driver FET.

In the input summation circuit, the converted voltage from summed current, $V_{SUM}$, is defined by Eq. (4.1) and Eq. (4.2), where $I$ is the current of current-to-voltage load FET. In this situation, this FET is operated under saturation current area. When the one input FET is ON, the $V_{SUM}$ becomes Eq. (4.1). When the two input FETs are ON, the $V_{SUM}$ becomes Eq. (4.2). From these equations, the $V_{SUM}$ is dependent on square root of reverse of input numbers. That's why the $V_{SUM}$ is changed in nonlinear.

$$V_{sum} = V_{IN} - V_{th} - \sqrt{\frac{2I}{\beta}}, \tag{4.1}$$

$$V_{sum} = V_{IN} - V_{th} - \sqrt{\frac{I}{\beta}}, \tag{4.2}$$

$$\beta = \frac{W}{L}\mu C, \tag{4.3}$$

where $W$ is the nanowire width of input nanowire FET, $L$ is the gate length of input nanowire FET, $\mu$ is the mobility of AlGaAs/GaAs HEMT, and $C$ is the gate capacitance of nanowire FET.

## 4.3 Experimental

The GaAs nanowire network was fabricated by the same process of nanowire FET as mentioned previous section. All FETs were fabricated by GaAs nanowire formed by EB lithography and wet chemical etching of AlGaAs/GaAs HEMT wafer. All FETs are the n-channel type because AlGaAs/GaAs HEMT has electron carriers. Therefore, the inverter was

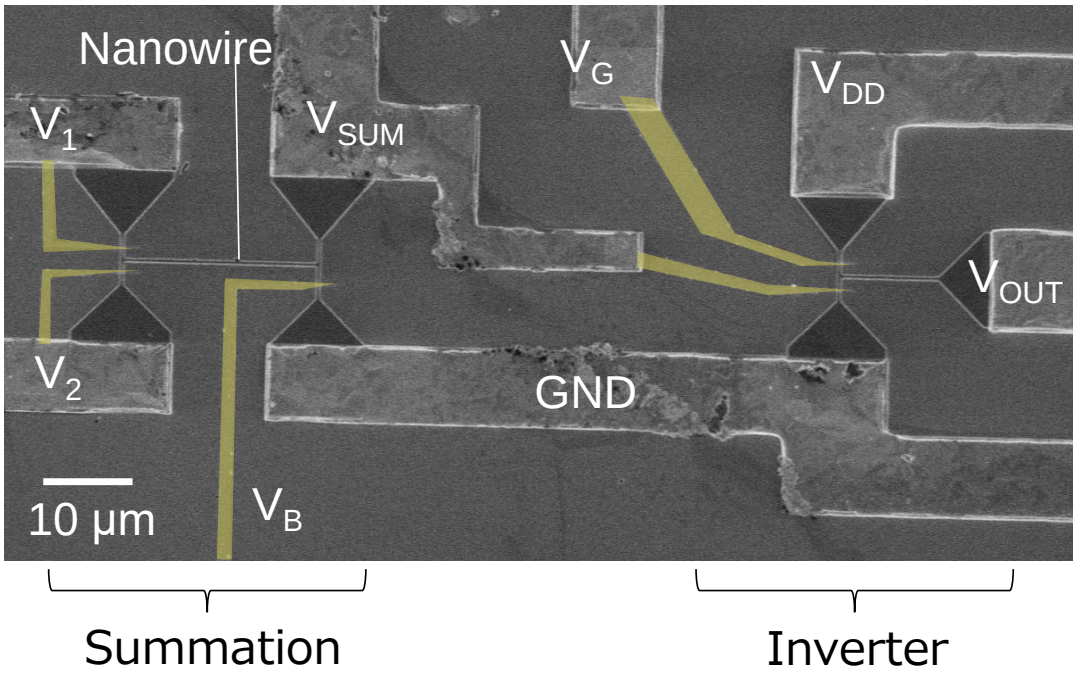



Fig. 4-2. The SEM image of a fabricated circuit.

composed only n-type FETs. The SEM image of fabricated integrated-threshold logic circuit is shown in Fig. 4-2. The gate of FET was all Schottky wrap gate structure. All FETs were monolithically integrated on a chip and wired FET-to-FET by <01-1> and <011> direction nanowire. The nanowire width were 200 nm and gate length were 250 nm.

The operation of the fabricated two-input threshold logic circuit was demonstrated with the supply voltage, $V_{DD}$, of 0.3 V, the FET gate voltage for current-to-voltage conversion, $V_B$, of 0.2 V or 0.42 V, and the gate voltage for the load FET in the inverter, $V_G$, of 0.3 V. The voltage swing of the input signals was 0.9 V and the frequency was 100 Hz. The threshold voltage was around 0.2 V. The experiments were carried out at room temperature.

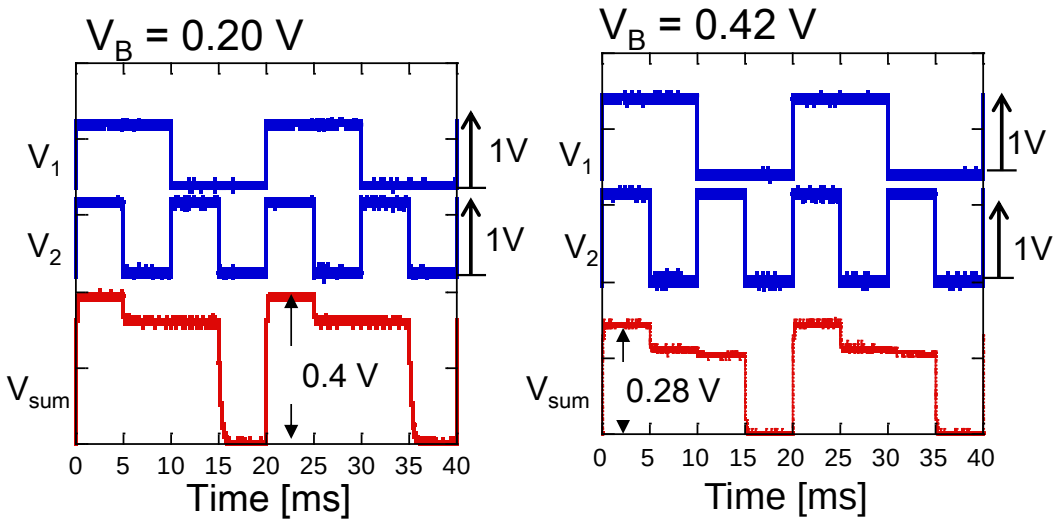
## 4.4 Results and discussion

### 4.4.1 Summation and inverter elements

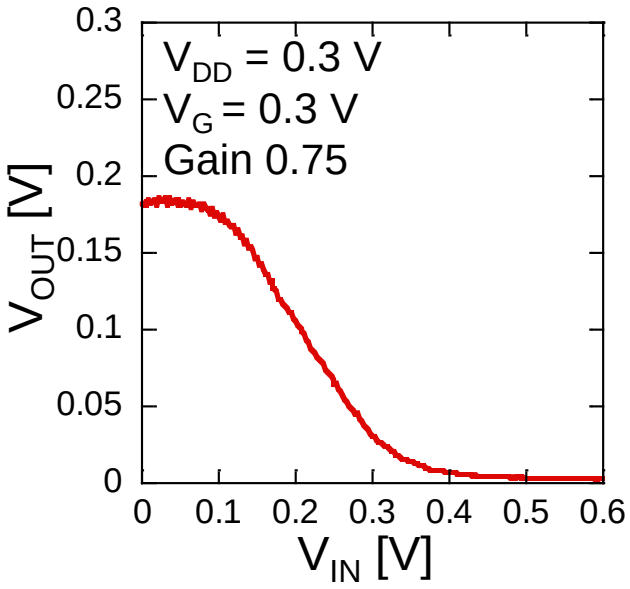
First the results of summation elements and the inverter element are shown in Fig. 4-3. Figure 4-3(a) shows the measured waveforms of the summed signals in the case of $V_B$ = 0.20 V and 0.42 V, respectively. The waveforms of summation indicated the three level corresponded to each inputs. They were not exactly proportional to the inputs, because the FET for the current-to-voltage conversion pulled up the drain potential of the FETs for the voltage-current conversion in the input stage. The highest voltage

level of summation was 0.3 V for $V_B$ of 0.42 V and 0.28 V for $V_B$ of 0.2 V. The output voltage was decreased approximately 30% by increasing $V_B$.

The transfer curve of fabricated inverter is shown in Fig.4-3(b). The $V_{DD}$ voltage was 0.3 V and gate voltage of load FET was 0.2 V. The differential




(a)




(b)

Fig. 4-3. (a)The input-output waveforms of the summation elements and (b) transfer curve of the fabricated inverter.

gain of this inverter was about 0.75. The threshold value of this inverter was around 0.2 V. The output voltage of inverter gave high level when the input voltage of inverter was less than 0.2 V. The low gain was due to low supply voltage. The result of summation was inputted into the gate of driver FET in the inverter. Because output of inverter was inverted the input signal, the expected outputs of this threshold logic circuit were NOR-gate and NAND-gate.

### 4.4.2 Threshold logic circuit

In this experiments, the input signal swing was 0.9 V and the gate voltage of current source FET was either 0.20 V or 0.42 V. $V_{DD}$ of inverter was 0.3 V and the gate voltage of load FET in the inverter was the 0.2 V. The input signal frequency was 100 Hz. The input-output waveforms of operating threshold logic circuit when $V_B$ = 0.20 V are shown in Fig. 4-4. The NOR gate operation was successfully demonstrated as the characteristics of the components in Fig. 4-3. However, the output voltage swing was as small as 0.1 V. This was because the signal amplitude was decreased in the summation device and the logic swing of the inverter output was insufficient.

The reconfiguration of Boolean logic gate in the threshold logic is desired. Though the logic function of the circuit could not be controlled by the

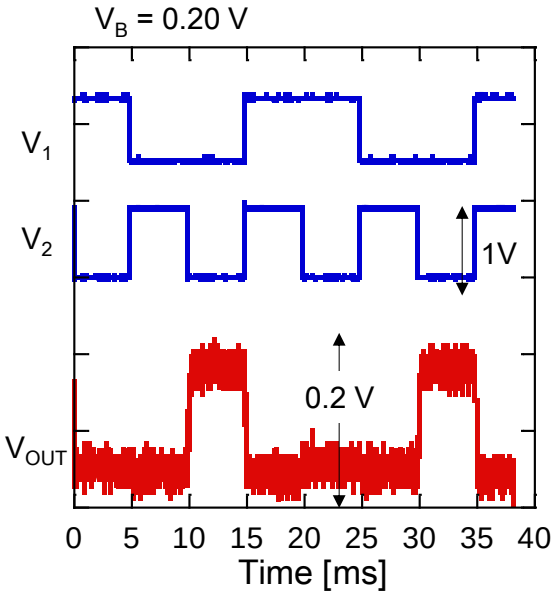



Fig. 4-4. Input-output waveforms of threshold logic circuit with $V_B = 0.20$ V.

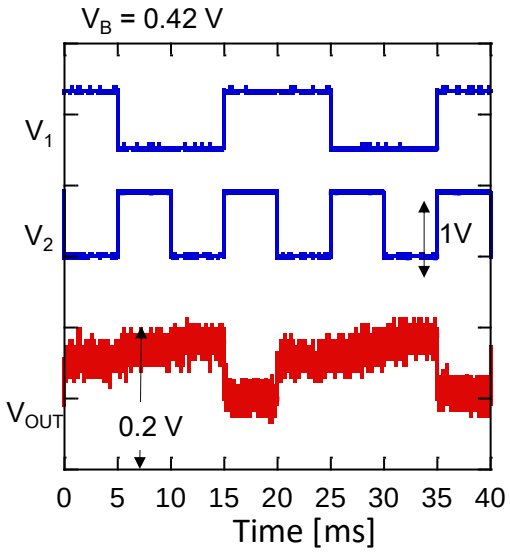



Fig. 4-5. Input-output waveforms of threshold logic circuit with $V_B = 0.42$ V.

fixed threshold of inverter due to fixed threshold voltage of a driver FET, another approach was taken as tuning the output level of summation circuit. The output level of summation circuit was depended on the gate-controlled conductance of *I*-to-*V* converter load FET. When its gate voltage was 0.42 V,

the input-output waveforms of threshold logic circuit showed the NAND gate operation as shown in Fig. 4-5. Therefore the possibility of reconfiguring the logic gate was demonstrated.

For input the output voltage into the next gate in this threshold logic circuit, it needs to increase the output voltage. The solutions are increasing the $V_{DD}$ voltage and improving the inverter gain. The inverter gain become following equation because the current flowing through load FET and driver FET is equal.

$$\frac{\partial V_{OUT}}{\partial V_{IN}} = \sqrt{\frac{\beta_{driver}}{\beta_{load}}} = \sqrt{\frac{W_{driver}/L_{driver}}{W_{load}/L_{load}}} \tag{4.4}$$

From above equation, it just have to adjust the device size ratio of the nanowire FET composing the inverter. To improve the inverter gain, it needs to design the optimal nanowire width and gate length and fabricate the nanowire structure precisely.

## 4.5 Summary

In this chapter I described the threshold logic circuit composed by GaAs nanowire FETs. First the summation circuit and the inverter, which play key role in the threshold logic, were characterized separately. Then, the logic gate operations of NOR and NAND were demonstrated by the fabricated threshold logic circuit. In this chapter, even though the function of fabricated threshold logic circuit could not be control by the threshold value of inverter

as a threshold function, through an alternative approach of changing the circuit parameter, the reconfiguration of threshold logic circuit was accomplished. I expect that the flexibility of threshold logic can be demonstrated if the threshold value of inverter can be shifted dynamically.

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# Chapter 5
# Electrical Reconfiguration of Threshold Logic Circuit

## 5.1 Introduction

The threshold logic circuit can change its logic function by shifting the threshold value in the element [1,2], as shown in previous section. However, the reconfiguration in the previous section was carried out statically. Usually the threshold voltage defining the logic function cannot be changed in the fabricated chip. Dynamic reconfiguration of the logic function gives more flexibility to the circuit and the system, and is expected to provide more efficient operation resulting in shorter time processing and low power consumption. To achieve the dynamic reconfigurability of the threshold logic circuit, it is necessary to shift the threshold voltage of the inverter which works as a threshold function in an element even after the circuit fabrication.

In this section, I propose the implementation of the dynamic threshold control capability in the inverter circuit by integrating the nanowire FET having a charge memory in the gate.

## 5.2 Concept and design

To shift the threshold value of threshold function, it needs to shift the threshold voltage of the inverter as a threshold function. The threshold voltage of inverter is depended on threshold voltage in the driver FET. When the switching from high level to low level in the transfer curve of inverter, the flowing current is same at load FET and driver FET. From that current relationship, the threshold voltage of inverter is given by

$$V_{INV} = \frac{V_{DD} - V_{T,load} + \left(1 + \sqrt{\frac{\beta_{driver}}{\beta_{load}}}\right) V_{T,driver}}{1 + \sqrt{\frac{\beta_{driver}}{\beta_{load}}}}, \tag{5.1}$$

$$\beta_{drive} = \frac{W_{driver}}{L_{driver}} \mu C_{driver}, \tag{5.2}$$

$$\beta_{load} = \frac{W_{load}}{L_{load}} \mu C_{load}, \tag{5.3}$$

where $V_{INV}$ is the threshold voltage of inverter, $V_{DD}$ is the supply voltage, $V_{T,\ load}$ is the threshold voltage of a load FET, $V_{T,\ driver}$ is the threshold voltage of a driver FET. And $W_{driver}$ and $W_{load}$ are the nanowire width of driver FET and load FET, respectively. $L_{driver}$ and $L_{load}$ are the wrap gate length of driver FET and load FET, respectively. $\mu$ is the carrier mobility. $C_{driver}$ and $C_{load}$ are gate capacitance of driver FET and load FET, respectively. From Eq. (5.1) the

threshold value of inverter can be shifted by changing the threshold voltage of a driver FET.

For post-fabrication controlling the threshold voltage of inverter, thin film insulator is inserted between the gate metal and the nanowire in the driver FET. By inserting the insulator film between the AlGaAs/GaAs nanowire surface and the gate electrode, the interface traps which can charge/discharge the electrons are generated [3,4]. When the electrons are captured in interface traps between insulator and AlGaAs surface, the channel is depleted as shown Fig. 5-1. The electrons are trapped by gate

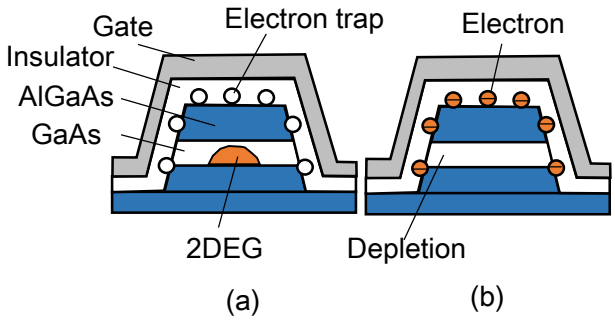


Fig. 5-1. Schematic of (a) discharged the electrons from trap and (b) charged the electrons to trap.

voltage of Metal-insulator-semiconductor (MIS) gate FET. Thus the threshold voltage shifts to positively. Here as the insulator, SiN film and $Al_2O_3$ film are used. The SiN film is known as an electron-trapping layer in the non-volatile memory devices [5-7]. $Al_2O_3$ film is known as good insulator which has a good connection between GaAs surface and $Al_2O_3$ [8]. Figure 5-2 shows the designed inverter composed by Schottky-gate FET as a load FET and MIS-gate FET as a driver FET.

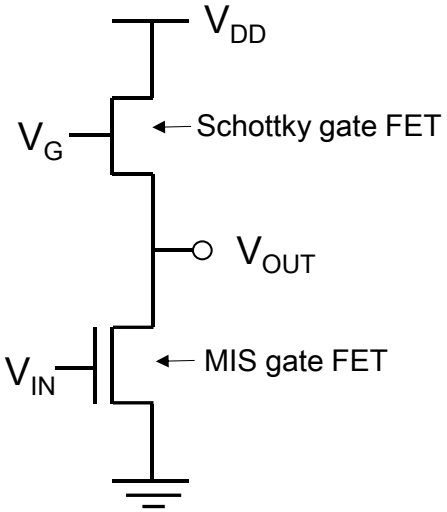


Fig. 5-2. The diagram of an inverter circuit using MIS-gate FET as a driver FET.

## 5.3 Experimental

After forming the nanowire by EB lithography, wet chemical etching and Ohmic electrode formation on AlGaAs/GaAs HEMT wafer, the insulator was deposited. The SiN film was deposited by electron cyclotron resonance chemical vapor deposition (ECR-CVD) on the GaAs nanowire at a substrate temperature of 260 ºC. The gas flow conditions of a SiN deposition were 30 sccm of silane ($SiH_4$) gas and 1 sccm of nitrogen ($N_2$) gas. The applying RF power was 100 W. The thickness of SiN was 10 nm from ellipsometry measurement. The $Al_2O_3$ film was deposited by atomic layer deposition at a substrate temperature of 300 ºC. The material gas were Trimethylaluminium (TMA) and $H_2O$. The thickness of $Al_2O_3$ film was 8 nm from an ellipsometry measurement. After insulator of SiN or $Al_2O_3$

deposition, a PtPd gate metal was deposited on insulator film. The gate patterns were exposed by EB writer. The fabrication process flow is shown in Fig. 5-3. First of all I characterized the $I_D$-$V_G$ hysteresis property of MIS-gate GaAs nanowire FETs. The hysteresis characteristics is appeared when the insulator trapped the electrons in interface traps between the nanowire and insulator.

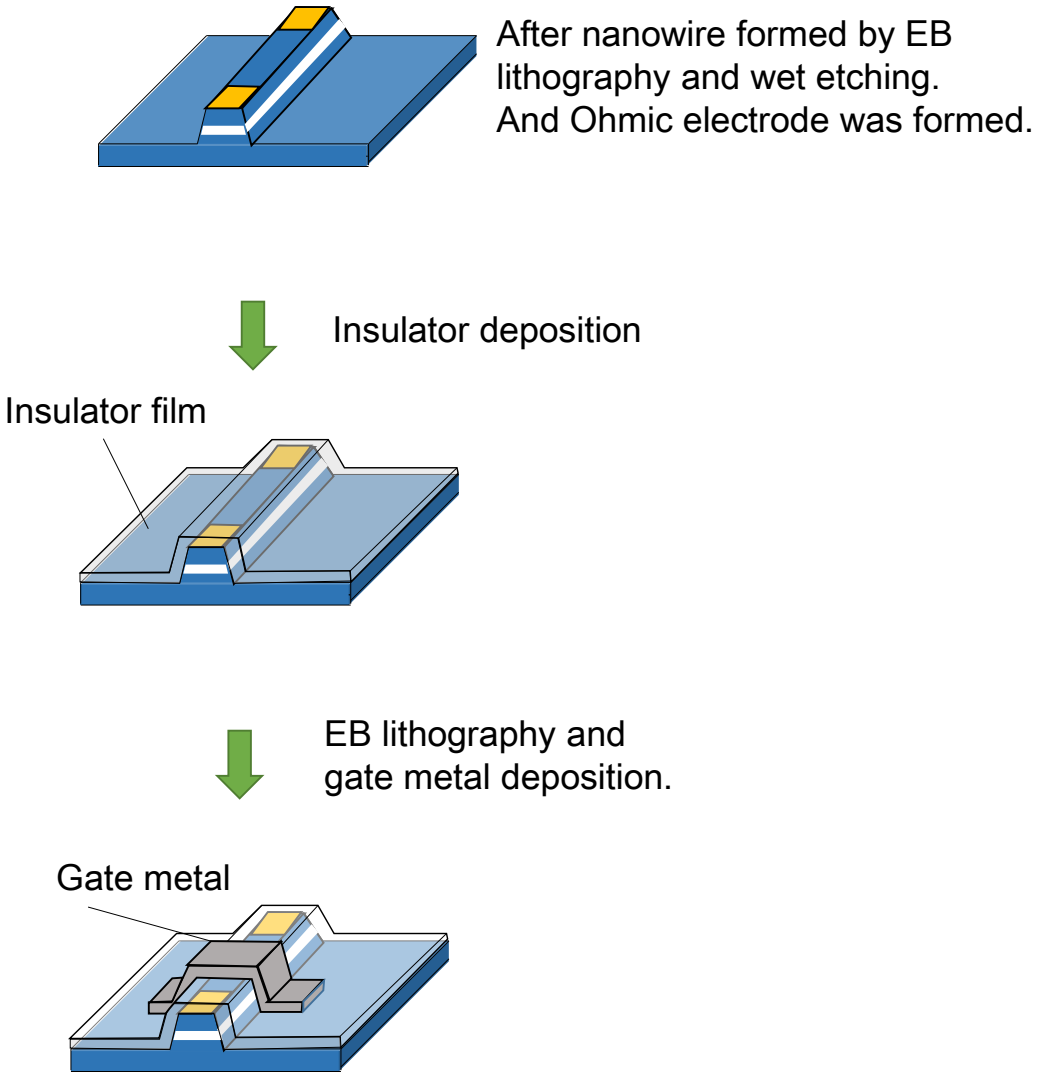


Fig. 5-3. Fabrication process of GaAs nanowire MISFET.

The emission time constant was estimated for SiN-gate and $Al_2O_3$-gate nanowire MISFET. By understanding the behavior of emission time constant, it is possible to determine which is suitable for MIS-gate inverter. The emission time constant was determined by $I_D$-time characteristics. The emission time constant estimated from the recovery time of the current after the gate voltage was set to 0 V immediately after 4 V or 2 V was applied to the gate for several time. The applied time of gate voltage of 4V or 2V was 1 ms, 10 ms, 100 ms, and 1000 ms.

Then the inverter composed by a Schottky nanowire FET for a load FET and MIS-gate nanowire FET for a driver FET was fabricated. By shifting the threshold voltage of driver FET, it is expected the threshold voltage of inverter is changed.

## 5.4 Results and discussion

### 5.4.1 GaAs nanowire MISFET

Figure 5-4 shows the $I_D$-$V_G$ characteristics of MIS-gate nanowire FET with SiN-gate and $Al_2O_3$-gate. In this measurement, the gate voltage was swept from -4 V to 4 V and then from 4 V to -4 V and the drain voltage is 500 mV. The hysteresis characteristics were obtained and the direction of hysteresis loop was clockwise in both MIS-gate nanowire FETs. The hysteresis width was 3.5 V in SiN-gate and 3.2 V in $Al_2O_3$-gate.

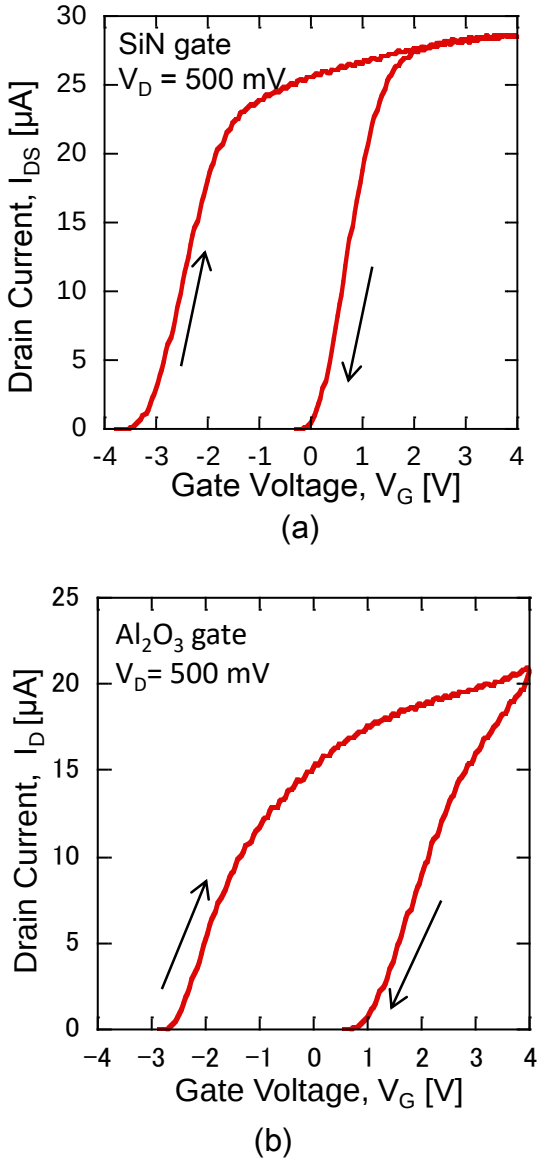


Fig. 5-4. $I_D$-$V_G$ characteristics of fabricated MIS-gate nanowire FET with (a) SiN-gate and (b) $Al_2O_3$-gate.

The emission time constant of MIS-gate nanowire FET was measured. Figure 5-5 shows the $I_D$-time characteristics and estimated electron emission time from interface traps. In the SiN film, the emission time constant decreased as the gate pulse time became shorter, but in the $Al_2O_3$ film, the emission time constant was constant even if the pulse time was shortened.

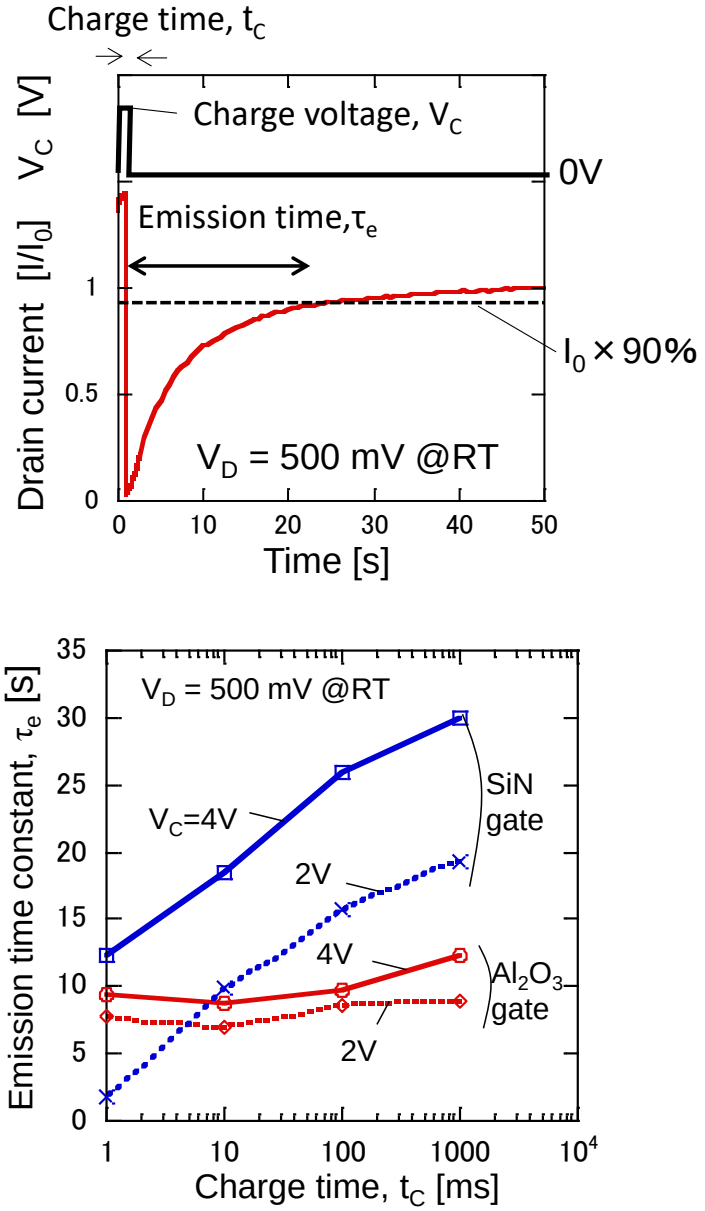


Fig. 5-5. The measured emission time constant from interface trap depending on charge time.

From these results, it could be seen that in the case of the SiN-gate, both the electron capture time constant to the trap and the handling time were long. In the case of $Al_2O_3$-gate, the capturing time constant was short, the electrons were charged in the traps in a short time, and the emission time constant was a constant value of about 10 s.

For MIS-gate inverter, the SiN-gate can control emission time constant with gate voltage and biasing time. In other words, the threshold voltage can be easily controlled through changing the number of trapped electrons. From this considering, the inverter characteristics using GaAs nanowire SiN-gate FET was fabricated.

### 5.4.2 Inverter characteristics using GaAs nanowire MISFET

Figure 5-6 shows the measured characteristic of the fabricated inverter in which the SiN-gate nanowire FET was used as a driver FET. First the $V_{IN}$ voltage swept from negative voltage to positive voltage. Afterwards holding the $V_{IN}$ voltage at 4 V for 10 s, the $V_{IN}$ voltage swept from positive

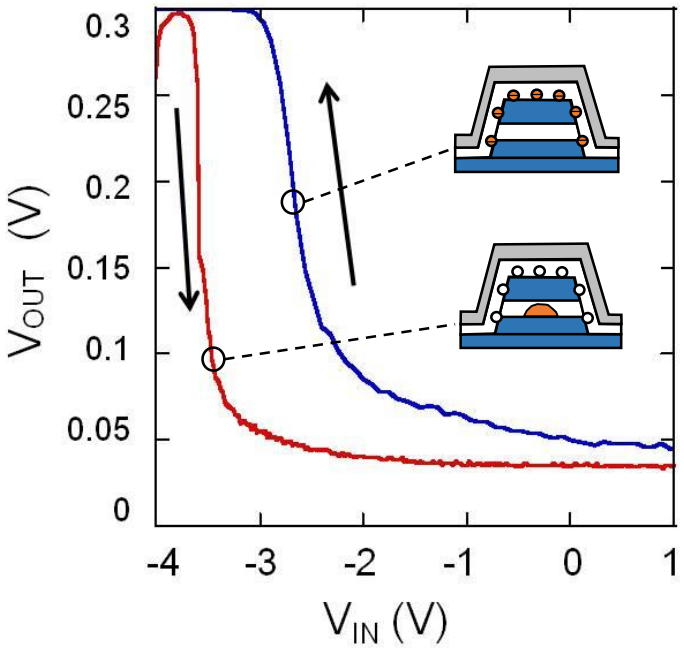


Fig. 5-6. Inverter characteristics using MIS-gate GaAs nanowire FET.

voltage to negative voltage. The transfer characteristics of inverter showed the double threshold voltages and the direction of the hysteresis was anticlockwise. By insertion the insulator, shifting threshold voltage of inverter was archived. This inverter enables shifting threshold value of threshold logic circuit. However fabricated inverter using MIS-gate had a deep negative threshold value. This deep threshold value cannot be used in the logic circuit because the logic signal is positive voltage. If this inverter with MIS-gate is used, the threshold value of inverter should be positive voltage. The causes of deep negative threshold value was the positive fixed charges in the insulator. A good quality insulator film is necessary for circuit application.

## 5.5 Summary

In this section, the concept of shifting the threshold value in the threshold logic and circuit design were explained. From the equation of threshold voltage of inverter, I proposed a threshold-controlled inverter using interface trap of GaAs MISFET. SiN-gate and $Al_2O_3$-gate GaAs nanowire FETs were fabricated and characterized focusing on the hysteresis characteristics and emission time constant. From those results, I fabricated the inverter using GaAs nanowire SiN-gate FET and characterized the inverter characteristics. The threshold shift by interface trap was confirmed but a deep negative threshold voltage was obtained. A deep negative threshold voltage shift was caused by the positive fixed charge in the

insulator. It is necessary to optimize the insulator formation process for reducing the fixed charge.

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# Chapter 6
# Computer-controlled GaAs Digital Wet Chemical Etching

## 6.1 Introduction

The etching technique is important in the semiconductor nanodevice fabrication. There are two etching techniques. One is the dry etching, which uses the gas, plasma, or radical and performs the etching in a vacuum chamber. It can achieve the nanoscale etching but causes damages on the semiconductor surface. The mechanism of the dry etching is to break the chemical bond in the sample surface by physical and/or chemical reactions. For nanodevices, the surface damage is a severe problem. In the case of Si, the damage can be removed by the high temperature annealing process and the material quality is recovered. However most of the compound semiconductors cannot be recovered by the annealing because of the difficulty in achieving both the crystallinity and stoichiometry at high temperature. For the III-V compound semiconductor, the dry etching is used for fabrication of the macroscopic device.

The wet chemical etching is a low damage process. In wet etching technique, the etching progresses breaking the chemical bond by the chemical reaction. However in this etching process it is difficult to precisely control the amount of etching and the etched structure, because fluctuation in etching time or etchant solution composition occurs due to manual operation and the side etching occurs. From the viewpoint of the nanostructure formation, size variation less than 10 nm both in depth and lateral directions is strongly required to obtain uniformity and reproducibility of the device characteristics. Thus, for the nanostructure formation of the III-V compound semiconductor, the high precision etching technique is still under development, for example, such as digital wet chemical etching [1-3], the neutral beam etching [4-9], and metal-assisted chemical etching [10]. In this chapter, in order to realize damage-free high precision etching technique for the III-V compound semiconductors, I investigate the digital wet etching technique using a computer-controlled wet etching machine. First I develop the etching machine which makes it possible to control the etching process precisely by spraying the solutions in sub second under the computer control. Namely the amount of the etching is controlled by spraying time and the number of spraying cycle. Here I examine the etching using $H_2SO_4$-based etchant. This etchant is often used in GaAs wet etching to achieve the steep and smooth sidewall of 55° angle for <01-1> direction on (100) GaAs substrate. However the etching rate is quite high over 100 nm/s and it is very difficult to obtain the etched structure having the designed size reproducibly.

## 6.2 Digital wet chemical etching technique

To improve the fluctuation of wet chemical etching, the digital wet etching machine was developed. The etching concept of the system is spraying the $H_2SO_4$-based etchant and the rinse solution alternately. By repeating that process, the etching depth is controlled. All etching sequence is done by automatically without any fluctuation in manual process. The digital etching of dry etching has been studied before [11]. However the digital dry etching was not practical because introducing the etching damage and large scale equipment were required. On the other hand automatization of wet etching was considered to be difficult [1], and there were few studies on automation of wet etching.

## 6.3 Computer-controlled wet etching machine

Figure 6-1 shows the schematic of developed digital wet etching machine. The size of developed machine was desktop size. The developed

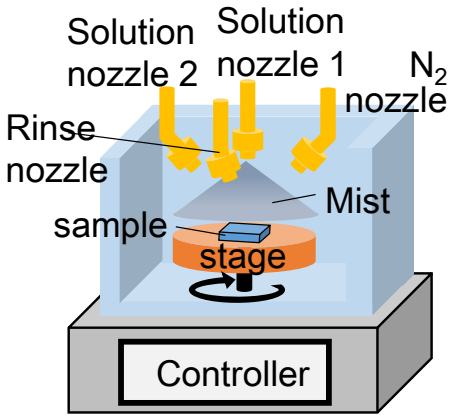


Fig. 6-1. Schematic of developed etching machine.

machine consists of two solution tanks, four solenoid spray nozzles, a rotatable stage, a chemical resistance chamber, and a digital computer. The solutions are sprayed from nozzles. The spray time is control by digital computer which has 0.1 seconds resolution. The digital computer can also control the etching sequence, spray timing, rotation speed of stage, and cycle number. Spray pressure is controlled by adding additional pressure of dry $N_2$ gas into tank. The compressed air is used for solution valve ON/OFF control. In this study the dry $N_2$ gas of 0.3 MPa was used as a compressed air. The spray pressure of solution and dry $N_2$ gas were 0.1 MPa and 0.2 MPa, respectively.

## 6.4 Experimental and results

### 6.4.1 Etching sequence

The substrate in etching experiments was (100) AlGaAs/GaAs HEMT wafer. As a mask, the photolithography resist SPR6810 was used. The AlGaAs/GaAs HEMT wafers cleaved in the area of 7 x 4 $mm^2$. After cleaning by acetone, ethanol, and deionized water in ultrasonic for 5 min respectively, the wafers was dried at 140 $^oC$ for 10 min. Before coating the SPR6810, primer was coated to improve the adhesion between the resist and the sample. The resist and primer coated by spin coater in 500 rpm for 3 s and 5000 rpm for 30 s. The prebake was carried out for 5 minute at 90 $^oC$ in oven. The exposure time was 6 s in photolithography. The development and rinse were carried out by CD-26 and deionized water, respectively. The development time was

30 s and rinse time was 30 s. The post bake was carried out for 10 minute at 110 °C in oven to improve the etching resistance of resist. The mask pattern was the line and space with half pitch of 2, 5, and 10 μm. The line directions were <01-1> and <011> direction. The resist thickness was about 1 μm. The etching sequence is shown in Table 6-1. In this experiment, three kind etchants were used. The etchant ratio of $H_2SO_4$:$H_2O_2$:$H_2O$ were 1:1:1, 1:0.2:1, and 1:1:10, hereafter they are referred as etchant A, B, and C, respectively. Increasing with the ratio of $H_2SO_4$ resulted in higher viscosity of the solution which made it more difficult to spray. Therefore higher gas pressure was used in the spray system. Each cycle consisted of the $H_2SO_4$-based etchant spray for 1 s, the rinse solution spray for 4 or 5 s, and dry $N_2$ blow for 5 s. The carried out etching cycles were 1, 3, and 5 cycles. The stage was rotated at 100 rpm in all sequence. The temperature of solutions were 20 °C. The etching carried

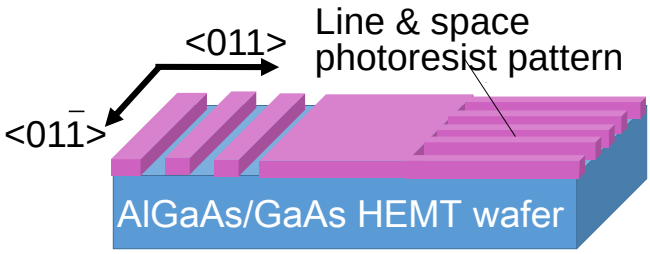


Fig. 6-2. Schematic of the mask pattern.

Table 6-1 Sequence and process time in a cycle

| | $H_2SO_4$: $H_2O_2$ : $H_2O$ | | |
|---|---|---|---|
| | A | B | C |
| | 1:1:1 | 1:0.2:1 | 1:1:10 |
| 1. Etchant spray | 1 s | 1 s | 1 s |
| 2. Rinse spray | 4 s | 5 s | 5 s |
| 3. Dry $N_2$ blow | 5 s | 5 s | 5 s |

out in the room temperature ambient. After etching, the photoresist mask was removed. The etching depth was measured the depth between unetched surface and etched surface from the SEM images. Also the cross-sectional structure was characterized from cross-sectional SEM images.

### 6.4.2 Etching depth

The measured etching depth of each etchant versus carried out cycle are shown in Fig. 6-3. Etching of the samples were successfully carried out

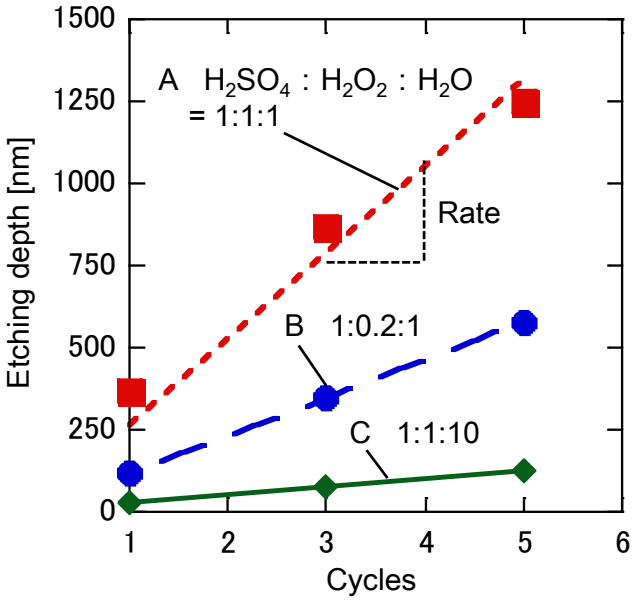


Fig.6-3 Etching depth vs. etching cycle.

Table 6-2 Evaluated etching rate

| $H_2SO_4$:$H_2O_2$:$H_2O$ | | Etching rate |
|---|---|---|
| A | 1:1:1 | 260 nm/cycle |
| B | 1:0.2:1 | 120 nm/cycle |
| C | 1:1:10 | 25 nm/cycle |

using the wet chemical etching machine with $H_2SO_4$-based etchant. The etched surface was smooth, similar to that obtained by dipping the sample in the etchant. The etching depth were depended on cycle number linearly. Therefore, we could control the etching depth by etching cycle number. From etching depth versus cycle number, the etching rate, etching depth per cycle number, was calculated. The calculated etching rate is shown in Table 6-2. The calculated the etching rate were from 25 nm/cycle to 250 nm/cycle. The low etching rate is obtained in $H_2SO_4$-based etchant system. The order of the etching rate seemed to depend on the ration of $H_2O_2$ to total etchant volume.

### 6.4.3 Cross-sectional structure

The SEM images of the cross-sectional formed mesa structure after 5 cycles etching using sequence in Table 6-1 are shown in Fig. 6-4. Usually anisotropic etching occurred in the wet chemical etching of a GaAs [12-15]. Similar etching was achieved in this digital wet chemical etching system. However the detailed configuration was different. The etchant A gave the forward-mesa shape along <01-1> direction. The mesa had sidewalls with an angle of 35.3° to the (100) GaAs substrate, corresponding to the crystallographic plane of {211}. However the upper part of the mesa showed {111} facet with an angle 54.7° to the (100) GaAs substrate. The height of the {111} portion was approximately 100 nm even changing the etching depth. Along <011> direction, the dovetail cross section was obtained. Formed angles

of the forward and reverse mesa planes were 54.7° and 109.5° to the (100) substrate, corresponding to the {1-11} and {-1-22} facets, respectively. The etchant B also provided the mesa shape similar to the etchant A. The {111} facet was again appeared in the upper part of the mesa, whose height was approximately 50 nm, not depending on the etching depth. The etchant C also gave the anisotropic etching, however, the cross sectional shape was slightly different from those obtained by the etchants A and B. The forward mesa shape was obtained for both <01-1> and <011> directions. The mesa sidewalls were composed of two planes with angles of 54.7° and 35.3° to the (100) substrate for both mesas. Corresponding crystallographic planes were {111} and {211} for the <01-1> direction mesa, and {1-11} and {2-11} for the <011> direction mesa, respectively. In general, the wet etching using the $H_2SO_4$-

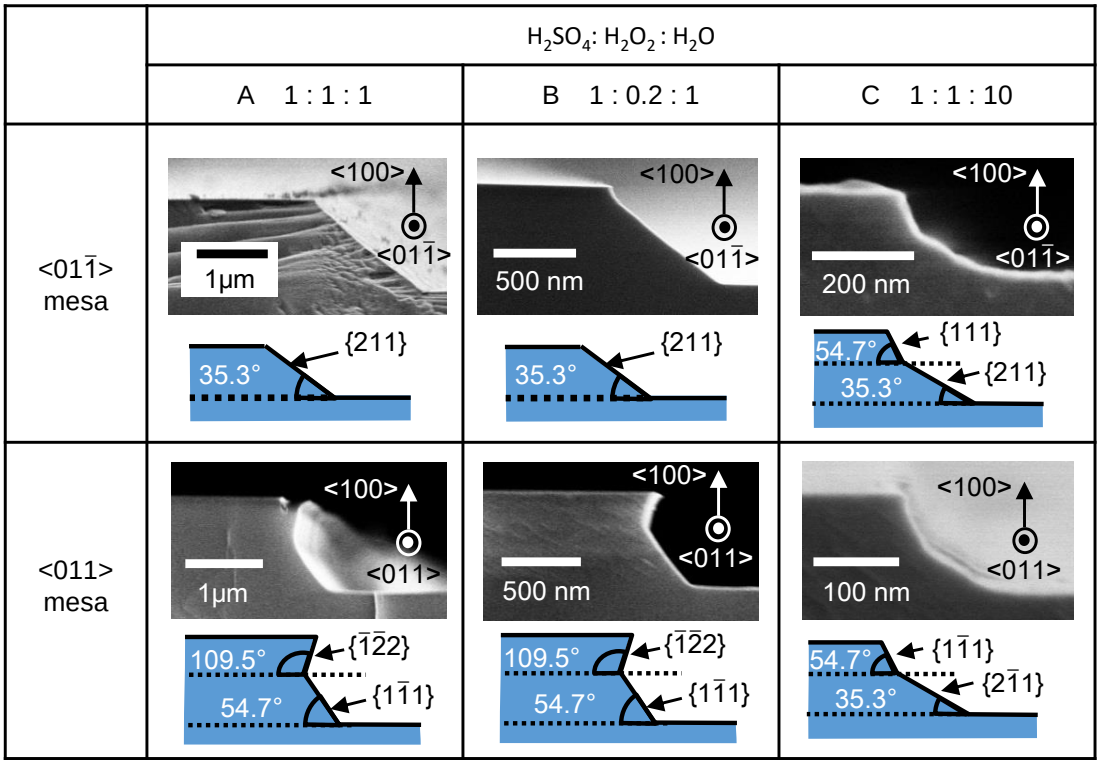


Fig. 6-4. Cross sectional SEM images of <01-1> and <011> mesa stripes with their schematic illustrations.

based etchant gives the forward mesa cross section with the {111} sidewalls for the <01-1> mesa and the dovetail cross section with the {1-11} and {-1-22} sidewalls for the <011> mesa [12].

## 6.5 Discussion

From these experiment results, the etching rate of 25 nm/cycle was obtained. It was lower than conventional $H_2SO_4$-based etchant etching. The obtained etched structures were anisotropic. However the shape had a difference between these results and conventional results. Usually etched the (100) GaAs by $H_2SO_4$-based etchant, the (111)-plane is obtained. In this study, the (211)-plane was obtained. The (111)-plane should be obtained because of the (111)-plane is lowest etching rate in GaAs. The reason is considered as short etching time. The etchant spray time was 1 s. Usually the wet chemical etching takes over 10 s. The etching reaction under 1 s is complex. Further investigation of etching reaction in short time is necessary.

## 6.6 Summary

In this chapter, a digital wet etching technique using a computer-controlled etching machine was proposed and demonstrated for high-precision GaAs-based nanostructure formation. This etching machine is

based on sequentially spraying etchant, rinse solution, and blowing dry $N_2$ onto the substrate. Using this system, the etching depth could be controlled in digital manner depending on the number of cycles. The low etching rate of 25 nm/cycle was achieved using the $H_2SO_4$-based etchant of 1:1:10. Anisotropic etching was observed in our wet etching technique, however the crystallographic plane of the sidewalls for the <01-1> mesa structure was partly different from that in the previous etching technique.

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# Chapter 7
# High-precision GaAs Digital Wet Chemical Etching

## 7.1 Introduction

In previous section, the digital wet chemical etching using the $H_2SO_4$-based etchant was investigated. However, the etching rate was still over 10 nm/cycle order, although the etching rate of a few nanometer order is demanded for the nanostructure formation providing meV order characteristic control. Such wet etching technique has not been achieved yet.

The basic chemical reaction of GaAs is given by Eq. (7.1) [1].

$$GaAs + 3H_2O_2 \rightarrow Ga(OH)_3 + As(OH)_3$$
$$Ga(OH)_3 + As(OH)_3 + 6H^+ \rightarrow Ga^{3+} + As^{3+} + 6\,H_2O \qquad (7.1)$$

From these equations, the chemical etching process consists of two steps, oxidation and oxide dissolution. By dividing these chemical reactions and causing them separately, it becomes possible to archive the etching rate in the atomic layer level. In this chapter I investigate the digital wet chemical etching that performs oxidation and oxide dissolution alternately.

## 7.2 Concept

The concept of high-precision digital wet chemical etching is shown Fig. 7-1. Usually in wet etching of compound semiconductor, the oxidation and dissolving the oxide is processed together [1]. In this study, it is separated etching reaction into two reaction, oxidation and dissolving the oxide. First the semiconductor surface is oxidized by oxidation agent and then the oxide is removed by acid. The oxidation agent spraying and acid spraying is done alternately. This concept was reported in 1996 [2]. It was done by manually process and only etching rate was reported. For nanostructure formation it is necessary to investigate not only etching rate but also the etched surface roughness.

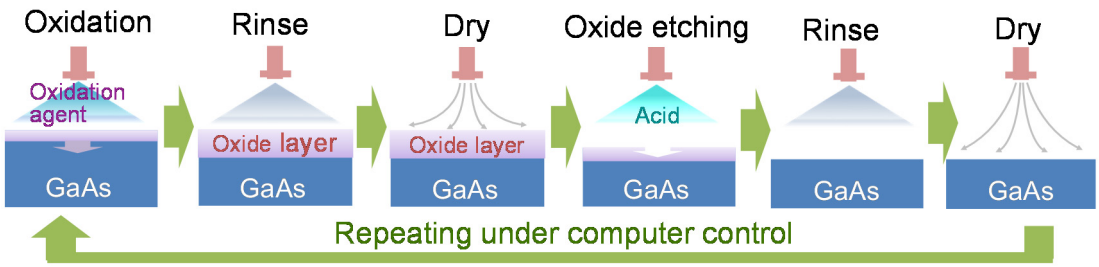


Fig. 7-1. The schematic of alternately etching concept

In this experiments, as an oxidation agent the hydrogen per oxide ($H_2O_2$ 30 wt%) was used. And as a removing oxide agent the HCl (35 wt%) was used. $H_2O_2$ is known to famous oxidation agent in compound semiconductor [3-5]. The HCl has a low viscosity and is frequently used as a native oxide removing agent. By using the digital wet chemical etching machine, a well-controlled the etching depth and time are achieved.

## 7.3 Experimental

The etching machine which is shown in previous chapter was used in high-precision digital wet etching. In the wet etching machine, the tanks were set for $H_2O_2$, HCl, and deionized water as show in Fig.7-2, respectively. The gas pressure was 0.1 MPa for $H_2O_2$ spray and HCl spray, 0.08 MPa for $H_2O$ spray. The $N_2$ dry spray of gas pressure was 0.2 MPa. The $H_2O_2$ was diluted in 10 %. The HCl was diluted in 1%, 3%, and 5% or 10%. First the surface oxidation GaAs by $H_2O_2$ was estimated. And then the etching depth and rate were characterized. Then the cross-sectional structure was characterized. Finally the etched surface was characterized and considered the digital etching process. The temperature of solution was 20 ℃. The stage was rotated at 100 rpm.

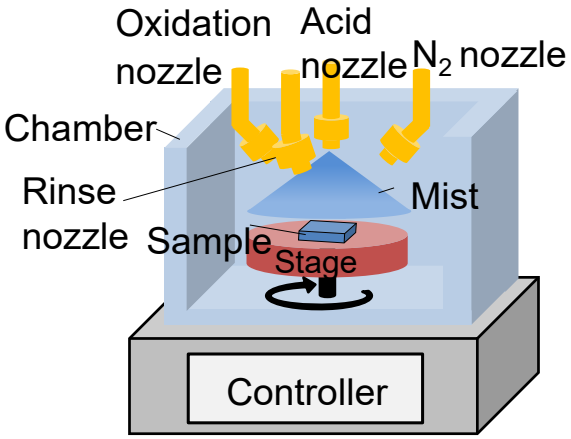


Fig. 7-2. Schematic of etching machine in this etching experiment.

The sample was used semi-insulated GaAs substrate. As a mask the photolithography resist as same as chapter 6 and shown as Fig.7-3.

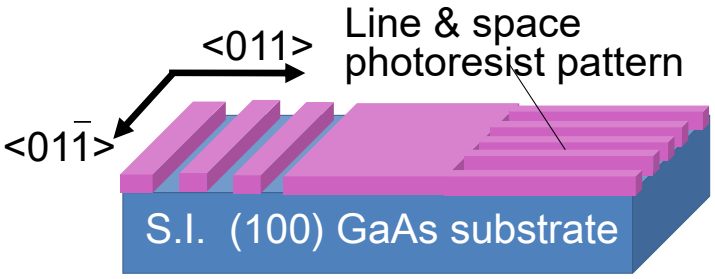


Fig. 7-3. Schematic of sample in this chapter.

First, I characterized the oxidation depth by 10% $H_2O_2$. The surface oxidation was carried out by the wet chemical etching machine. The spray times of 10% $H_2O_2$ were varied from 0.5 s to 5 s. To avoid the influence of native oxide, the native oxide was removed by spraying 10% HCl for 10 s before the $H_2O_2$ oxidation. That removed depth was defined as a native oxide thickness. And then the oxidation and removing oxide process were started 1 cycle. After spraying $H_2O_2$ and HCl, the surface on sample was rinsed by deionized water. After the removing the formed oxide by $H_2O_2$ and the resist, the etching depth was measured by atomic force microscopy (AFM). The oxide thickness was defined by the difference between the native oxide thickness and the etching depth.

Next, the experiment of repeating oxidation and removing oxide alternately by using digital wet etching machine was carried out. The etching depth and etching rate were characterized. The oxidation agent was 10% $H_2O_2$ and the acid was 1%, 3%, and 5% HCl. To avoid the influence of initial native oxide, the native oxide was removed by HCl treatment before alternately etching sequence. The time of removing the native oxide was 4 s for 1% HCl and 2 s for 3% and 5% HCl. After the native oxide removing,

immediately the etching sequence was started. The etching sequence was shown in Table 7-1. Both the oxidation agent spraying time and HCl spraying time were 0.5 s. To avoid the resist dissolving, the diluted solution and short spraying time of 0.5 s were used. The etching was done under room light. To evaluate the etching rate and to characterize the progress of the etching, 5, 10, 20, 30 cycles of the sequence was examined for etching.

Table 7-1 Etching sequence of alternately process.

| Sequence | |
|---|---|
| 1. $H_2O_2$ spray | 0.5 s |
| 2. Rinse spray | 5.0 s |
| 3. $N_2$ blow | 5.0 s |
| 4. HCl spray | 0.5 s |
| 5. Rinse spray | 5.0 s |
| 6. $N_2$ blow | 5.0 s |

To understand the nanoscale evolution and mechanism, the effect of the light irradiation was characterized using the white LED. By illuminated the white LED, the excited the holes on GaAs surface. The LED light power was 8 mW/cm$^2$. The white LED light irradiated during only oxidation or only removing the oxide. The concentration of HCl in this experiment was 3%. I also investigated the effect of the exited holes on oxidation and oxide dissolution processes separately by irradiating light only in $H_2O_2$ spraying or in HCl spraying.

After whole etching process the samples were cleaved into half. The cross-sectional structure was characterized by taking cross-section SEM

images. The groove surface of the etched samples were characterized by AFM. Then the surface roughness was characterized.

## 7.4 Results and discussion

### 7.4.1 Surface oxidation

Usually GaAs is oxidized in air at room temperature. The reported oxidized layer thickness was about 2-3 nm at room atmosphere [6]. This oxidized layer is called native oxide. The native oxide was removed by 10% HCl before oxidation thickness by $H_2O_2$.

The oxidation thickness by 10 % $H_2O_2$ versus spraying time is shown in Fig. 7-4. The error bars show the shallowest and the deepest depth. And an AFM image after 2.0 s spraying time is shown in Fig. 7-4. The smooth groove was obtained. The oxide formation of approximately 2 nm thickness immediately occurred within 0.5 s. After then, the oxidation process slowed down and saturated at 3 nm.

### 7.4.2 Etching depth

The measured etching depth versus cycles are shown in Fig. 7-5. The error bars are shown the standard deviation. The etching depth was depended on cycle number linearly. The calculated etching rate from Fig. 7-5 are shown in Table 7-2. The etching rate were 2.0 nm/cycle for 5% HCl, 1.2 nm/cycle for 3% HCl, and 0.35 nm/cycle for 1% HCl. The GaAs etching was successfully

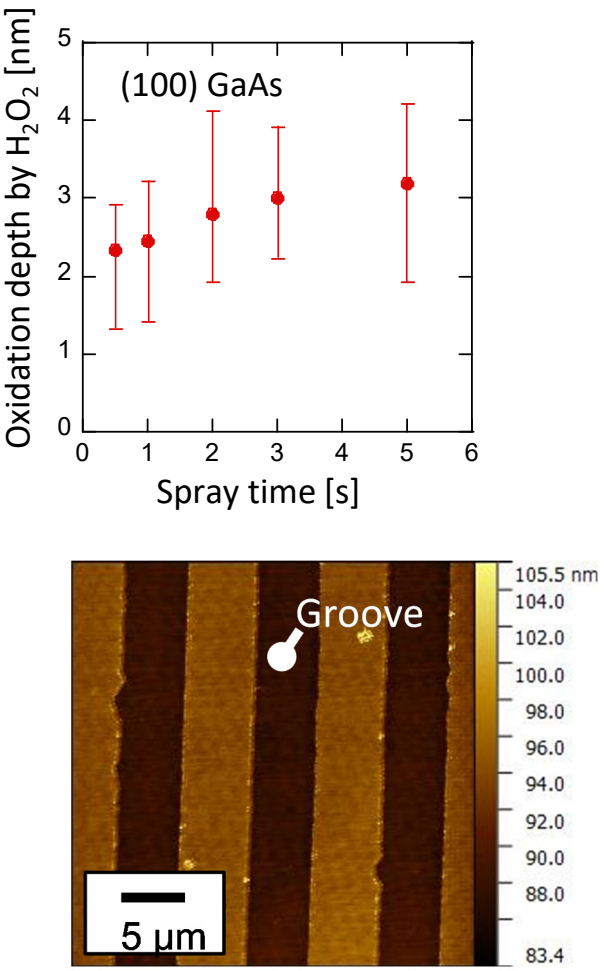


Fig. 7-4. The oxidation thickness vs spray time and an AFM image of after etching.

carried out by the alternate reaction process using the wet chemical etching machine. The etching rate was less than saturated oxidation depth of 3 nm. Then the etching depth was controlled by dynamic oxidation and oxide dissolution process. From these results the low etching rate less than 2.0 nm/cycle was achieved. Since the lattice constant of GaAs is 5.653 Å, achieved etching rate was comparable to 3.5 monolayers of GaAs.

The uniformity of etching depth is one of the important factors. The on-chip uniformity of etching depth was investigated in this study. The

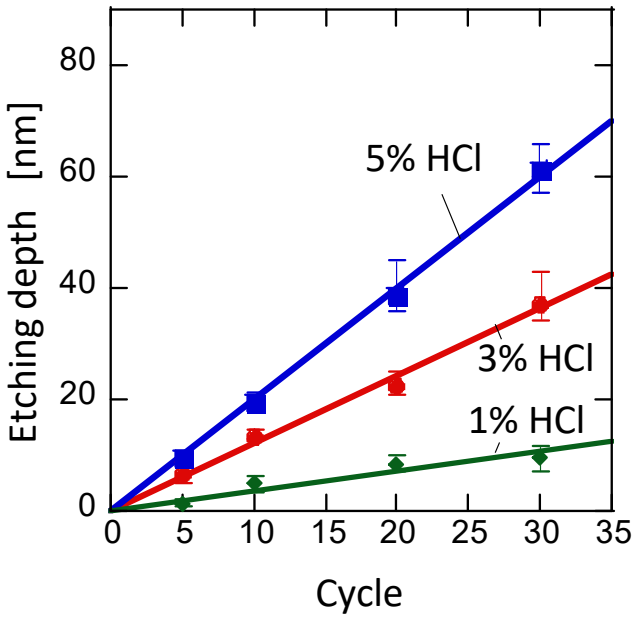


Fig. 7-5. Etching depth depending on cycle number.

Table 7-2. Evaluated etching rate.

| | Rate |
|---|---|
| 1% HCl | 0.35 nm/cycle |
| 3% HCl | 1.2 nm/cycle |
| 5% HCl | 2.0 nm/cycle |

etching depth was measured at thirty different positions on a chip of 6 x 6 $mm^2$ area size. The standard deviation in the 3% and 5% HCl concentration after 30 cycles were 36.9 and 61.3 nm, respectively. The deviation after 30 cycles was approximately 2.29 nm for 3% HCl and 2.00 nm for 5% HCl. From these result, the standard deviation per cycle was 0.076 nm/cycle for 3% HCl and 0.067 nm/cycle for 5% HCl. A good uniformity was obtained in this digital wet etching.

### 7.4.3 Structural characterization

The cross-sectional structure was characterized from the SEM images. The cross-sectional SEM images are shown in Fig. 7-6. The SEM image of 1% HCl is not shown because it was difficult to characterize the etched structure with very shallow depth. The etched structure was not anisotropic shape. In 5% HCl etching, the side etching was occurred. Side etching amount was larger than vertical etching amount. In 3% HCl, the side etching was not occurred.

Next the surface roughness was characterized. The surface roughness was measured the groove area of 1 μm² by AFM after etching and removed resist mask. The bare GaAs surface roughness was 0.3 nm.

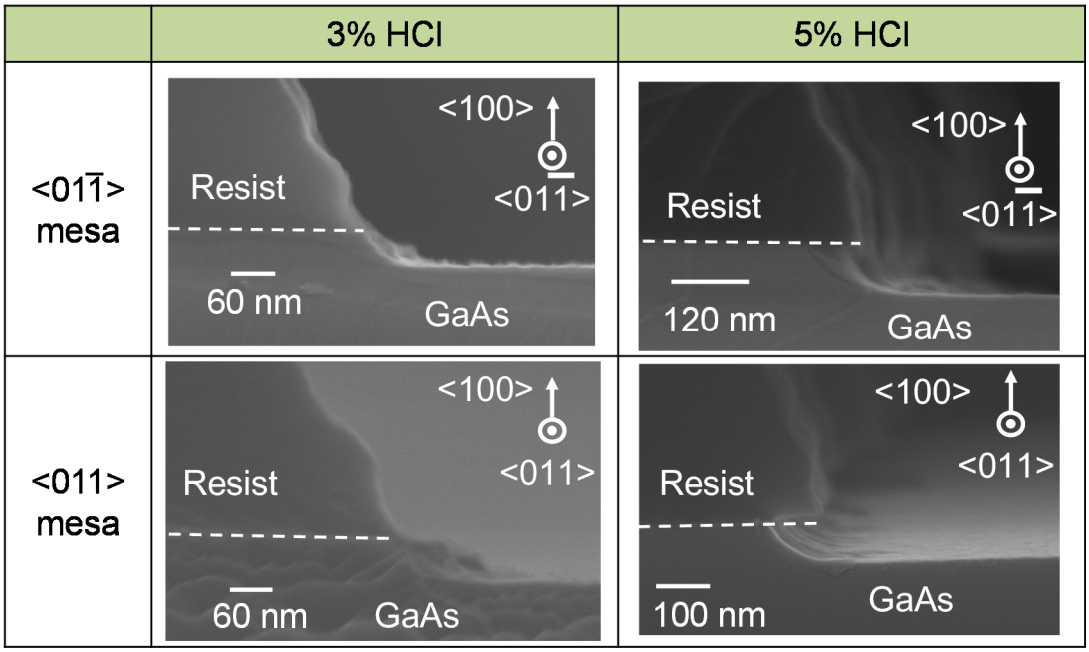


Fig. 7-6. Cross-sectional SEM images after 30 cycles etching

The bird-view AFM images after 30 cycles of all HCl concentration are shown in Fig. 7-7. The groove roughness is characterized in root mean square (RMS) value as shown in Fig. 7-8. The nanohillocks were seen on etched surface. The surface roughness RMS were 1.63 nm, 1.58 nm, and 1.07 nm for 1%, 3%, and 5% HCl, respectively. The nanohillocks number became smaller with increasing HCl concentration. Also the height of nanohillocks were increasing with cycle numbers. Also fig. 7-8 shows the roughness RMS depending on carried out etching cycle. The surface roughness increased with

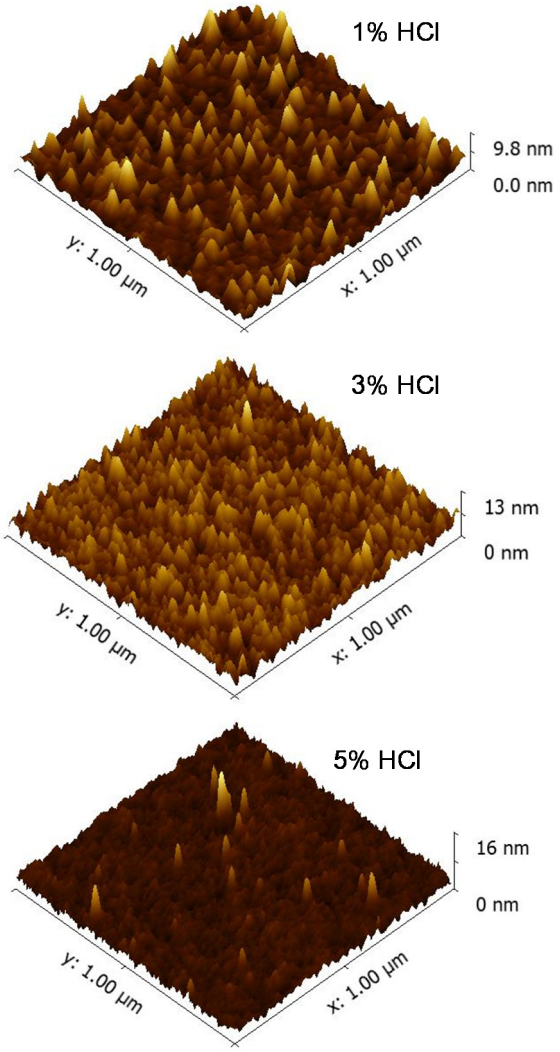


Fig. 7-7. The bird-view AFM images after 30 cycle etching.

etching cycle number. In 5% HCl, the surface roughness was smaller than other HCl concentration. From Fig. 7-7 and Fig. 7-8, it is obvious that the formation of nanohillocks was depended on HCl concentration.

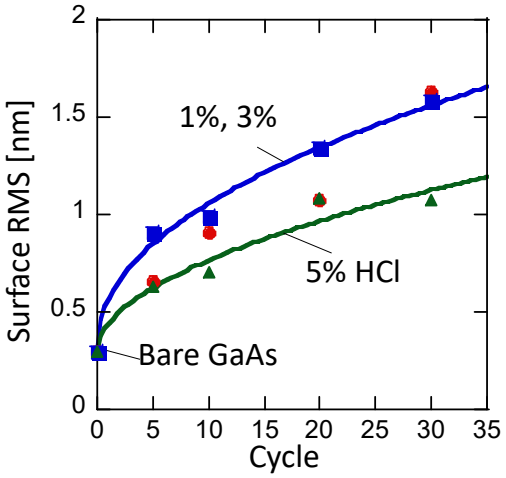


Fig. 7-8. The surface roughness RMS after digital wet etching.

### 7.4.4 Nanoscale structure evolution and mechanism

In this subsection the nanoscale structure evolution and mechanism are shown. By understanding the mechanism of nanohillocks formation, it may be possible to control the progress of structure formation during the digital etching. The above digital wet etching was carried out under room light irradiation with power of 90 μW/cm$^2$. It is possible that the exited hole affected the etching or oxidation process. To understand the effect of hole, the

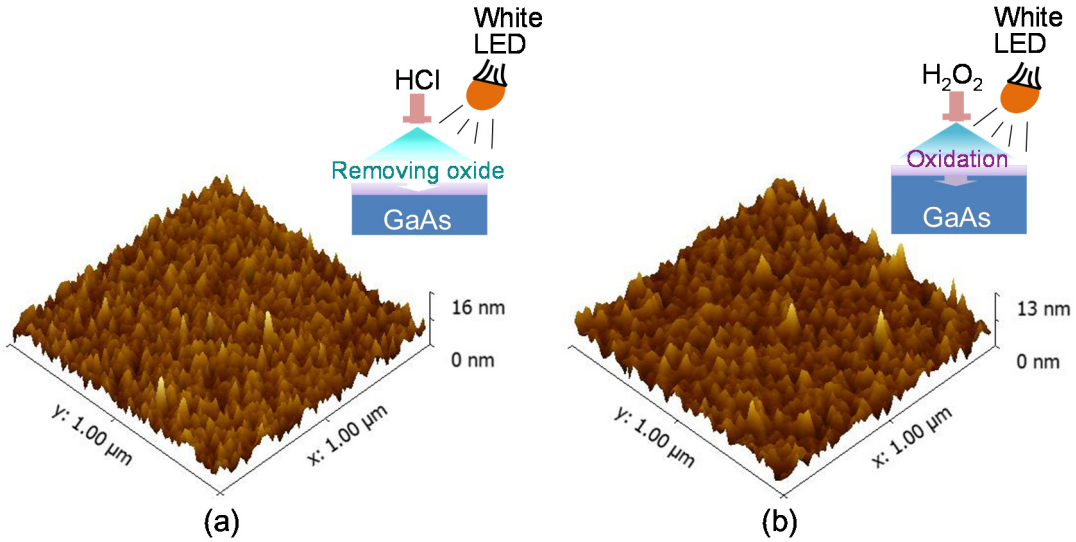


Fig. 7-9. The bird-view AFM images after 30 cycles digital wet etching with 3% HCl under white LED irradiation (a) only HCl spraying and (b) only oxidation.

digital etching under white LED light irradiation with 8 mW/cm$^2$ was carried out and characterized the etched surface.

The evaluated roughness RMS value after 30 cycles with 3% HCl etched surface was 1.55 nm for irradiation only removing oxide process and 1.27 nm for irradiation only oxidation process. The bird view AFM images are shown in Fig. 7-9. The RMS value was decreased by white LED light irradiation through the oxidation process. This means the exited holes affected the oxidation process. The nanohillocks formation was often reported the case of Si etching [7-10]. In case of Si nanohillocks formation, it is considered the anisotropy or micro mask (nanomask) as a cause. If the anisotropy is the cause, the difference of etching progress arises by the difference of etching rate of crystal facet and forms the hillocks. If the micromask (nanomask) is the cause, the surface atom bind the ion in etchant

or impurities in solutions and the mask is formed locally. That mask suppressed the etching and the hillocks are formed at the mask area. In this digital wet etching, it seems that the nano mask effect was occurred. In the case of Si etching, the $OH^-$ become a micro (nano) mask. In this etching, it seems that the $Cl^-$ became a nanomask. $Cl^-$ usually terminated the GaAs surface after removing oxide [11,12]. Cl terminated surface suppresses the oxidation of GaAs surface. In this digital etching, there was a difference depending on HCl concentration. In case of 5% HCl, it seems that the etched surface was terminated by $Cl^-$ uniformly after every cycle. Therefore the nanohillocks did not be produced. In case of 1% and 3% HCl, it seems that the etched surface was terminated by $Cl^-$ non-uniformity. From the etching rate, it seems that the $Cl^-$ was insufficient on surface. The non-uniformity terminated created the nanomask non-uniformity. By the non-uniformity nanomask, the next oxidation became non-uniformity. In case of white LED irradiation on only oxidation, it seems that the oxidation process was enhanced by exited holes. The chemical reaction equation of GaAs oxidation with hole is given by [1]

$$GaAs+6OH^-+6h^+ \rightarrow \frac{1}{2}Ga_2O_3+\frac{1}{2}As_2O_3+3H_2O. \quad (7.3)$$

This equation shows the hole affects the GaAs oxidation. Because of increasing hole of numbers, the GaAs oxidation was enhanced. Therefore it is considered that the locally nanomask was decreased. It seems that the nanohillocks were formed by repeating the non-uniformity oxidation. To obtain the smooth etched surface, it may be necessary to carry out the digital wet etching under high power light. It is necessary to investigate more detail

condition.

## 7.5 Summary

In this chapter I described the digital wet etching by oxidation and oxide dissolution alternately. The etching rate less than 2.0 nm/cycle was archived. The obtained etching rate was corresponding to a few atomic layers. From the characterization of the cross-sectional structures, the side etching was almost suppressed using the 3% HCl for the oxide dissolution. However there were nanohillocks on the etched surface. I discussed the mechanism that the surface Cl terminated surface acts as nanomasks.

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# Chapter 8
# Conclusion

The objectives of this work were the implementation of the threshold logic circuit using the GaAs nanowire network and its demonstration, and the development of the high precision wet chemical etching technique for formation of the GaAs nanowire networks in reproducible manner necessary for high density integration of the nanowire FETs having uniform characteristics. The main results of this work are summarized below.

In Chapter 4, I designed and fabricated a two-input threshold logic circuit using a GaAs-based nanowire network. From the characterization of the fabricated circuit, the logic operations of NOR and NAND gates and their switching by changing the threshold were successfully demonstrated.

In Chapter 5, I investigated the dynamic control of the threshold value in the nanowire network threshold logic circuit. In order to control the threshold value, the GaAs nanowire MISFET which had a hysteresis of the transfer characteristics was fabricated and this device was applied to the

inverter circuit for the threshold function in the threshold logic. I experimentally confirmed the memory function on the GaAs nanowire MISFET arising from the hysteresis characteristics. The threshold shift of the fabricated inverter integrating a GaAs nanowire MISFET was demonstrated. From the result, the capability of the reconfigurable threshold logic using the GaAs nanowire network was clarified.

In Chapter 6, I developed a computer controlled spray system for digital wet chemical etching and the digital wet etching technique using the $H_2SO_4$-based etchant was investigated. The etching rate as low as 25 nm/cycle was successfully demonstrated by spraying solution. Anisotropic cross-section structure were obtained in this technique. The high etching depth controllability in the present etching technique was confirmed.

Chapter 7 described another digital wet etching technique in which the oxidation and removing the oxide were alternately performed. This complex process was easily carried out by our computer-controlled etching machine with highly precise time control. Then the atomic-level etching with the etching depth less than 2 nm/cycle was archived. In addition, the suppression of the side-etching and spontaneous nanohillock formation on the etched surface were observed in this process. I explained the observed results by a simple model considering the dynamic flow of the solutions in sub-second process and the Cl termination of the surface.

From the above results, this study found a clue of new information processing using GaAs nanowire network and the wet etching technique for high precision fabrication of nanodevices.

List of figures

Chapter 5



Chapter 6



Chapter 7

List of Publications/Conferences

## 1. Publications related to this work


[1] Ryota Kuroda and Seiya Kasai, “GaAs Nanowire FET-integrated Threshold Logic Circuit,” Proceedings of The 22nd International Workshop on Post-Binary ULSI Systems, pp. 80-82, 2013.

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