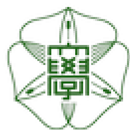
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DOCTORAL DISSERTATION

博士論文

Growth of III-V Semiconductor Nanowires and Their Photovoltaic Application

(III-V 族化合物半導体ナノワイヤの成長と太陽電池応用)

Graduate school of Information Science and Technology,

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北海道大学大学院情報科学研究科

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A dissertation submitted in partial fulfillment

of the requirements for the degree of

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Dissertation Supervisor

Professor Takashi Fukui

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Chapter 1 General Introduction

1.1 Overview

Along with the rapid economic development since the Industrial Revolution took off in the 18th century, fossil fuel consumption has been increased dramatically, as shown in **Fig. 1-1** [1]. As a result, exhaustion of fossil fuel reserve and environmental problems such as air pollution and global warming has become international issues [2]. Renewable energies, such as sunlight, wind, rain, tides, waves, and geothermal heat, are expected to solve these problems because the energies are non-polluting and sustainable on a human timescale. Especially, photovoltaic power generations, are generate electrical power by converting solar radiation into direct current electricity using semiconductors, have many advantages over no pollution and noise, no mechanical moving parts, very few limit of installation locations, constant efficiency regardless of the scale, and so on.

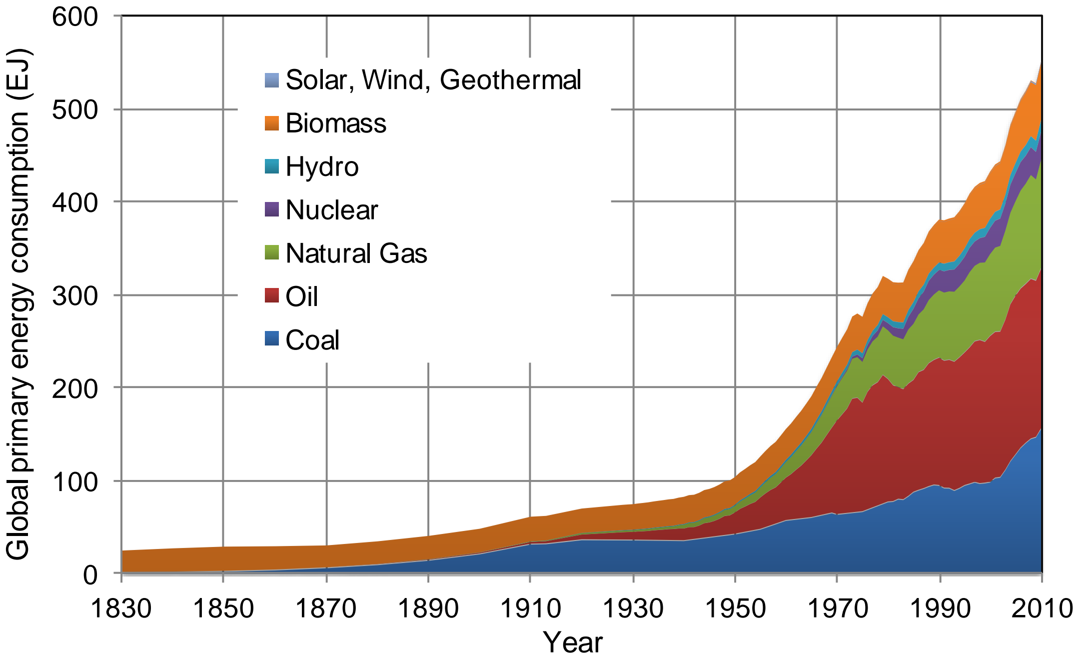

Fig. 1-1 Stacked chart of global primary energy consumption.

Thus the photovoltaics are one of the most promising power generation methods of renewable energy but it has a tremendous challenge to get the power-generating cost down to the levels in other power generation such as nuclear and thermal energy. Although to enhance the power conversion efficiency and reduce the fabrication cost of solar cells are required to accomplish the cost down, Silicon (Si) series solar cells that are the mainstream of solar cells will come closer to the limit of the efficiency and the production cost in the near future. Theoretical limit of the unijunction solar cells is approximately 33%, while efficiencies for the best lab examples of the Si series solar cells have 25.0%, that of gallium arsenide (GaAs) have 28.8%, and that of indium phosphide (InP) have 22.1% [3]. III-V semiconductor materials such as GaAs and InP are promising for one of the next-generation solar cells alternative to the Si series solar cells. Currently, the best lab examples of III-V semiconductor multi-junction solar cells, that are containing three *p-n* junctions, have demonstrated performance approximately 44%. Theoretical limit of the multi-junction solar cells is over 60% by using four or more junction [4]. Basically the choice of materials for each sub-cell is designed with lattice-matching, current-matching, and high performance optoelectronic properties. To keep crystal quality of the sub-cells, the lattice constant of the each materials must be closely matched. This restriction makes it difficult for achieving multi-junction cells with over **5**0% efficiency.

Semiconductor nanowire-array structures have been attracting a one of the innovative methods to overcome this problem. The nanowires are defined as one-dimensional structures with the diameters of hundreds nanometers or less and heights of several micrometers. The nanowires can be heteroepitaxially grown on the high lattice-mismatched substrate with maintenance of the crystal quality owing to the elastic relaxation of a strained layer at the interface between the bottom of a nanowire and the substrate [5]. Moreover, a size- and position-optimized nanowire array architecture can absorb an amount of light almost equal to that of a bulk structure with an antireflection coating because of its near-field-optics enhanced absorption and anti-reflection effect [6,7], resulting in low cost production. According to calculations, standard quantity of materials of the nanowire array solar cells become much less than that of the conventional crystal Si solar cells, as shown in **Table 1**. Furthermore, the standard quantity of materials could significantly improve by a combination of light concentration system and multi-junction cells. These structures have the great potential to resolve both the expensive fabrication cost and depletion of the semiconductor materials.

The first steps toward the practical use of nanowire-based solar cells are fabrication of position-controlled nanowire array and experimental proof of high crystal quality in lattice mismatch system. Since the method of growing Si nanowire using Au-assisted vapor-liquid-solid (VLS)

Table 1-1 Comparison of material use per power generation of solar cell structures.

	Power conversion efficiency (%)	Standard quantity of material (mg/W)	Amount used for 5MW (kg)
c-Si bulk (comm.)	14	3300	17000
c-Si thin (lab.)	17	630	3100
InP NW array (future)	20	4.8	24
4j NW + conc.(×500) (future)	50	0.042	0.21

growth was developed by Wagner and Ellis [8], most of the approaches to producing semiconductor nanowires have been based on this method [9]. In this method, nanowires are grown on a semiconductor substrate where eutectic liquid alloy particles were formed in advance by the reaction between the catalyst and a host substrate material below the growth temperature of nanowires. Hence, there is some concern about degradation of crystal quality and poor device performance owing to incorporation of the catalyst into grown nanowires and about difficulties in control the size and position of nanowires. As an alternative to VLS growth method, we have reported on the growth of group III-V semiconductor nanowires using catalyst-free selective-area metal-organic vapor phase epitaxy (SA-MOVPE) [10–12]. This method enables formation of nanowires without using a catalyst and has a great advantage in securing the crystal quality of nanowires over those grown using VLS. Another advantage is that the nanowires grown by SA-MOVPE have a flat-top crystal facet and we can form size- and position-controlled nanowires. In previous studies, the growth of binary-alloy III-V semiconductor, such as GaAs, InP, and indium arsenide (InAs), nanowires by SA-MOVPE have been reported [13–15], while that of the ternary-alloy III-V semiconductor, are commonly used to materials of multi-junction solar cells such as indium gallium arsenide (InGaAs) and indium gallium phosphide (InGaP), have been very few reports [16].

The second steps toward the practical use of nanowire-based solar cells are fabrication of position-controlled nanowire array solar cells and demonstration of these architectural effects. Theoretical simulations of the architectural effects and experimental demonstrations of the device of the nanowire-based solar cells have been reported since the early 2000s [17–19]. The nanowire solar cells previously-reported, however, were measured the cells composed of only one nanowire [18] and of nanowire array irregularly-sized, -positioned, and -growth direction [19]. Establishment of

position-controlled nanowire array solar cells and demonstration of its architectural effects are need for practical use of nanowire-based solar cells.

1.2 Objective

With a background described in the previous section, the purpose of this study is to investigate a lattice-mismatched growth and characterization of InGaAs ternary alloy nanowires formed on GaAs(111)B substrate. In addition, we fabricate position-controlled nanowire array solar cells and demonstrate their architectural effects. To achieve these purposes, we aim to achieve the key step toward the practical use of the nanowire-array solar cells. The objective of this work is summarized as follows;

i. to investigate a growth condition dependence of InGaAs ternary alloy nanowires,
ii. to analyze a crystal quality of a InGaAs nanowires grown on lattice-mismatched GaAs(111)B substrates,
iii. to realize a nanowire-array-based solar cells and demonstrate the architectural effects,
iv. to investigate a surface passivation to prevent surface recombination for a nanowire array solar cells, and
v. to propose a novel device structure for nanowire array solar cells.

1.3 Outline of This Thesis

This thesis describes a series of experiments aimed at understanding and controlling semiconductor nanowires growth by using SA-MOVPE and applying the nanowire array to photovoltaic devices. This thesis divided into 8 chapters.

Chapter 2 serves as an overview of the research field of nanowire growth and their photovoltaic application.

In chapter 3, detailed fabrication and characterization techniques of semiconductor nanowires and their photovoltaic application are described. First, we describe overview of a MOVPE growth technique, the growth process, the system, and the growth characteristics. Next, the growth method of semiconductor nanowires by using SA-MOVPE is described. Third, we explain the fabrication process for nanowire array solar cells. Finally, we describe characterization techniques that used for observing and imaging of structural information and investigation of optical properties of nanowires and measurement of solar cell properties.

In chapter 4, we describe a growth of InGaAs ternary alloys nanowire arrays on GaAs(111)B substrates by using SA-MOVPE. First, growth temperature dependence of the InGaAs nanowires on GaAs(111)B are explained. The uniformity, the growth rate, and the atomic composition are influenced by the growth temperature. Second, we represent effects of lattice mismatch on the crystal quality for InGaAs nanowires grown on GaAs(111)B substrates. The crystal quality is investigated by using the transmission electron microscopy and micro-photoluminescence measurement.

In chapter 5, we elucidate a growth of position-controlled InP core-shell nanowire array by using SA-MOVPE and their photovoltaic application. We experimentally demonstrated a low reflectance effect and a surrounding light absorption effect of nanowire array. In addition, a dependence of the performance characteristics on the illumination intensity is investigated.

In chapter 6, we discuss an application of a lattice-mismatched AlInP window layer to passivate a InP core-shell nanowire array solar cells. One of the disadvantages of nanowire arrays for photovoltaic application is high surface recombination due to high surface-to-volume ratio. Here we investigate the surface passivation for nanowire array solar cells to solve the problem. Performance characterization comparison of with and without the passivation layer for InP core-shell nanowire array solar cells are discussed.

In chapter 7, we describe a heterojunction solar cell that combines a *p*-doped InP nanowire array and a transparent indium tin oxide (ITO) layer. The ITO not only acted as a transparent electrode but also as forming a photovoltaic junction. The device need only one doped nanowire growth layer instead of two, resulting in improving the growth controllability and reducing the cost. We discuss a comparison of the device to world-record InP cell in an internal quantum efficiency.

Summary and conclusions of this work are shown and outlook for nanowire array solar cells are discussed in chapter 8,

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Chapter 2 Fundamentals

In this study, the semiconductor nanowire array based photovoltaic cells are investigated by using selective-area metal organic vapor phase epitaxy (SA-MOVPE). The semiconductor nanowires are expected to be building-blocks for future nm-scaled electronics and optoelectronics, and have been studied for the last several decades. The array of nanowires has many advantages for photovoltaic application arise from such a unique structure.

This chapter describes the fundamentals and features of semiconductor nanowires and their photovoltaic application.

2.1 Semiconductor Nanowires

2.1.1 VLS method

Growth of free-standing semiconductor nanowires using Au-assisted vapor-liquid-solid (VLS) method was developed by Wagner and Ellis at Bell Labs in 1964 [1]. Then, for long years, research of nanowires was not active. After research group of Hitach demonstrated the growth of GaAs *p-n* junction nanowires by VLS method and their optoelectronic application in the early 1990s [2,3], the nanowires have become a focus attention in the field of nanoscale electronic/photonic devices. The device applications of semiconductor nanowires have mainly been realized using the catalyst-assisted VLS method because of uncomplicated growth process. InP nanowire field-effect transistors [4], GaN nanowire lasers [5], and piezoelectric nanogenerators based on ZnO nanowire arrays [6] were demonstrated. In this method, the nanowires are grown on a semiconductor substrate where eutectic liquid alloy particles were formed in advance by the reaction between the catalyst and the host substrate material, as shown in **Figs. 2-1**. One-dimensional crystal growth occurs from

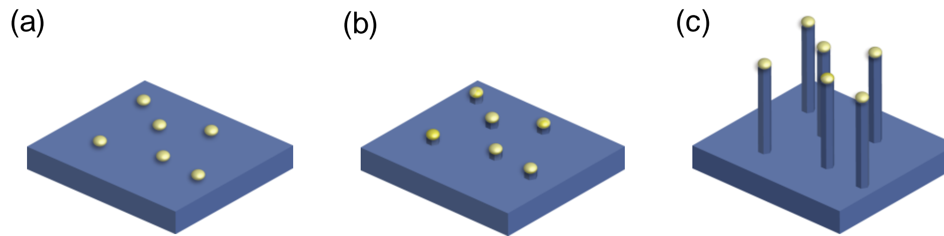

Fig. 2-1 Schematic of catalyst-assisted VLS growth of nanowires: (a) metal particles are deposited onto a substrate and heated the particle to form liquid droplets, (b) nucleation occurs at the droplet-crystal interface during an appropriate supersaturation of growth materials is achieved, (c) nanowire growth occurs at the droplet-wire interface.

nucleated metal seeds at the liquid-solid interface during a gas containing the growth materials flows over the grown substrate. The diameter and position of the nanowires are determined by that of the metal seeds. The method is higher growth rate and lower growth temperature than the conventional planar growth. However, there is concern about degradation of crystalline quality and device performance owing to incorporation of the metal catalyst into grown nanowires.

2.1.2 SA-MOVPE

Alternatively, the semiconductor nanowires can be grown by selective area growth (SAG) method which restricts the growth area using a mask substrate. The SAG, using chloride phase epitaxy of Si, was developed by Joyce and Baldrey in 1962 [7]. They used Si(111) substrate covered with SiO2 mask for the SAG. After a quarter-century later, fabrication of narrow two-dimensional electron gas channels on GaAs/AlGaAs using SA-MOVPE was first reported by Asai *et al*. in 1987 [8]. Following this, quantum wires structures [9,10], tetrahedral dot structures [11] of III-V compound semiconductors using this method were also demonstrated by Fukui *et al*. at NTT Lab.

The first application of SA-MOVPE for fabrication of the nanowire structure was reported by Hamano *et al*. in 1997 [12]. They grew GaAs nanowire array on a SiO_2 masked GaAs(111)B substrate for applying two-dimensional photonic bandgap crystals. Since the beginning of 2000s, growth of III-V semiconductor nanowires by this method have been studied mainly among our group. Growth condition dependences of InGaAs [13], InP [14, and GaAs nanowire array [15], controlled

growth facet for axial/radial direction of InP [16] and GaAs nanowires [17], and growth of InAs nanowires on Si(111) [18] have been investigated.

Schematic illustration of nanowires growth process using catalyst-free SA-MOVPE is shown in **Fig. 2-2**. After a SiO_2 film of a few tens of meter thick was deposited on the (111) substrate surface, periodic array of opening patterns were defined using electron beam lithography and wet/dry etching. Then the growth of nanowires on the partially-masked substrate was carried out in a MOVPE system.

2.2 Nanowire-Based Solar Cells

Semiconductor nanowires and its array structures have a great potential to realize high power conversion efficiencies and low fabrication costs of solar cells. The nanowires are one-dimensional architecture with diameters less than a micrometer, which should allow efficient lateral stress relaxation. Moreover, their array structure is able to absorb incident light almost perfectly with reduced material use through combining intrinsic anti-reflection and efficient absorption effects. These advantages have been stimulated research into nanowire-based solar cells.

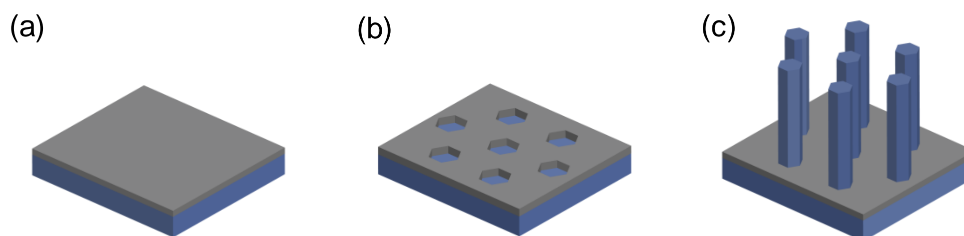

Fig. 2-2 Schematic of nanowires fabrication by SA-MOVPE: (a) deposition of thin SiO_2 film on substrates, (b) definition of opening patterns using electron beam lithography and wet chemical etching, (c) faceting growth of nanowires occurs by MOVPE.

2.2.1 History

Photovoltaic cells based on a single nanowire or nanowire arrays have been theoretically and empirically demonstrated from the mid-2000's and increasing exponentially over time, as shown in **Fig. 2-3**. Comparison between the device performance of a radial p-n junction nanowire array cell geometry and that of a conventional planar cell geometry [19] and optical absorption in Si nanowire arrays [20] and InP nanowire arrays [21] were simulated. Meanwhile, wide variety of semiconductor materials such as ZnO nanowire arrays [22], a Si single nanowire [23], *p*-GaN nanowire arrays on *n*-Si [24], InP nanowire arrays [25], a GaAs single nanowire [26], and CdS/CdTe nanowire arrays [27] was reported. However, power conversion efficiencies of these early works on the nanowire or the nanowire array based solar cells were much lower than that of the conventional planar cells because of unoptimized cell design such as a diameter, height, array pitch, doping concentrations and passivation technologies and of difficulties on the fabrication of position-controlled and high-quality nanowire arrays. Since the beginning of 2010's, solar cells exceeding 10% efficiency of a GaAsP single nanowire [28] and InP nanowire arrays [29] and applied technology such as a tandem junction structure [30] and a surface passivation [28,31] were investigated, therefore nanowire-based solar cells is steadily going on practical realization.

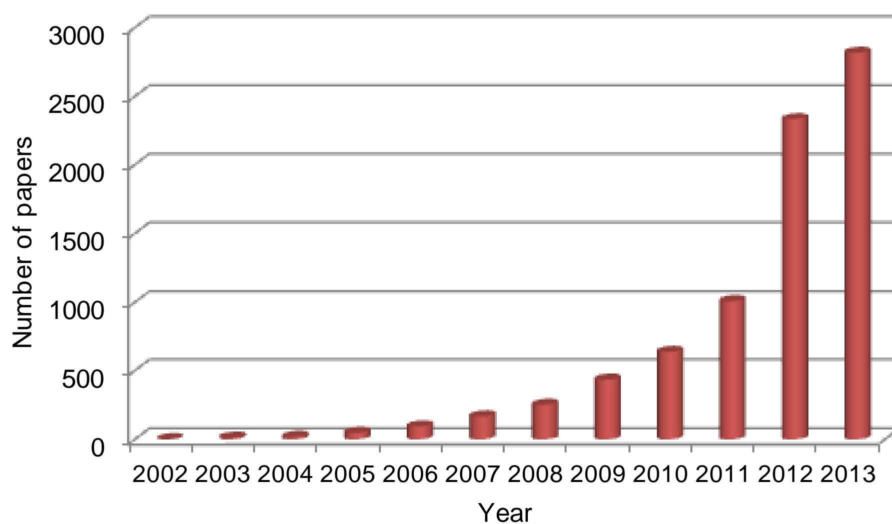

Fig. 2-3 Number of publication on nanowire-based solar cells. (Web of Science database, topic = (nanowire* OR nanorod* OR nanowhisker*) AND ("solar cell*" OR "photovoltaic cell*"))

2.2.2 Advantages

Absorption Enhancement

When the diameter of the nanowire is comparable to or smaller than the radiation wavelengths, the nanowire can absorb not only the portion of a wave incident directly on it but also the surrounding wave [20]. The geometric-optics definition of incident area does not apply due to this effect, and the rigorous solution of the Maxwell equation is imperative to explain this properties. The detailed balance efficiency limit of InP nanowire array solar cells was simulated by Kupec *et al*., as shown in **Fig. 2-4** [21]. In case of the diameter of 180 nm and the spacing of 360 nm, the array cells compete with the conversion efficiency of conventional planar structures despite of only 38% of active material. In 2013, Krogstrup *et al*. experimentally demonstrated that the enhanced light absorption using a vertically-aligned single GaAs nanowire cell with the diameter of 425 nm by using scanning photocurrent measurement [32]. This advantage lead toward the reduction in fabrication costs of solar cells.

Antireflection

Nanowire arrays have an intrinsic antireflection effect due to these unique structures. Effective-medium models predict a reduction of the reflectance of nanowire array layers stem from the effective refractive index of nanowire arrays are higher than the air and lower than the same material substrates [20]. In fact, the effect was experimentally demonstrated by the randomly-aligned nanowire array of various semiconductor materials such as Si, InP, GaP [33,34]. While the conventional planar structures generally have an average reflectance of ~30%, the nanowire arrays have less than a few percent of that in the wavelength range of solar spectra. The reflectance of nanowire array is so significantly-low that it is not necessary to applied antireflection coating on the cells.

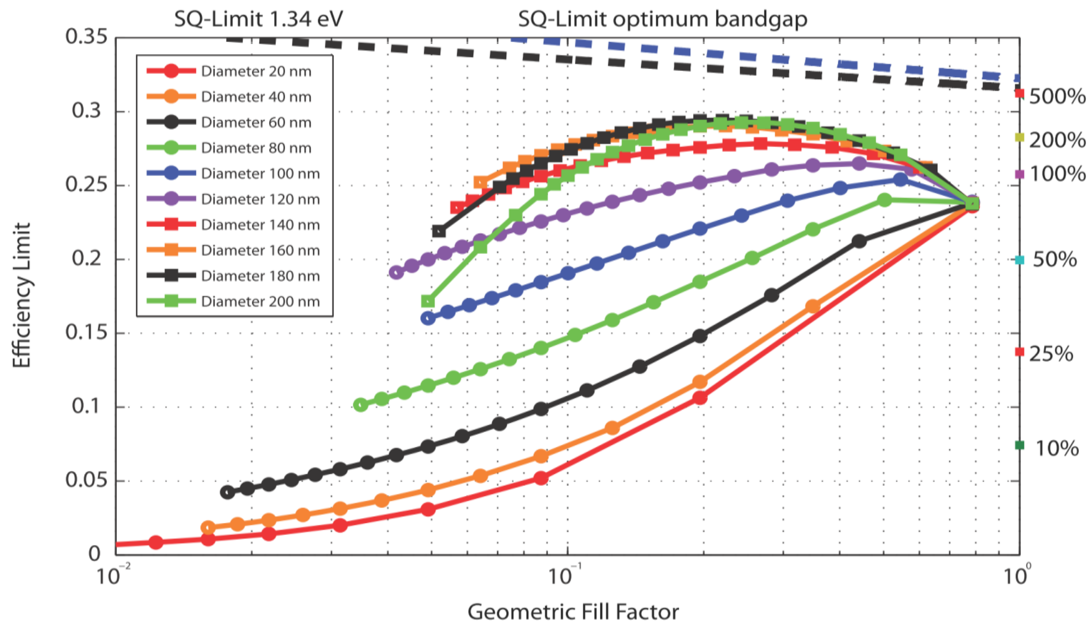

Fig. 2-4 Detailed balance efficiency limit of InP nanowire array solar cells for various diameters at various geometric fill factors, thermodynamic limits (dashed lines) and reference thin-film efficiencies for various material use compared with that of the nanowire cells (markers on the right). Nanowires are arranged in square array and have the height of 2000 nm [21].

Short Carrier Collection Lengths (as radial junction)

Vertically-aligned nanowire arrays, each having a radial *p-n* junction, are electrically superior compared with that of thin film structures [19]. While the each nanowire could absorb incident lights in the long axial direction, it could collect photo-generated carriers in the short radial direction. The structure, which could carrier collection effectively, allow for using the inexpensive materials with low minority-carrier diffusion lengths due to either a high density of defects or a high concentration of impurities. In case of the conventional planar *p-n* junction cells, the minority-carrier diffusion length must be long to collect the photo-generated carriers completely to achieve high conversion efficiency.

Higher Critical Thickness (as axial junction)

The nanowires with the diameters in nanometer-micrometer range have free surfaces not only at the top but also at the side, resulting in efficient lateral stress relaxation. Thanks to the elastic relaxation of a strained layer at the interface, we can expect that semiconductor nanowires are

heteroepitaxially grown with high crystal quality on substrates of different lattice constants. The relation between a critical layer thickness of the nanowire and that of the radius was computed by Glas, as shown in **Fig. 2-5** [35]. The critical thickness is increase with decreasing the nanowire diameter. This calculation agree with the experimental result reported by Tomioka *et al*. that GaAs nanowires with the diameter of ~30 nm were coherently grown on Si(111) substrates with lattice mismatch of 4.1% [36]. The advantage gives expansion of material selectivity for lattice-mismatched multi-junction system for achieving the ultrahigh efficiency cells.

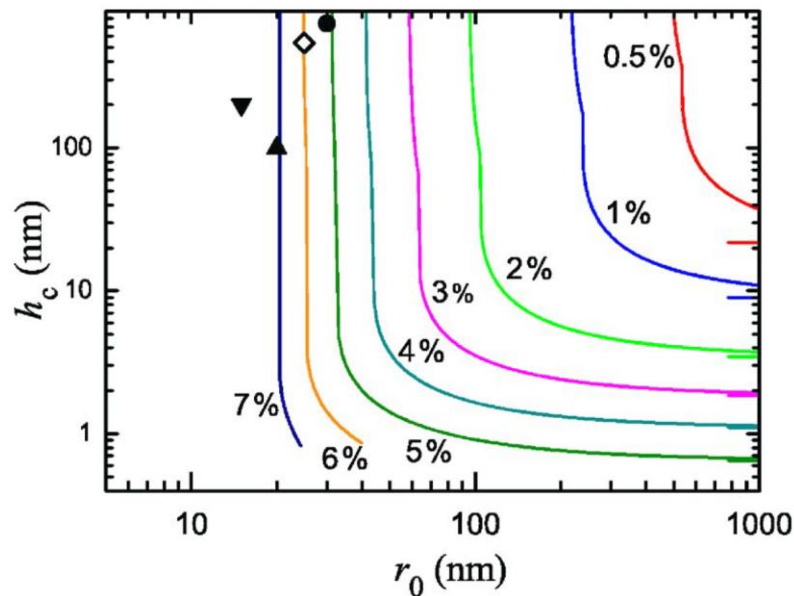

Fig. 2-5 Variations of the critical thickness of a misfitting layer growing on top of a nanowire as a function of the wire radius, r_0, for various values of the lattice mismatch and a Poisson's ratio of 1/3 [35].

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Chapter 3 Experimental Techniques

3.1 Introduction

This chapter deals with fabrication and characterization methods for III-V semiconductor nanowires used in this work. The nanowires are formed by using selective-area metal-organic vapor phase epitaxy (SA-MOVPE) which is one of the formation methods of semiconductor nanostructures based on pure vapor phase growth. First, we describe the principle and system of the MOVPE growth. After that the fabrication method of nanowires by using SA-MOVPE and fabrication process of their photovoltaic device are shown. Finally, we introduce the structural and optical characterization methods for the nanowire array structure.

3.2 Principles of MOVPE

3.2.1 Advantages

MOVPE is one of the chemical vapor deposition (CVD) methods to epitaxially form single crystal or polycrystalline thin films on substrates by using carrier gases including precursors such as metal-organic compounds and hydrogen compounds. The features of MOVPE are as follows;

i. to be able to control atomic composition of mixed crystal semiconductors by ratio of supplying gases,
ii. to be able to grow various kinds of compound semiconductors by using a number of metal-organic compounds and hydrogen compounds of group II, III, IV, V, and VI,

iii. to be able to form steep heterostructures and pn-junctions by precise flow control and rapid lines switching of supplying gases, and

iv. to be able to uniformly grow epitaxial layers on many large-area substrates at once.

3.2.2 MOVPE System

Figure 3-1 illustrates the MOVPE system schematically. The system fall into three essential components: a gases delivery system, a reactor system, and exhaust disposal system.

The gases delivery system consists of lines for carrier hydrogen (H_2) gas and precursors, bubblers that are filled with metal-organics, and mass-flow controllers (MFCs), and is connected to the others in downstream. We can control saturated vapor pressure of the metal-organics using constant-temperature bath for the bubblers. Therefore, the metal-organic supply could adjustable by the temperature of the bubblers and the gases mass flow.

The reactor system has a quartz reactor, a quartz tray for putting substrates, and a carbon susceptor and rf-coil for heating the substrates. We used a reactor of horizontal type in this study, which has advantages for in-plane uniformity due to low disordered gas stream and good controllability of an interface composition between the materials because of small volume in the reactor.

The exhaust disposal system comprises exhaust lines, a rotary pomp to decrease the pressure, and a ballast line to stabilize the reactor pressure. These are connected to exhaust toxic gas treatment system because toxic gases and metal-organics such as arsine, silane, tertiarybutylphosphine, trimethylgallium, and trimethylindium are used as the source materials in MOVPE. The ballast lines compensate vacuuming of the rotary pomp to control and stabilize the pressure in the reactor. The working pressure of 0.1 atm is maintained with the automatic pressure controller, because it can form a steep hetero-interface due to high velocity of carrier gases flow.

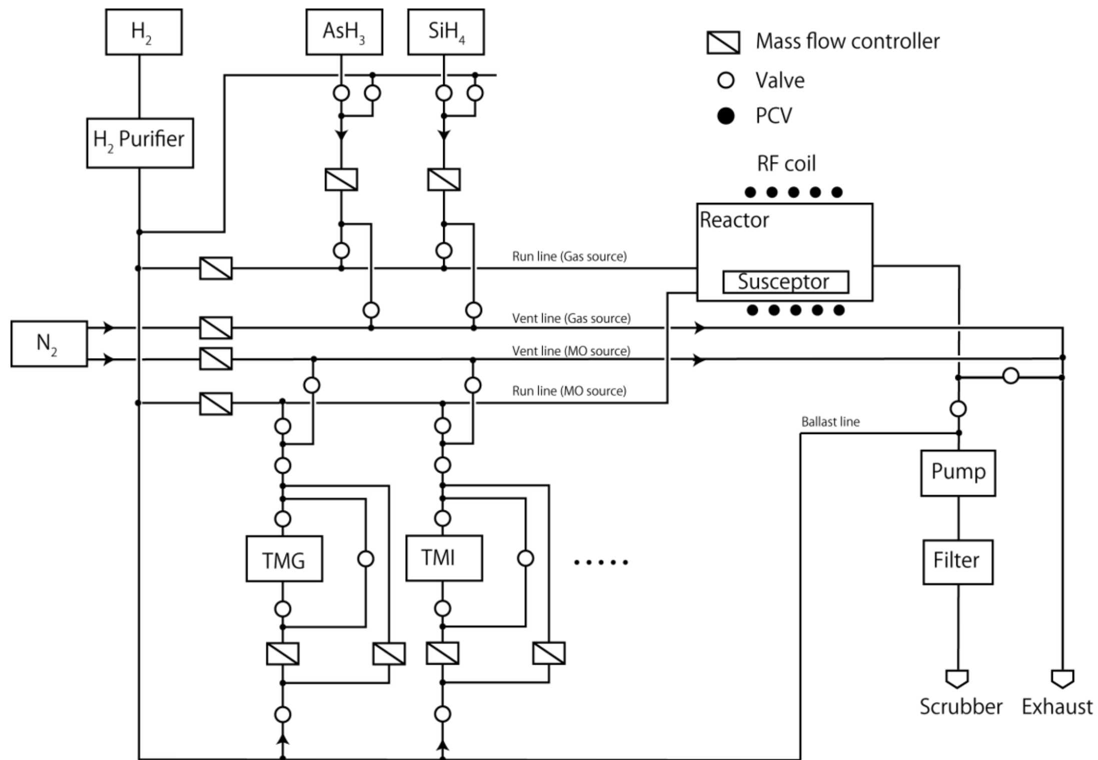

Fig. 3-1 Schematic of MOVPE system.

3.2.3 MOVPE Growth Process

There are four general phases of crystal growth by MOVPE as follows [1].

i. Thermodynamics that dominated driving force for the overall growth process, and kinetics defines the rates at which various steps occur.

ii. Mass and heat transport phase by diffusion and convection of the source materials through boundary layer toward the substrate surfaces.

iii. Physical surface processes for surface migration and reconstruction, adsorption and desorption of radicals and adatoms, and two/three-dimensional nucleation.

iv. Chemical reactions phase for pyrolysis of precursors and adducts, adsorption/desorption of precursors and intermediates, and surface reconstruction.

The growth rate is determined by the slowest process among described above. When viscous fluids flow in the reactor, the flow velocity is decreased with approaching the inside wall and it become zero accordance with the Newton's law of viscosity (**Fig. 3-2**). The boundary layer is the layer of fluid in the immediate vicinity of the substrate surface where the slow velocity. The boundary layer thickness, δ, defined as the distance from the interface at which the velocity component parallel to the wall becomes 99% of its main-stream value;

$$\delta = 4.64 \sqrt{\mu L / \rho U_0} \tag{3.1}$$

where μ is coefficient of viscosity, L is the distance from front edge of the susceptor, ρ is density of gases, and U_0 is velocity of the gas. The thickness is increased in inversely proportional to the square root of the velocity and become thicker toward downstream. Because the source materials are consumed when the growing the crystals, there is a difference in the materials concentration between in the main stream and in the substrate surface. The source materials diffuse through the boundary layer into the substrate due to the differential concentration

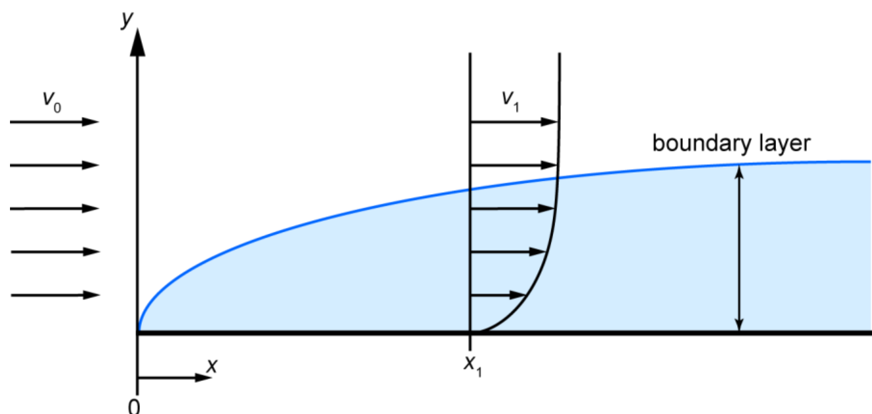

Fig. 3-2 Schematic of boundary layer, where v_0 is constant velocity at free stream and v_1 is velocity profile including the boundary layer.

3.3 Fabrication Processes

3.3.1 Nanowire Array Growth by SA-MOVPE

Selective area growth (SAG) is the bottom-up method for epitaxially growing semiconductor materials on the partially coated substrates by metals or amorphous thin film. The SAG by MOVPE has been studied from the late 1980's and used various electrical/optical applications such as hexagonal-facet double heterojunction laser [2] and GaAs/AlGaAs pyramids-shaped quantum wells [3]. The advantages of SA-MOVPE are as follows;

i. to be able to fabricate position- and size-controlled nanometer scale buildings,
ii. to be able to epitaxially grow high crystalline semiconductor materials with high growth rate, and
iii. to be able to form three-dimensional architecture differ from bulk structure.

The schematic of fabrication process for semiconductor nanowire arrays by SA-MOVPE is shown in **Figs. 3-3**. Fabrication of nanowires is started by preparing patterned substrates partially covered with a SiO_2 mask for SA-MOVPE. After a 20-nm-thick SiO_2 film is deposited on the substrate by plasma sputtering (**Fig. 3-3(a)**), hexagonal opening patterns of arbitrary diameters and size are defined using electron beam lithography and wet chemical etching with buffered hydrofluoric acid (BHF) (**Fig. 3-3(b)**). SA-MOVPE growth of semiconductor materials is carried out in a horizontal MOVPE system working at a pressure of 0.1 atm, and the total flow rate of the gases is maintained at 5.75 standard liters per minute (**Fig. 3-3(c)**).

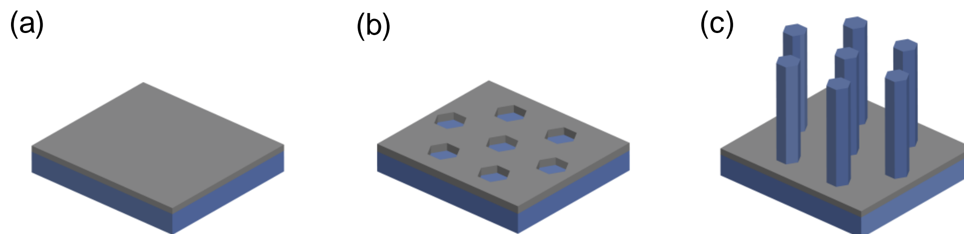

Fig. 3-3 Schematic of fabrication process for nanowire array by SA-MOVPE.

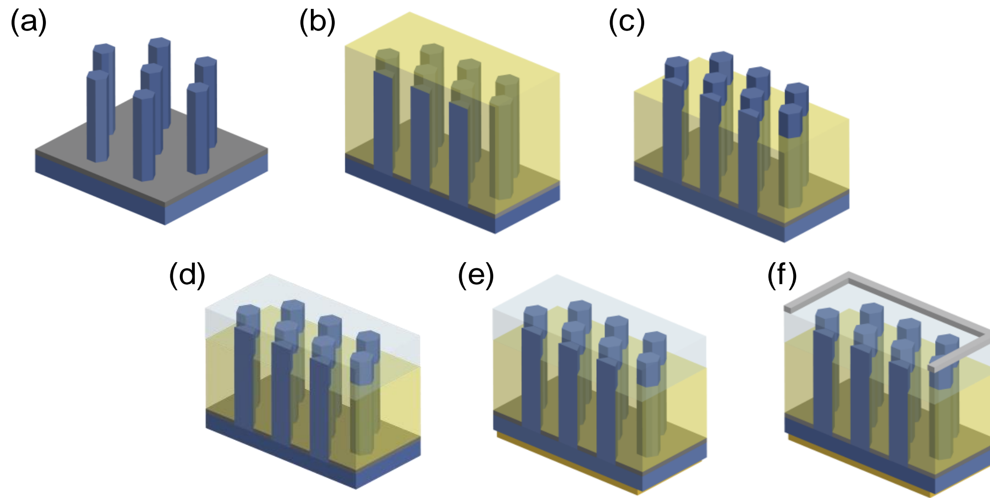

Fig. 3-4 Schematic of fabrication process for nanowire array solar cells

In this study, 5% arsine diluted in hydrogen and tertiarybutylphosphine are used as group V source materials and trimethylgallium and trimethylindium are used as group III source materials. As *n*-type and *p*-type dopants for InGaAs and InP nanowires, monosilane and diethylzinc are used respectively. The growth temperatures are between 480–650 °C for InP nanowires and 600–700 °C for InGaAs nanowires.

3.3.2 Nanowire Array Solar Cells

Figure 3-4 shows the schematics of fabrication procedures for nanowire array solar cells. The brief explanations are described below.

After the growth, the nanowire array is embedded by spin-coating benzocyclobutene (BCB, Dow Chemical). The overlaid BCB layer is etched by reactive ion etching with CF_4/O_2, exposing the tips of the nanowires. A transparent indium tin oxide (ITO, $SnO_2 : In_2O_3 = 10 : 90$ wt.%) layer is then rf sputtered at a rate of 0.11 nm/s for 45 min onto the nanowire array at room temperature and annealed in N_2 at 400 °C for 15 min. The sputtered ITO film typically has a sheet resistance of 10 Ω/□ and an optical transmittance higher than 85% in the wavelength range between 400 nm and 900 nm. U-shaped Ag and alloying Au-Zn electrodes are, respectively, formed on the ITO layer and back of the substrate.

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Chapter 4 Growth of InGaAs Nanowires on GaAs(111)B

We fabricated InGaAs nanowires in SiO_2 mask openings on a GaAs(111)B substrate at growth temperatures of 600–700 °C using catalyst-free selective-area metal organic vapor phase epitaxy (SA-MOVPE). At a growth temperature of 600 °C, particle-like depositions occurred, but they decreased in number and density when the growth temperature was increased and the mask opening diameter was decreased from 300 to 50 nm. Photoluminescence (PL) spectra measured for the nanowires indicated a blue-shift in the peak from 0.95 to 1.3 eV as the growth temperature was increased from 600 to 700 °C, indicating an increase in the Ga composition from 62 to 88% in the InGaAs nanowires.

In addition to the above, we analyzed the effect of lattice mismatch on crystal structure and quality of the InGaAs nanowires on GaAs(111)B. An energy dispersive X-ray (EDX) microscopy analysis indicated that the atomic contents of group-III atoms, Ga and In, were constant with little dispersion along a 2 μm-long nanowire. This indicates that a possible difference in migration length between In and Ga atoms on the sidewall facets has no effect on the compositional distribution along the nanowires with lengths of up to 2 μm. Photoluminescence spectra for InGaAs planar layers grown on GaAs(100) and GaAs(111)B substrates showed no peak corresponding the InGaAs band-edge emission, due to lattice mismatch between the layers and the substrate. However, the nanowires with a lattice mismatch of 2.1% showed a strong and sharp band-edge emission peak at 1.12 eV. This means that crystal quality of the InGaAs nanowires was better than that of the planar layers for a lattice-mismatched system.

4.1 Introduction

Free-standing semiconductor nanowires have become a focus of attention in the field of nanoscale electronic/photonic devices and bio-devices [1-6]. They have advantages for making one-dimensional vertical nano-architectures. III-V semiconductor nanowires with high crystal quality can be heteroepitaxially grown with high lattice-mismatch on Si substrates [7] owing to the elastic relaxation of a strained layer at the interface between the bottom of a nanowire and Si [8]. Moreover, a periodic nanowire array structure has the advantage of improving optical absorption and reflection over planar layers [9], and an InP nanowire array solar cell has been reported [10].

Since the method of growing silicon whiskers using Au-assisted vapor-liquid-solid (VLS) growth was developed by Wagner and Ellis [11], most of the approaches to producing semiconductor nanowires have been based on this method [12]. In this method, nanowires are grown on a semiconductor substrate where eutectic liquid alloy particles were formed in advance by the reaction between the catalyst and a host substrate material below the growth temperature of nanowires. Hence, there is some concern about degradation of crystalline quality and poor device performance owing to incorporation of the catalyst into grown nanowires. As an alternative to VLS, we have reported on the growth of group III-V semiconductor nanowires using catalyst-free selective-area metal-organic vapor phase epitaxy (SA-MOVPE) [13-15]. This method enables formation of nanowires without using a catalyst and has a great advantage in securing the crystal quality of nanowires over those grown using VLS. Another advantage is that the nanowires grown by SA-MOVPE have a flat-top crystal facet and we can form, with precise control of growth conditions, lateral/axial heterostructures, which should be more suitable for making Fabry-Perot cavity structures along the axial direction of the nanowire compared with nanowires grown by VLS.

In previous studies, we reported on the growth of InGaAs nanowires by SA-MOVPE [16-20] and on the fabrication of top-gate metal-semiconductor field-effect transistors using SA-MOVPE-grown InGaAs nanowires [21]. InGaAs is a bandgap-engineering material synthesized by controlling the composition of group-III atoms [22], in which the lattice constant also changes in accordance with the changes in composition. Thanks to the elastic relaxation of a strained layer at the interface, we can expect III-V semiconductor NWs are heteroepitaxially grown with high crystal quality on substrates for a lattice-mismatched system [8], where we might find a chance to develop a novel device based upon a strained energy band structure. Recently, we have found that the shape and alloy composition of ternary InGaAs nanowires obtained by SA-MOVPE are strongly dependent on the

growth conditions. It is thus necessary to further explore the growth conditions of the InGaAs nanowires for fabricating complex heterostructures.

This chapter describe the growth temperature dependence of InGaAs nanowires grown on GaAs(111)B substrates using SA-MOVPE and discuss the growth characteristics of the height and diameter of the nanowires, crystal composition, and optical spectra obtained by micro-photoluminescence (μ-PL). Additionally, the effect of lattice mismatch on crystal structure and quality of InGaAs nanowires grown on GaAs(111)B was investigated, using scanning electron microscopy (SEM), transmission electron microscopy (TEM), and μ-PL at 4 K.

4.2 Experimental Methods

Fabrication of nanowires was started by preparing patterned GaAs(111)B substrates partially covered with a SiO_2 mask for SA-MOVPE. After a 20-nm-thick SiO_2 film was deposited on the GaAs(111)B substrate by plasma sputtering, hexagonal opening patterns were defined using electron beam lithography and wet chemical etching with buffered hydrofluoric acid. The SiO_2 pattern was designed to be a periodic array of openings with the diameter d_0 in the range from 50 to 200 nm and the pitch a from 0.5 to 2.0 μm in 100 × 100 μm^2 regions. **Figure 4-1** shows a SEM image of a mask

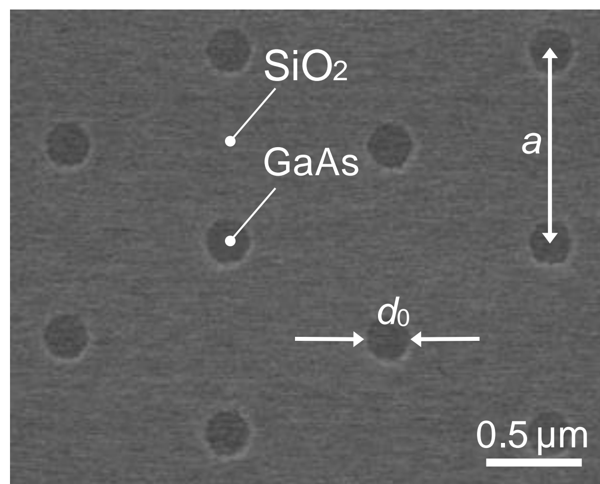

Fig. 4-1 SEM plan-view image of the mask substrate surface with periodic array openings with diameter d_0 and pitch a.

pattern fabricated on the substrate with d_0 = 200 nm and a = 1.0 µm. SA-MOVPE growth of undoped InGaAs was carried out in a horizontal MOVPE system working at a pressure of 0.1 atm, and the total flow rate of the gases was maintained at 5.75 standard liters per minute. The source materials were 5% arsine (AsH_3) diluted in hydrogen as a group V source material, and trimethylgallium (TMGa) and trimethylindium (TMIn) as group III source materials. For the experiments of growth temperature dependence, the partial pressures of AsH_3, [AsH_3], TMGa, [TMGa], and TMIn, [TMIn], were 1.25×10^{-4}, 1.42×10^{-6}, and 1.22×10^{-7} atm, respectively. The V/III ratio and [TMGa] to [TMIn] ratio were 81 and 92 : 8, respectively. Meanwhile, for the analyzing of the effect of lattice mismatch on crystal structure, [TMGa] was changed to 4.97×10^{-7} atom. The growth temperature T_G was varied between 600 and 700 °C. Substrate used for MOVPE were undoped semi-insulating GaAs(111)B and GaAs(100).

4.3 Growth Temperature Dependence

4.3.1 Structural Characterization

SEM 45°-tilted images of SiO_2-patterned substrate surfaces after SA-MOVPE at growth temperatures from 600 to 700 °C are shown in **Figs. 4-2(a)-(e)**. The pattern pitch a and the mask opening diameter d_0 are 1.0 µm and 100 nm, respectively. We can see particle-like depositions with diameters of 1 to 3 µm on the patterned areas for the samples grown at 600, 625, and 650 °C. The density of the particle-like depositions was maximum at 600 °C [**Fig. 4-2(a)**], but the depositions decreased in size and density with increasing growth temperature [**Figs. 4-2(b), (c)**] and disappeared

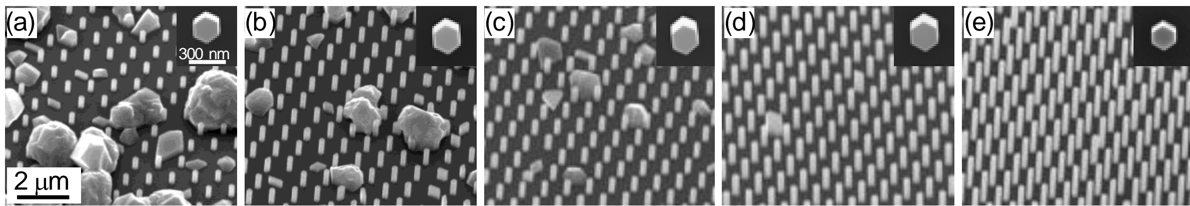

Fig. 4-2 SEM images of InGaAs nanowires grown at (a) 600, (b) 625, (c) 650, (d) 675, and (e) 700 °C. The mask pattern pitch a and mask opening diameter d_0 are 1.0 µm and 100 nm, respectively. The inset shows a top view of the nanowire

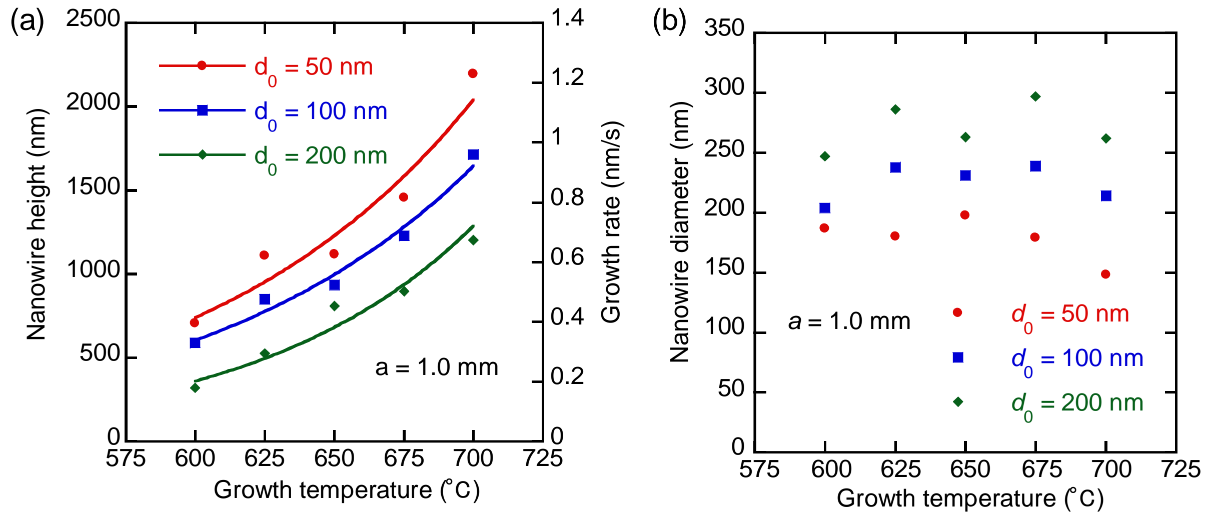

Fig. 4-3 Growth temperature dependence of (a) height and growth rate and (b) diameter of InGaAs nanowires for a = 1.0 μm.

at approximately 675–700 °C [**Figs. 4-2(d), (e)**]. We consider that the cause of the temperature dependence of the particle-like deposition is related to nucleation, migration, and desorption of the source materials at the SiO_2-patterned areas, which will be discussed in section 4.3.3. Arrays of hexagonal pillar-shaped nanowires grew from the mask openings on the patterned areas where the particle-like deposition were not observed, as shown in the SEM images in **Figs. 4-2(a)-(e)**, and nanowire height increased with increasing growth temperature.

The relationships of growth temperature with the height and growth rate of the nanowires for a = 1.0 μm were shown in **Fig. 4-3(a)**. Here, the height/growth rates of grown nanowires were plotted as a function of T_G. The height and growth rate of the nanowires clearly increased at higher temperatures and for smaller d_0 values. This can be explained by the enhanced surface migration and the incorporation of source materials into the nanowire crystal at higher temperatures. **Figure 4-3(b)** shows the diameters of nanowires for a = 1.0 μm and various d_0 values plotted as a function of growth temperature. The diameters of the nanowires for each d_0 appear to be roughly equal and independent of the temperature under this growth condition. On the other hand, the diameter increased by about 80–160 nm from the mask opening diameter d_0 of 50–200 nm and the amount of diameter increase showed no dependence on d_0.

4.3.2 Optical Characterization

Figures 4-4(a) and **4-4(b)** show PL spectra of InGaAs nanowires grown at 700 °C with d_0 = 50–300 nm, and a = 0.5 and 2.0 µm, respectively. The observed PL peak energies for the nanowires grown with a = 0.5 µm were 1.36–1.37 eV, but those for the nanowires grown with a = 2.0 µm were approximately 1.22–1.25 eV, as shown in **Figs. 4-4a)** and **4-4(b)**, respectively. The difference in the PL peak energies for a = 0.5 and 2.0 µm indicates that the Ga composition in the nanowires for a = 0.5 µm was higher than that for a = 2.0 µm. The PL intensities of the nanowires for a = 2.0 µm were relatively lower than those for a = 0.5 µm. We consider that the low peak energies caused by the sample structure, which made the total number of nanowires excited by the laser light one order of magnitude greater for a = 0.5 µm than for a = 2.0 µm. We find in **Fig. 4-4(b)** that the PL peak energy shifted slightly to a higher energy region as d_0 decreased from 300 to 50 nm. This indicates that the Ga composition increased by 1.7–2.3% as nanowire diameter decreased. However, we do not find any clear dependence of the PL peak energy shift on d_0 for a = 0.5 µm, as shown in **Fig. 4-4(a)**.

The PL spectra of nanowires grown at temperature of 600–700 °C are plotted in **Fig. 4-5**. The pattern pitch a and the mask opening diameter d_0 were 1.0 µm and 200 nm, respectively. The PL peak energy increased from 0.95 eV for nanowires grown at 600 °C to 1.31 eV for nanowires grown at 700 °C, indicating a strong dependence on growth temperature. Estimated Ga compositions of

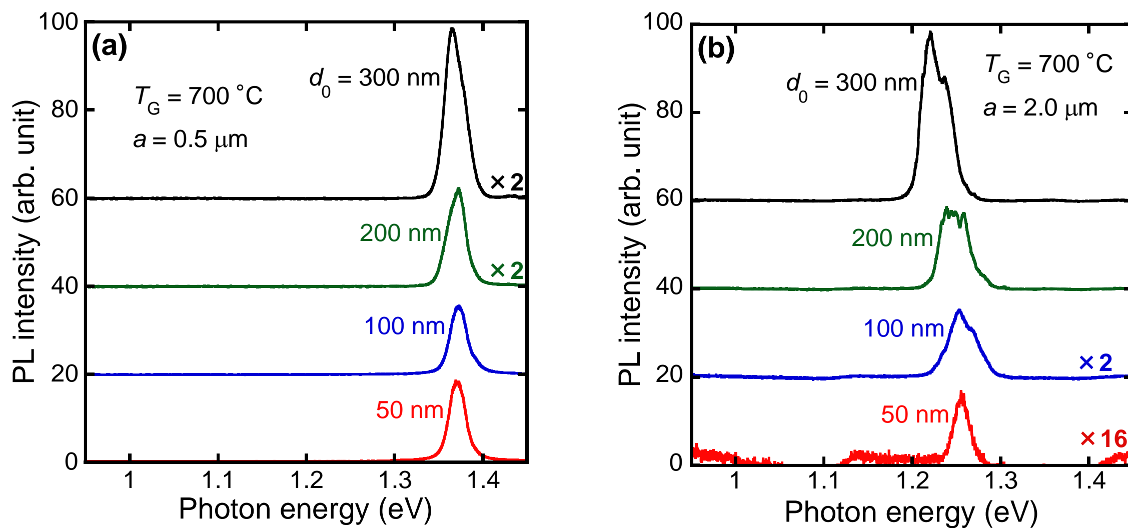

Fig. 4-4 µ-PL spectra for InGaAs nanowires measured at 4.2K. Spectra taken for pattern pitch of (a) 0.5 and (b) 2.0 µm. The base of each spectrum is shifted along the vertical direction for clarity.

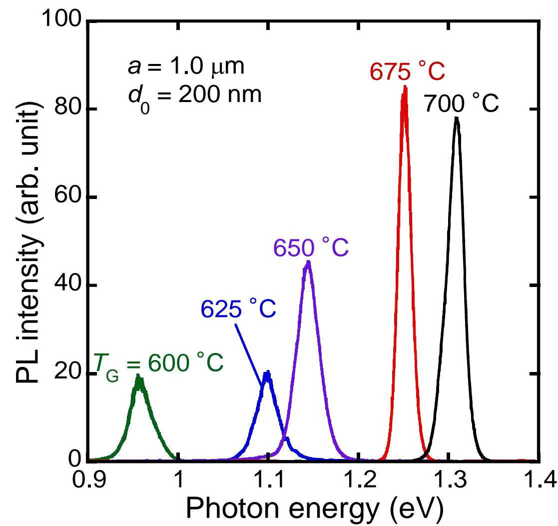

Fig. 4-5 μ-PL spectra for InGaAs nanowires grown at 600, 625, 650, 675, and 700 °C with a = 1.0 μm.

InGaAs nanowires are plotted in **Fig. 4-6**, where we applied linear approximation of the energy band gap between GaAs and InAs to obtain the atomic composition from the PL peak energy position [23].

The full widths at half maximum (FWHMs) of the PL spectra for the nanowires are also plotted in **Fig. 4-6**. We found that the Ga composition of the nanowires grown at 700 °C was nearly equal to the group III gas supply ratio, x_{supply} = [TMGa]/([TMGa]+[TMIn]), that is, 92%. The Ga composition decreased with decreasing growth temperature. However, FWHM increased with decreasing temperature. We speculate that the temperature dependence of FWHM in the PL spectra was caused by the effect of crystal alloying, which became marked owing to the increase in In composition from 10 to 40%, and the lattice mismatch between the grown InGaAs and the GaAs substrate increased with decreasing temperature.

4.3.3 GaAs and InAs Portions in InGaAs Nanowires

We confirmed that the increase in nanowire height with decreasing d_0 for each growth temperature was attributable to the collection of growth species in a mask opening area from the surrounding mask surface, and our results agreed with those reported by Ikejiri *et al* [15]. In addition, we consider that an As trimer on a GaAs(111)B surface may be related to the growth characteristic.

It was reported that the GaAs(111)B surface was partially covered by As trimers [24], and the coverage increased with decreasing growth temperature [25]. The increase in the coverage of As trimers on GaAs(111)B may hinder Ga atoms from being adsorbed onto the surface, causing a decrease in growth rate along the (111)B direction [26]. Our InGaAs nanowires grown at 700 °C have a Ga composition of up to 88%, as shown in **Fig. 4-6**; therefore, we consider that the growth characteristics are similar to those of GaAs nanowires. We consider that the decrease in growth rate with decreasing growth temperature may be due to the increased coverage of As trimers. Similar results were obtained for the mask pattern pitches of $a = 0.5$ and 2.0 μm.

From the growth temperature dependence of InGaAs nanowire height and atomic composition (**Figs. 4-3(a)** and **4-6**), we estimated portions for GaAs and InAs inside an InGaAs nanowire, as plotted by squares and diamonds, respectively, in **Fig. 4-7**. We found that the InAs portion was almost independent of temperature, but the GaAs portion decreased with decreasing temperature. It was reported that for GaAs nanowires grown on a GaAs(111)B substrate, the optimum growth temperature was about 750 °C [15] and the growth rate in the <111>B direction decreased with decreasing growth temperature owing to increased coverage of As trimers on the (111)B substrate [26]. Therefore, our result for the decreased height of the GaAs portion in the InGaAs nanowire with decreasing growth temperature agrees well with the model of GaAs nanowire growth on a GaAs(111)B substrate. Tomioka *et al.* found that the optimum growth temperature of InAs

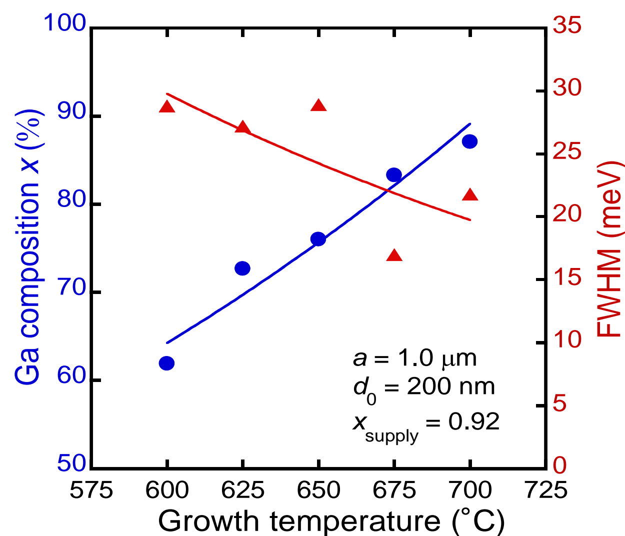

Fig. 4-6 Growth temperature dependence of Ga composition x in $In_{1-x}Ga_xAs$ nanowire and FWHM.

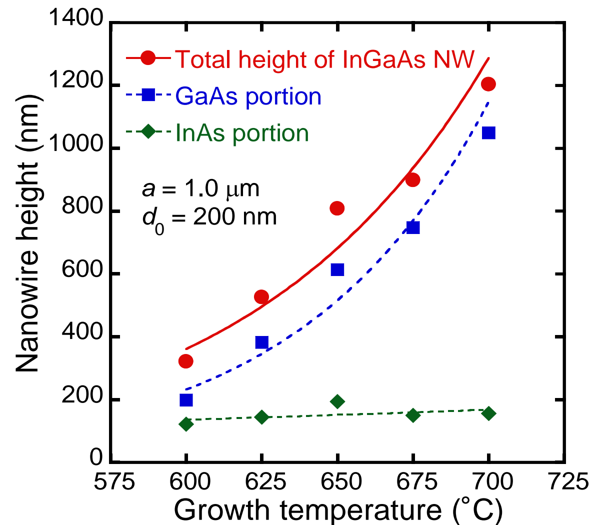

Fig. 4-7 Growth temperature dependence of GaAs and InAs portions in height and total InGaAs nanowire height for d_0 = 200 nm and a = 1.0 μm.

nanowires grown on an InAs(111)B substrate using SA-MOVPE was about 540 °C [27]. They argued that InAs nanowire growth was not hindered by As trimers, but was similar to planar InAs layer growth on InAs(001). The result for the InAs portion plotted in **Fig. 4-7** indicates that InAs nanowire growth was not affected by the formation of As trimers on (111)B. From this argument, we speculate that some amount of the source material to be consumed as the GaAs portion of the InGaAs nanowire might be changed to the particle-like depositions on the masked surface, as observed in the SEM images of **Fig. 4-2**.

We explained in §4.3.2 that the PL spectra of InGaAs nanowires grown at 700 °C with a pattern pitch of a = 2.0 μm shifted to a higher energy region by about 0.1 eV compared with those with a = 0.5 μm [**Figs. 4-4(a)** and **4-4(b)**]. This corresponds to the composition change of a 5% increase in Ga (5% decrease in In). We consider that this was caused by the increased mask area with increasing pitch, where the amount of indium evaporating from the mask surface is much larger than that of gallium [18]. Peak splitting or overlapping of multiple spectra can be seen in some PL spectra in Fig. 5(b). We consider that this may be caused by a small variation of InGaAs composition among 3–5 nanowires within the laser spot. On the other hand, no peak splitting or overlapping was observed for the InGaAs nanowires shown in **Fig. 4-4(a)**, where about 15 nanowires were irradiated by the excitation laser, so we consider that each spectrum was masked by the integration of many nanowires even if a small variation in composition occurred. Regarding the dependence of PL peak

energy on d_0, the mask opening diameter, the result showed a shift by about 30 meV to a higher energy region as d_0 decreased from 300 to 50 nm, as shown in **Fig. 4-4(b)**. This indicates that the smaller the nanowire diameter, the larger the Ga composition. When we look at the PL peak energies for a = 0.5 μm [**Fig. 4-4(a)**], we find no distinct dependence of peak energy on d_0 compared with that for a = 2.0 μm. We also find no clear dependence of PL peak energy on d_0 for a = 1.0 μm. We do not understand why there was no diameter dependence for a = 0.5 or 1.0 μm, but there was dependence for a = 2.0 μm. We require more detailed analysis with further experiments to clarify this.

4.4 Lattice mismatch growth

4.4.1 InGaAs Nanowires Grown on GaAs(111)B

Figure 4-8 shows SEM images of InGaAs nanowires grown using SA-MOVPE on a GaAs(111)B substrate with the SiO_2 mask pattern having pitch and opening diameter of 0.5 μm and 90 nm, respectively. A cross-sectional high-angle annular dark-field (HAADF) TEM image of a single nanowire indicates that it was grown without lateral growth onto the SiO_2 mask, as seen from

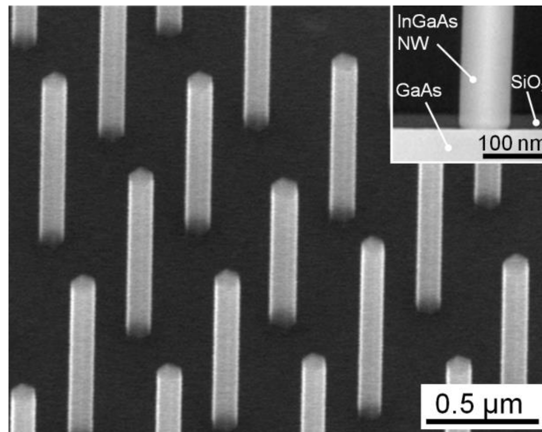

Fig. 4-8 45°-tilted view SEM image of InGaAs nanowire array. The mask pattern pitch a and the diameter d are 0.5 μm and 90 nm, respectively. The inset shows an HAADF-TEM image of the nanowire and GaAs substrate with SiO_2 mask pattern.

the close-up view in **Fig. 4-8**.

To examine the distribution of atomic content and crystal structure along the ternary alloy nanowire, we measured three portions of a 2-μm long nanowire. **Figures 4-9 (a)–(d)** show cross-sectional HR-TEM images of an InGaAs nanowire (90 nm in diameter) and locally magnified images at the top, middle, and bottom of nanowire, respectively. The corresponding SAED patterns are shown on the right side of the magnified HR-TEM images, **Figs. 4-9(e)–(g)**. We find that the hexagonal spot patterns in **Figs. 4-9(e)–(g)** indicate a zincblende structure and that there is no

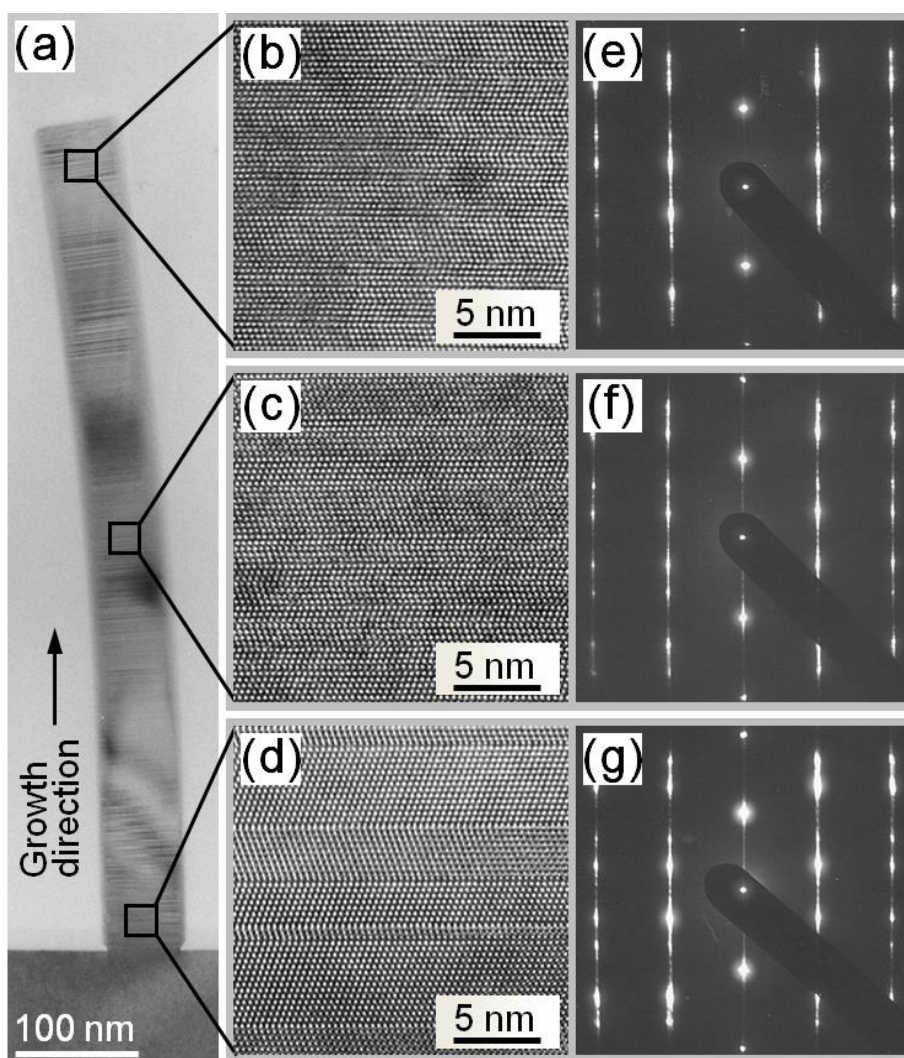

Fig. 4-9 (a) Cross-sectional TEM images of InGaAs nanowire 90 nm in diameter and locally magnified images at the (b) top, (c) middle, and (d) bottom of the nanowire. The corresponding SAED patterns at the (e) top, (f) middle, and (g) bottom of the nanowire.

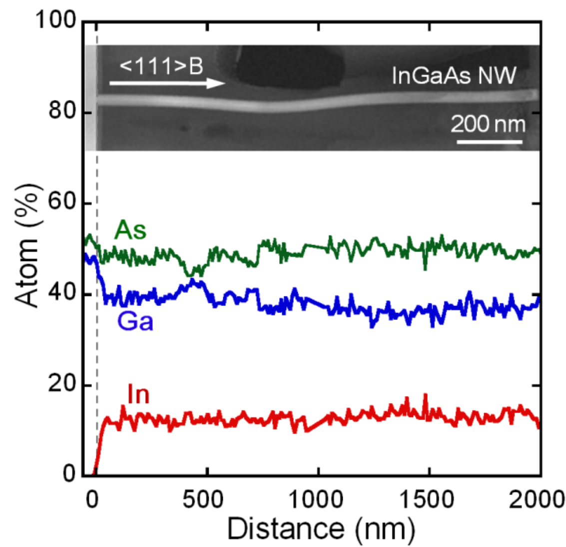

Fig. 4-10 Atomic content profiles for Ga, In, and As measured along an InGaAs nanowire by EDX. An HAADF-TEM image of the sample is posted above the profiles. The dashed line shows the interface between the nanowire and GaAs substrate.

wurtzite material anywhere from top to bottom except for the twin boundaries. The TEM images and the SAED patterns also show that the nanowire has rotational twins around the ⟨111⟩ axis as known from streak satellite spots found near the main spots (corresponding to the zincblende structure). The formation mechanism was discussed by Tomioka *et al*. for InAs nanowires [28] and by Yoshida et al. for GaAs nanowires [29]. Yoshida *et al*. argued that the density of rotational twins, that is, the frequency of rotational twins, along the ⟨111⟩ direction increased as the SiO_2 mask opening diameter was decreased. Tomioka *et al*. stated coexistence of zincblende and wurtzite segments with randomly stacked atomic layers in the very small transition thickness for the InAs nanowires with diameters ranging from 28 to 170 nm [29]. Their analyses also revealed that the frequency of rotational twins was not clearly dependent on the position along the nanowire. Our TEM measurements for the InGaAs nanowires with diameters of 60 nm and 90 nm showed that the twin frequency for the 60 nm diameter nanowire was higher than that for the 90 nm diameter nanowire. The dependence was similar to that reported by Yoshida *et al*. Thus we think that the formation mechanism of the rotational twins in the InGaAs nanowires is like that in GaAs nanowires.

Figure 4-10 shows atomic content profiles for As, Ga, and In obtained by EDX line-scans along the longitudinal direction of a nanowire, with a HAADF-TEM image posted above the profiles. The image shows that the nanowire is about 2 μm long and 60 nm in diameter and a bit curved near

the middle point. The deformation in the nanowire in **Fig. 4-9(a) or Fig. 4-10** was caused by the process of embedding it in resin. In **Fig. 4-10**, green, blue, and red lines represent atomic fraction profiles of elemental As, Ga, and In, respectively. The content ratio of In to Ga is about 26 to 74, as deduced from the profiles. Therefore, the lattice mismatch between the InGaAs nanowire and the GaAs substrate is approximately 1.9 %. The atomic content profiles in **Fig. 4-10** indicate that the group-III mole fractions are virtually constant along the 2-μm-long nanowire, which also indicates that the difference in migration length between In and Ga atoms on the sidewall facets has no effect on the longitudinal composition change in nanowires up to 2 μm. We think that the result is very important to fabricate lattice mismatched InGaAs nanowire devices, in which the atomic composition needs to be constant along the longitudinal direction of a nanowire.

4.4.2 Interface of Nanowire and Substrate

Figure 4-11(a) shows an HR-TEM image of a heterointerface between the InGaAs nanowire and GaAs substrate. The diameter and height of the nanowire are 90 nm and 950 nm, respectively. The lattice mismatch between the nanowire and the substrate is 2.1%, as estimated from the peak

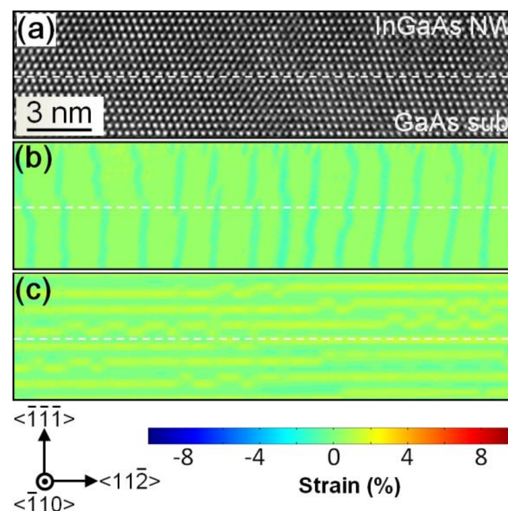

Fig. 4-11 (a) HR-TEM image at the interface between an InGaAs nanowire and the GaAs(111)B substrate. The white broken line shows the interface; (b) ε_{xx} and (c) ε_{yy} are two-dimensional strain maps calculated along the <-1-12> and the <-1-1-1> directions from image (a).

position of the μ-PL spectrum of nanowires (shown in **Fig. 4-12**). We calculated the displacements in the lattice image of the heterointerface and converted them into strain maps using the peak-pair finding method developed by Galindo *et al*. [30], who analyzed strain distributions around the interface of CdTe/GaAs. Our analysis is shown in **Figs. 4-11(b)** and **(c)**. **Figure 4-11(b)** describes two-dimensional strain fields ε_{xx}, whose $\boldsymbol{x}$ vector is parallel to the ⟨-1-12⟩ direction and **Fig. 4-11(c)** describes strain fields ε_{yy}, whose $\boldsymbol{y}$ vector is parallel to the ⟨-1-1-1⟩ direction, calculated from the displacement of the bright spots in the HR-TEM image. If misfit dislocations developed at the heterointerface, pairs of red-and-blue spots (the color indicating the magnitude of the localized compressive/tensile strain) at a dislocation could be observed on the strain map as described by Galindo *et al*. Tomioka *et al*. reported InAs nanowires grown on Si(111) and observed the pairs of red-and-blue spots corresponding to misfit dislocations at the interface using the peak-pair finding method [7]. The period was about 3 nm, caused by the lattice mismatch of 7% between InAs and Si. In the case of our wires, despite the lattice mismatch of as high as 2.1% (the period for misfit dislocations is estimated at 16.8 nm for total relaxation), no pair of red-and-blue spots was observed at the heterointerface as shown in **Figs. 4-11(b)** and **(c)**, suggesting no misfit dislocation. Our InGaAs nanowires grown on GaAs(111)B are well within the coherent growth range calculated by Glas [8]. It is thus stated that InGaAs nanowires as thick as 90 nm can be grown without defects, and therefore with good crystal quality over planar layers in heteroepitaxial growth.

4.4.3 Crystal Quality Comparison with Planar Growth

To gain more information about the difference in crystal quality between the nanowires and the planar lattice-mismatched epitaxial layers, we measured μ-PL as shown in **Fig. 4-12**. InGaAs nanowires used for the PL measurement were about 1 μm long and as thin as 90 nm and they were grown with a pitch of 0.5 μm. InGaAs planar layers grown on GaAs(111)B or GaAs(100) were about 0.3 μm thick. The crystal volume of the planar layer irradiated by the laser beam was assumed to be 20 times greater than that of nanowires. A strong peak with the full-width at half maximum of -19.3 meV was observed at 1.12 eV for the InGaAs nanowires, while the InGaAs planar layers grown on GaAs(111)B and GaAs(100) indicated no peak around 1.1 eV and only a weak band-edge emission peak from the GaAs(100) substrate at 1.5 eV. From the PL peak energy position, we

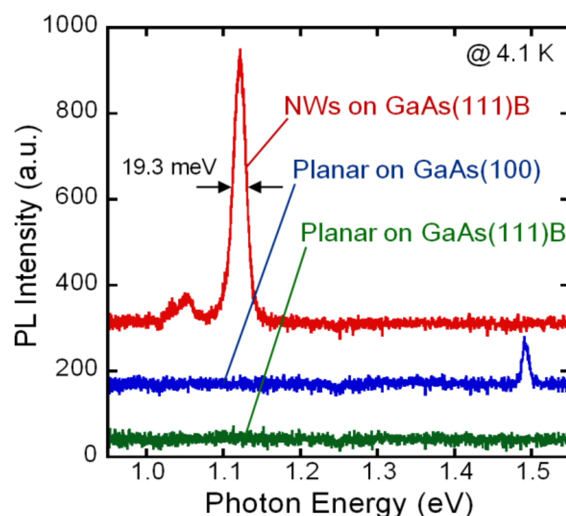

Fig. 4-12 PL spectra for InGaAs nanowires, InGaAs planar layers on GaAs(100), and (111)B substrate at 4.1K.

estimated the atomic content ratio of In to Ga (In/Ga) to be 26/74 in the nanowires. The ratios for the planar layers on GaAs(111)B and GaAs(100) substrates were 21/79 and 18/82 respectively, as determined by x-ray diffraction measurements. A crosshatch pattern caused by the lattice mismatch was observed by atomic force microscopy for the planar layer grown on GaAs(100). These results indicated that the heteroepitaxially grown nanowires under lattice-mismatched conditions were of better crystal quality than the planar layers used in this experiment.

4.5 Conclusion

We successfully fabricated highly uniform InGaAs nanowire arrays on GaAs(111)B substrates using SA-MOVPE. It was found that growth temperature strongly affected the growth characteristics of the InGaAs nanowires. In a low growth temperature range of 600–650 °C, particle-like depositions of 1–3 μm in diameter were observed on the patterned SiO_2 mask areas. However, the depositions decreased in size and density with increasing growth temperature, and highly uniform nanowire arrays without the depositions were grown at 700 °C. The heights and growth rates of the nanowires increased at higher growth temperatures, but the diameters of the nanowires for each mask opening diameter appeared to be roughly equal and independent of temperature. The PL peak

energy for the nanowires grown at 600 °C was 0.95 eV. This peak energy exhibited a blue shift with increasing growth temperature. We calculated the atomic composition of InGaAs nanowires from PL peak energy, which indicated that the Ga composition decreased with decreasing growth temperature. We estimated the volume portions of GaAs and InAs in the InGaAs nanowire and found that the InAs portion was constant between 600 and 700 °C, while the GaAs portion decreased as growth temperature decreased, which might be related to As trimers capped on GaAs(111)B and could be a cause of the particle-like depositions on the SiO_2 mask.

We investigated the effect of lattice mismatch on the crystal quality for InGaAs nanowires grown on GaAs(111)B substrates using SA-MOVPE. Nanowires with a lattice-mismatch of 2.1% were found to grow coherently on GaAs(111)B without misfit dislocations. A PL spectrum for the InGaAs nanowires grown on GaAs(111)B showed a strong band-edge emission peak at 1.12 eV, while InGaAs planar layers grown on GaAs(111)B or GaAs(100) exhibited no band-edge emission peak. This indicates that the crystal quality of the heteroepitaxially grown InGaAs nanowires was better than that of the planar layers, showing promise for fabricating heterostructure nanowire devices using a lattice-mismatched material system.

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Chapter 5 InP Core-Shell Nanowire Array Solar Cells

We demonstrate position-controlled III-V semiconductor nanowires by using selective-area metal-organic vapor phase epitaxy and their photovoltaic application. We grew a position-controlled and uniformly-shaped InP nanowire array. Power conversion efficiency of 4.23% was achieved for InP core-shell nanowire array solar cells. The devices showed a low reflectance without applying an anti-reflection coating and good short-circuit current density over the theoretical limit in a simple ray optics description. Furthermore, we analyzed a quantum efficiencies and dependence of the performance on the illumination intensity.

5.1 Introduction

Semiconductor nanowires have attracted much attention for use in future nanometer-scale electronic and optical devices, because they have small diameters and large surface areas that enable the fabrication of various kinds of functional devices through the use of *p-n* junction or heterojunction structures [1-4]. Moreover, in photovoltaic applications, a highly regular nanowire array has advantages of enhanced light absorption [5,6] and low-cost processing using fewer materials compared with conventional Si solar cells (**Fig. 5-1**). The nanowires of axial junction structure can realize misfit-dislocation-free heterojunction within several percent of lattice mismatch [7], and that of core-shell structure offer efficient carrier separation and collection at contact electrodes [8].

Typical approach to grow nanowires is based on a vapor-liquid-solid (VLS) growth method, which uses catalysts and liquid phase underneath metal particles for crystallization [1,9]. VLS-grown III-V compound semiconductor nanowires were investigated by Hiruma *et al* . in the early 1990s

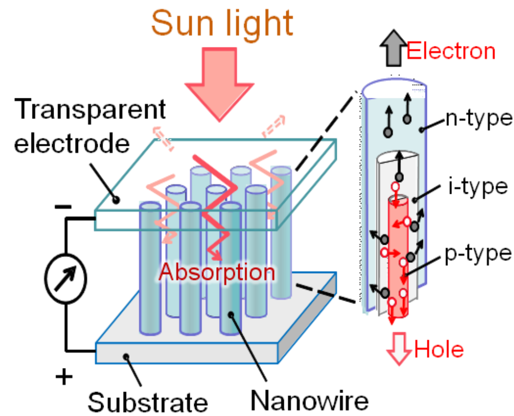

Fig. 5-1 Schematic view of core-shell nanowire array solar cell.

[10], and their publications have increased since early 2000s. This method can be used to synthesize almost all semiconductor materials through simple procedures [11-13]. However, it sometimes encounters difficulties in forming axial or/and core-shell heterojunction continuously with sharp interfaces, and problems of incorporation of metal-catalysts. In addition, it cannot grow position-controlled nanowires and fabricate the nanowire array uniformly. From these reasons, the VLS method is not suitable for device application, especially photovoltaic cells which required large area, uniformity, and sharp interface.

Another approach to grow nanowires is catalyst-free selective-area growth [14]. This method use amorphous thin film, such as SiO_2 and SiN_X, for confining the growth area, and enables the fabrication of nanostructures with sharp interface heterojunction structure without any catalysts. To fabricate the nanowire structure, it need to use of (111)A- or B-oriented substrates because its enables the formation of both inclined {110} facets and vertical {110} or {-211} facets. The formation of {-110] vertical facets on a (111)B-oriented substrate has been demonstrated by Fukui *et al*. [15], and then these structures were applied to laser and photonic crystals. This faceting growth approach can be applied to grow nanowires by using smaller mask openings [16]. The growth conditions and mechanism of III-V compound semiconductors nanowires by using selective-area metal organic vapor phase epitaxy (SA-MOVPE) have been reported in the past decade [17-19]. After that electric/optical device applications of the nanowires with good property which grown by using SA-MOVPE have been reported by Tanaka *et al*. and Tomioka *et al*. [20,21].

This growth method can expect to realize nanowire array solar cells which have excellent properties take advantage of the feature of nanowire array architecture. So far, many publications of

photovoltaic applications based on nanowires have been reported, but the nanowires mostly fabricated by VLS method and few uniformly nanowire array which is position-controlled. It is thus necessary to fabricate the position-controlled nanowire array solar cells and demonstrate the effects stem from the structure for realization of novel photovoltaic cells.

This chapter describes the fabrication of InP nanowire array solar cells by using SA-MOVPE and their photovoltaic application. Light and dark *I–V* measurements of the nanowire array solar cells were carried out at room temperature using a d.c. source meter and a xenon lamp with an AM1.5G filter. We discuss the light intensity dependence of solar cells parameters. In addition, external and internal quantum efficiencies in the wavelength range from 300 to 1000 nm were investigated with 10-nm resolution using an automated quantum efficiency measurement system

5.2 Experimental Procedure

The nanowires we report here were grown on patterned InP (111)A substrates partially covered with a SiO_2 mask. The SiO_2 patterns were designed to be a periodic triangular array of openings with a diameter of 120 nm and a pitch of 400 nm. SA-MOVPE growth of core-shell InP nanowires was carried out in a horizontal MOVPE system working at 0.1 atm, and the total flow rate of the gases was maintained at 5.75 standard liters per minute. Tertiarybutylphosphine (TBP) and trimethylindium (TMIn) were used as material sources, and diethylzinc (DEZn) and monosilane (SiH_4) were used as the *p*- and *n*-type dopants, respectively. After thermal cleaning at 580 °C in an atmosphere of H_2 and TBP, *p*-type InP core nanowires were grown for 8 min at 640 °C. *N*-type InP shell layers were then grown continuously for 15 min at 560 °C. For the core nanowires, the partial pressures of the TBP, TMIn, and DEZn were 8.1×10^{-5}, 4.4×10^{-6}, and 8.6×10^{-8} atm, and for the shell layers, the partial pressures of the TBP, TMIn, and SiH_4 were 1.6×10^{-4}, 4.4×10^{-6}, and 1.3×10^{-7} atm, respectively. Secondary ion mass spectrometry analysis of the thin film crystal grown outside the nanowire array revealed that the concentration of Zn in the *p*-type layer and of Si in the *n*-type layer were 6×10^{18} and 1×10^{18} atoms/cm^3, respectively.

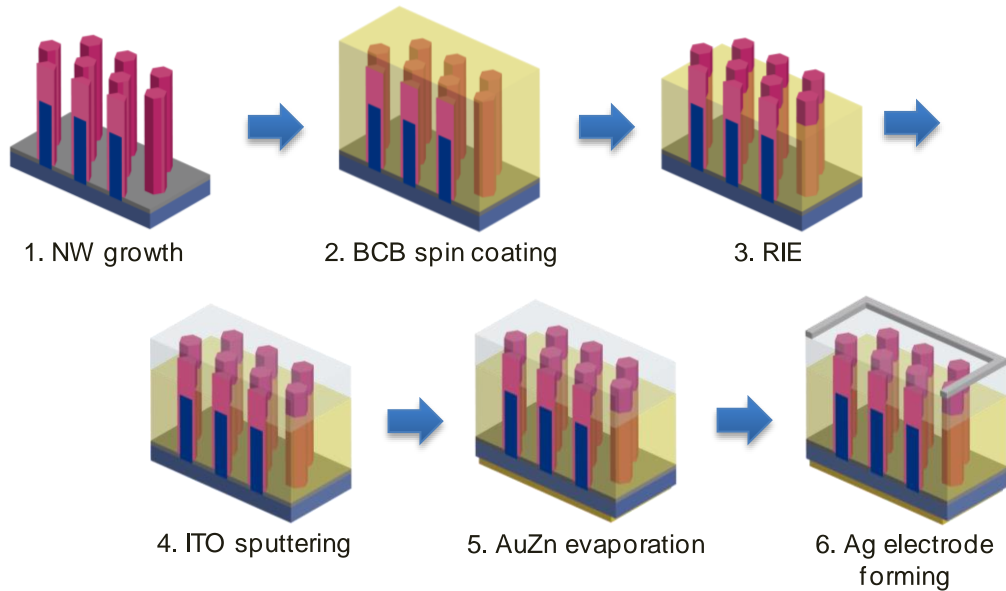

Fig. 5-2 Fabrication process of nanowire array solar cells.

As shown **Fig. 5-2**, for solar cell fabrication, the space between nanowires was filled by spin coating with benzocyclobutene (BCB) resin as a transparent electrical insulator. The excess overlaid resin was removed by reactive ion etching, and the areas that needed to be removed in order to expose the nanowire tips were defined by lithography. Then, a transparent indium tin oxide (ITO) electrode was sputtered onto the nanowire array at room temperature and annealed at 400 °C for 15 min. Finally, the backside electrode was formed by alloying Au-Zn, and the comb-shaped electrode on the front surface was formed by depositing Ag.

5.3 Growth of Core-Shell *p-n* InP Nanowires

Figure 5-3 shows 45°-tilted scanning electron microscopy (SEM) image of the grown InP core-shell nanowire array. We can see the position-controlled and uniformly-shaped InP nanowire array. An average height and a diameter of the grown nanowire were 1.2 μm and 180 nm, respectively. The average diameter of core InP nanowires was 135 nm and this was almost equal to that of the holes in the SiO_2 mask pattern on the substrate. From these results, thickness of the *n*-type shell layer was approximately 23 nm. A geometric fill factor (G_{FF}), which is a footprint of the

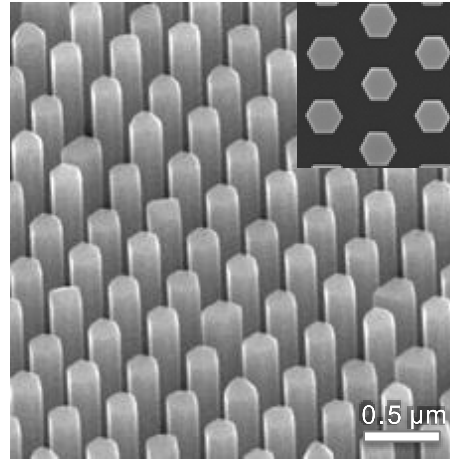

Fig. 5-3 45°-tilted SEM image of the grown InP core-shell nanowire array. Inset shows top view of the nanowire array.

nanowires, was approximately 0.203. The nanowires were grown vertically and had hexagonal <-211> facets, as shown in inset of **Fig. 5-3**. **Figure 5-4** shows absorption efficiency of the solar spectrum at AM1.5G (η_{abs}) versus InP thickness characteristics. The efficiency was calculated according to the following equation;

$$\eta_{\mathrm{abs}} = \int_{280}^{925} \left\{1 - \mathrm{e}^{-t \cdot \alpha_{\mathrm{InP}}(\lambda)}\right\} \cdot \frac{F_{\mathrm{ph}}(\lambda)}{F_{\mathrm{phInP}}} \cdot d\lambda \tag{5.1}$$

where t is the thickness of the InP, α_{InP} is the absorption coefficient of the InP, F_{ph} is the photon flux of the solar radiation at AM1.5G, and F_{phInP} is the total photon flux which is able to absorb fully in the InP. The integral range is set over bandgap of InP. The fabricated nanowires could absorb the incident light approximately 97%. The length of the nanowires was sufficient for absorption the incident light.

We fabricated a photovoltaic device using a grown core-shell *p-n* junction InP nanowire array. **Figure 5-5** shows a cross-sectional SEM image of a core-shell InP nanowire array solar cell. The gap between the nanowires was filled with the BCB, and the substrate and the ITO layer were separated completely by the BCB layer. The cause of uneven-shaped ITO layer is that there were great differences in heights of the nanowires and the BCB layer. The active area was 0.473 mm^2 as defined by using photolithography and reactive ion etching of BCB layer. The area contained the gap between the nanowires but excluded the grown nanowire area covered by BCB layer.

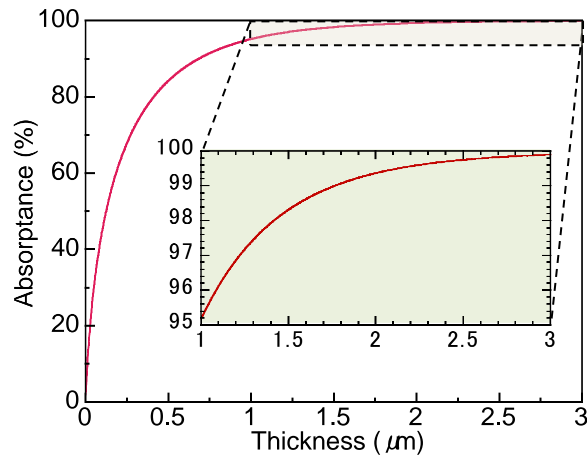

Fig. 5-4 Absorption efficiency of the solar spectrum at AM1.5G versus InP thickness characteristics. Inset shows the graph within a narrow thickness range from 1 to 3 μm.

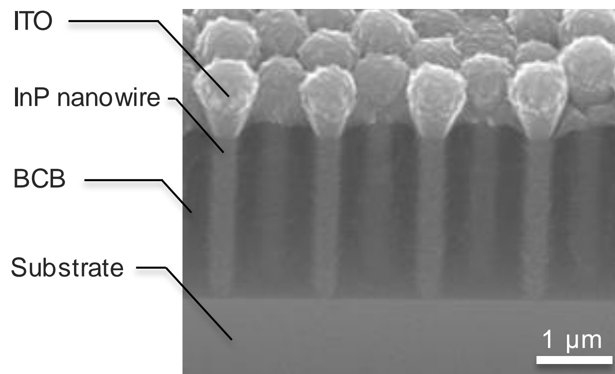

Fig. 5-5 Cross-sectional SEM image of a core-shell InP nanowire array solar cell.

5.4 Solar Cells Performances

Figures 5-6 plot the current density versus voltage (*J-V*) characteristics of the InP nanowire array solar cell in the dark and under air-mass 1.5 global (AM1.5G) illumination. The radiation intensity was calibrated using a reference cell module just before measurement. The device had good rectifying properties and a rectification ratio greater than 10^5 at ±1.2 V, which means that a leakage current was extremely low. An open circuit voltage (V_{OC}), a short circuit current density (J_{SC}), and a fill factor (*FF*) were 0.674 V, 11.1 mA/cm^2, and 0.585, respectively, as shown in **Fig. 5-6(b)**. From these figures of merit, an overall power conversion efficiency (η) was 4.23%. The J_{SC} is 31.9% of

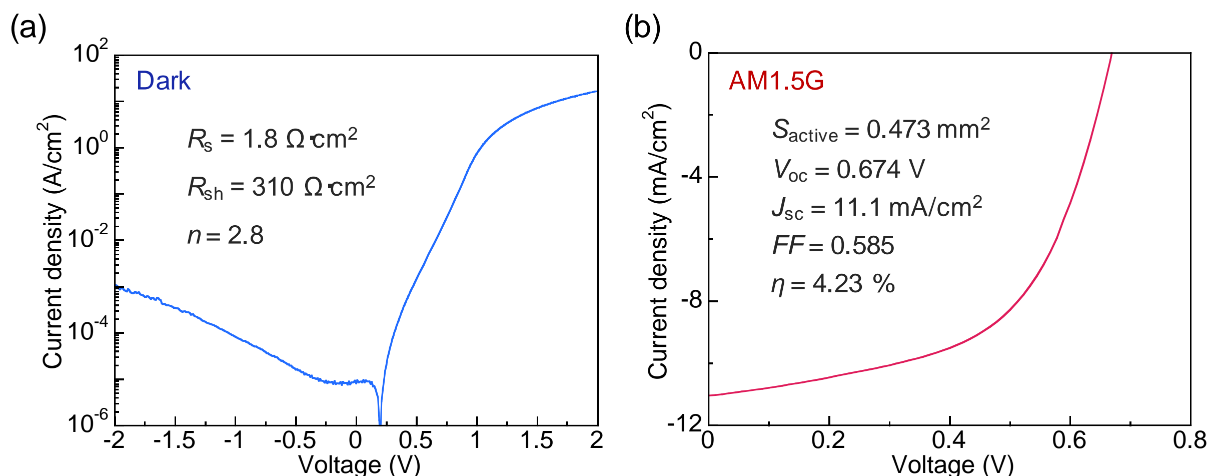

Fig. 5-6 Current density–Voltage characteristics of the InP nanowire array solar cell (a) in the dark and (b) under AM1.5G illumination.

the theoretical limit of InP cells that is 34.8 mA/cm^2 calculating from a solar spectrum data at AM1.5G supplied by National Renewable Energy Laboratory [22]. It means that the fabricated device demonstrated the enhancement of light absorption effect in nanowire array architecture, because the J_{SC} of the device exceed the maximum J_{SC} in the ray optics picture, 7.1 mA/cm^2 (20.3% of the theoretical limit). Thus, incident light that traveled between the nanowires was absorbed surrounding nanowires. The ideality factor, series resistance, and shunt resistance determined from the illuminated *J*-*V* characteristic were 2.8, 1.8 Ω·cm^2, and 310 Ω·cm^2, respectively.

To analyze the absorption properties, we investigated external quantum efficiency (EQE), internal quantum efficiency (IQE), and reflectance of the cell, as shown in **Fig. 5-7**. The reflectance was very low in the whole wavelength range despite having no any antireflection coating. This low reflectance results from the lower index of refraction in the nanowire array structure which was formed a stepped-index antireflection coating [23]. In the wavelength range between 700 and 820 nm, the IQE of the device was over 40% and was decreased with a shift to shorter wavelength. IQE curve was almost equal to the EQE due to the low reflectance. We consider that the low IQE may be caused by two reasons. First, the device did not employ a surface passivation for decreasing recombination rate and a window layer for rejecting carriers moving toward the surface and the front electrode. Second, the lateral thickness of shell layer was too thin to form a *p*-*n* junction. The thickness estimated from the SEM image was about 23 nm, which exceeded the depletion depth of

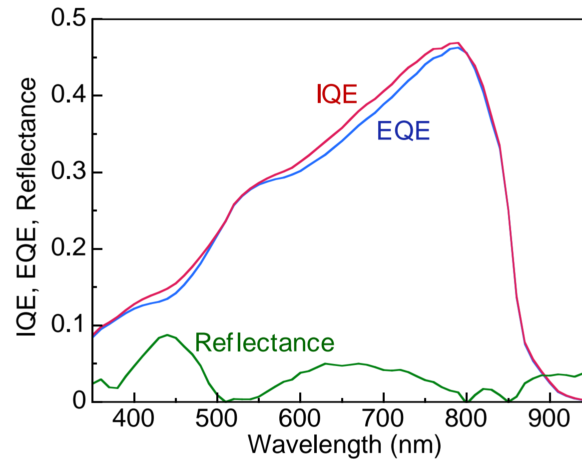

Fig. 5-7 EQE, IQE, and reflectance of the InP core-shell nanowire array solar cell.

~25 nm calculated based on carrier concentrations. Thus the charge carrier separation was not sufficient.

Next, we analyzed the dependence of the performance characteristics on the illumination intensity, as shown in **Figs. 5-8**. The intensity changed from 30 to 140 mW/cm^2. As expected, the J_{SC} showed liner increase with increased the intensity. This is because photocurrent is proportional to the photon flux. In contrast, the V_{OC} increased slightly from 0.64 to 0.73 V with increasing the light intensity from 30 to 140 mW/cm^2, because the V_{OC} is logarithmically proportional to the J_{SC}. The FF also increased slightly with increasing the intensity due to the increase of the V_{OC} and low series resistance. Through the increase of V_{OC} and FF with increased the intensity, the device efficiency increased slightly with increased the intensity. These dependence results in line with expectations mean that the fabrication process of the nanowire array solar cells was successful and the device was well functioning which is based on a solid state semiconductor physics.

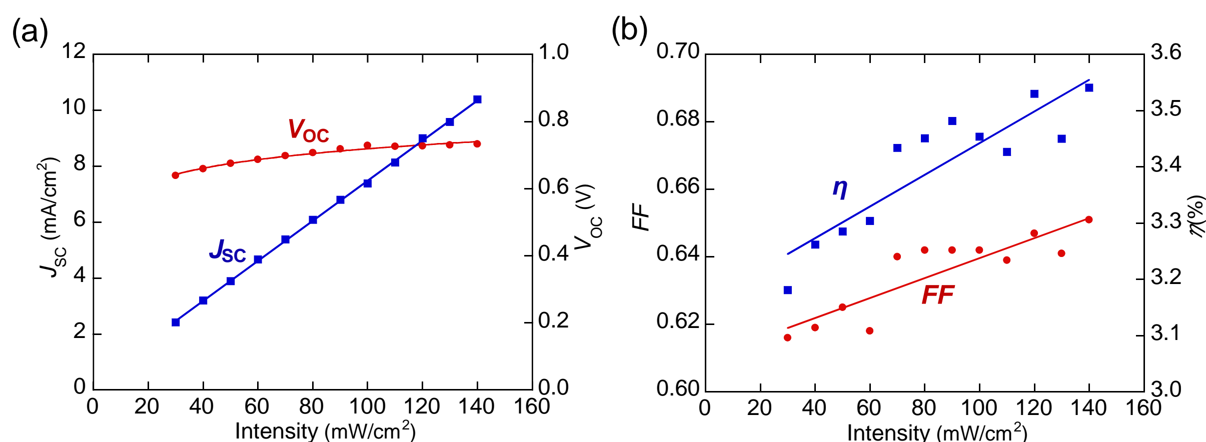

Fig. 5-8 Illumination intensity dependence of the (a) V_{OC}, J_{SC}, (b) *FF*, and η in the InP core-shell nanowire array solar cell.

5.5 Conclusion

In conclusion, we demonstrated a growth of position-controlled InP nanowire array by using SA-MOVPE and their photovoltaic application. The fabricated device showed good rectification properties and photovoltaic performance. It exhibited a η of 4.23% under AM1.5G with a V_{OC} of 0.674 V, J_{SC} of 11.1 mA/cm^2, and *FF* of 0.585. The periodic nanowire array solar cells demonstrated the light absorption enhancement effect by low reflectance obtained without applying anti-reflection coatings and absorption of incident light that traveled between the nanowires. Furthermore, we analyzed the dependence of the performance characteristics on the illumination intensity and confirmed that the device was well functioning which is based on a solid state semiconductor physics. Although a number of issues remain to get higher conversion efficiency, the results reported here represent the potency and the capabilities of the nanowire-array-based solar cells.

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Chapter 6 InP/AlInP Core-Multishell Nanowire Array Solar Cells

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We report surface-passivated core-shell InP nanowire array solar cells fabricated using catalyst-free selective-area metal organic vapor phase epitaxy. Reflectance measurements confirm enhanced light absorption due to significantly reduced reflectance over a wide spectral range. The wide-band-gap outer shell layer of core-multishell nanowires effectively passivates the large surface area of the nanowires, increasing the short-circuit current density and elevating the energy conversion efficiency by 6.35% under AM1.5G illumination. This passivation technique could open a new approach to nanowire-based photovoltaics with higher energy efficiency.

6.1 Introduction

Semiconductor nanowires are promising materials for next-generation photovoltaic devices, and periodical array architecture is expected to enhance energy efficiency while keeping manufacturing costs low [1-8]. The periodic nanowire array structure is potentially able to enhance optical absorption by reducing optical reflectance [9-11]. Moreover, solar cell array elements with core-shell structure are potentially advantageous with regard to the efficiency of charge collection because of the radial junction structure due to their cylindrical geometry [12]. Core-shell nanowire array solar cells have nonetheless shown poor short-circuit current density J_{SC} [2,4-7]. Additionally, the J_{SC} = 24.6 mA/cm^2 of the best reported InP nanowire cell with 13.8% efficiency [1] was still 71% of the theoretical limit 34.5 mA/cm^2, and hence improvement of the J_{SC} is important to increase efficiency. The reason for decreasing J_{SC} is thought to be the high surface recombination due to the high surface–to-volume ratio of nanowires [13]. It is well known that J_{SC} and conversion efficiency

improvements could be achieved by using surface passivation due to the reduction in surface recombination [14,15].

We have reported that high-quality nanowires can be grown by catalyst-free selective-area metal organic vapor phase epitaxy (SA-MOVPE) using a mask substrate [6]. The advantages of this method are that the nanowire position and diameter are controlled by adjusting the mask design and that we can form both lateral and axial heterostructures by controlling the growth conditions appropriately [16]. This SA-MOVPE method can therefore be used to make nanowire solar cells [6,17,18], nanowire field-effect transistors [19], and nanowire light-emitting diodes [20]. In this study, we experimentally demonstrate surface passivation and improvement conversion efficiency of core-shell InP nanowire solar cells using catalyst-free SA-MOVPE.

6.2 Experimental Procedure

The nanowires we report here were grown on patterned InP (111)A substrates partially covered with a SiO_2 mask. The SiO_2 patterns were designed to be a periodic triangular array of openings with a diameter of 120 nm and a pitch of 400 nm. SA-MOVPE growth of core-shell InP nanowires was carried out in a horizontal MOVPE system working at 0.1 atm, and the total flow rate of the gases was maintained at 5.75 standard liters per minute. Tertiarybutylphosphine (TBP) and trimethylindium (TMIn) were used as material sources, and diethylzinc (DEZn) and monosilane (SiH_4) were used as the *p*- and *n*-type dopants, respectively. After thermal cleaning at 580 °C in an atmosphere of H_2 and TBP, *p*-type InP core nanowires were grown for 10 min at 630 °C. *n*-type InP shell layers were then grown for 15 min at 470 °C. For the core nanowires, the partial pressures of the TBP, TMIn, and DEZn were 6.5×10^{-5}, 2.7×10^{-6}, and 8.6×10^{-8} atm, and for the shell layers, the partial pressures of the TBP, TMIn, and SiH_4 were 4.9×10^{-4}, 2.7×10^{-6}, and 1.3×10^{-7} atm, respectively.

As shown **Fig. 6-1**, for solar cell fabrication, the space between nanowires was filled by spin coating with benzocyclobutene (BCB) resin as a transparent electrical insulator. The excess overlaid resin was removed by reactive ion etching, and the areas that needed to be removed in order to expose the nanowire tips were defined by lithography. Then, a transparent indium tin oxide (ITO) electrode was sputtered onto the nanowire array at room temperature and annealed at 400 °C for 15

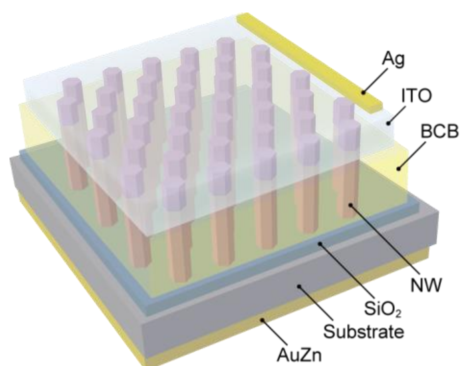

Fig. 6-1 Schematic illustration of an InP nanowire solar cells.

min. Finally, the backside electrode was formed by alloying Au-Zn, and the comb-shaped electrode on the front surface was formed by depositing Ag.

6.3 Growth of InP/AlInP Core-Multishell Nanowires

As shown in the scanning electron microscopy (SEM) image in **Fig. 6-2**, a highly uniform array of hexagonal nanowires 1.45 μm high and 190 nm in diameter was formed on the mask substrate. The average diameter of the core nanowires with hexagonal {-211} facets was 120 nm, equal to the hole diameter of the SiO_2 mask pattern on the substrate, so the shell layer was 35 nm

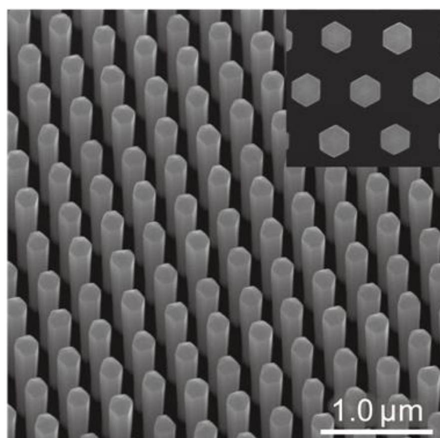

Fig. 6-2 Typical SEM image showing selective-area growth of InP nanowire array on InP(111)A substrate

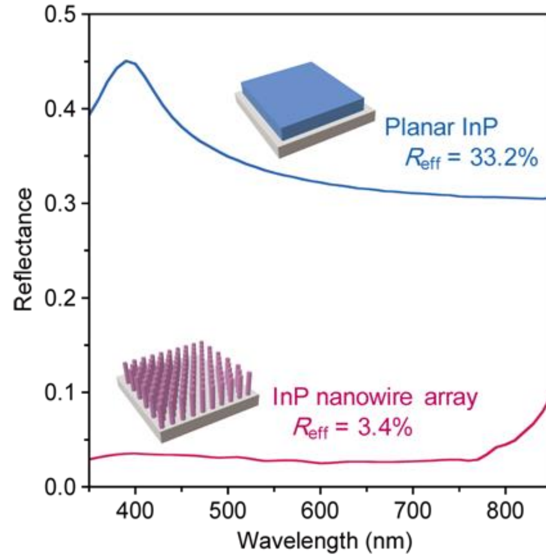

Fig. 6-3 Measured reflectance properties of InP nanowire array and planar substrate. Insets are schematic images of a nanowire array and a planar InP substrate.

thick. The geometric fill factor ff_{NW}, defined as the ratio between the footprint area of the nanowires and the area of the unit cell, was 0.24. It is important to note that selective-area electron diffraction patterns indicated that the nanowires grown this way had a single-crystalline wurtzite structure without stacking faults. The reflectances of the InP nanowire cell array and a reference planar cell are shown in **Fig. 6-3**. To evaluate the array's overall reflectance in the solar spectrum, we calculated the effective reflectance [21]:

$$R_{\mathrm{eff}} = \int_{350}^{850} R(\lambda) \cdot J_0(\lambda) \cdot d\lambda \Big/ \int_{350}^{850} J_0(\lambda) \cdot d\lambda \tag{6-1}$$

where R is the reflectance, and J_0 is the photon flux of the solar spectrum under Air Mass 1.5 global (AM1.5G) illumination. The R_{eff} of the nanowire array is 3.4%, which is one-tenth that of the planar cell (33.2%). The nanowire array can be modeled as a series of thin films with graded refractive index [22], and a model based on an effective medium approximation indicates significantly suppressed reflectance [9]. A very small reflectance over this wide spectral range can be achieved using a planar cell only if a sophisticated texture structure with added special antireflection coatings is used [23-25].

6.4 Solar Cells Performances

Next, we characterized the performance of these InP nanowire solar cells. The current density-voltage characteristic measured under simulated AM1.5G illumination (100 mW/cm^2) at room temperature is shown in **Fig. 6-4**, where the current densities correspond to the active areas of the cells (800 × 800 μm^2). The illumination intensity was calibrated using a standard silicon photodiode (BS-500, Bunkoukeiki). The cell has an open-circuit voltage V_{OC} of 0.365 V, a J_{SC} of 17.3 mA/cm^2, and a fill factor FF of 0.567, for an overall efficiency of 3.59%. Despite the ff_{NW} of 0.24, the cell has a J_{SC} better than that of previously reported nanowire solar cells [6]. The V_{OC}, however, is lower than that of the best InP planar solar cell that has been reported [26] because the interfacial recombination makes the reverse saturation current density J_0 large, 10 $\mu A/cm^2$, and the ideality factor n high, 2.0. One sees in **Fig. 6-5** that the nanowire solar cell, like the as-grown InP nanowire array, has low reflectance even though it does not have specially designed antireflection coatings. The internal quantum efficiency (IQE) in the mid-range of the sunlight spectrum (550–800 nm) is about 60%, which is lower than that of a planar InP solar cell. This relatively low IQE is probably due to the high surface recombination loss stemming from the high surface–to-volume ratio of the nanowire array.

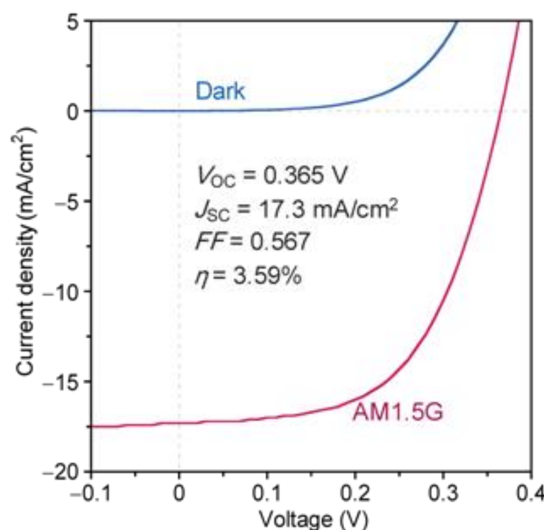

Fig. 6-4 Current density–Voltage characteristic of the nanowire array solar cells under 1-sun illumination (AM1.5G) and in the dark.

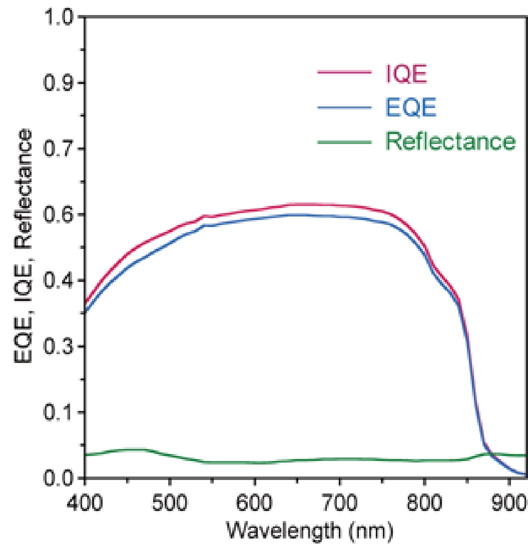

Fig. 6-5 Measured reflectance, EQE, and IQE of the nanowire array solar cells.

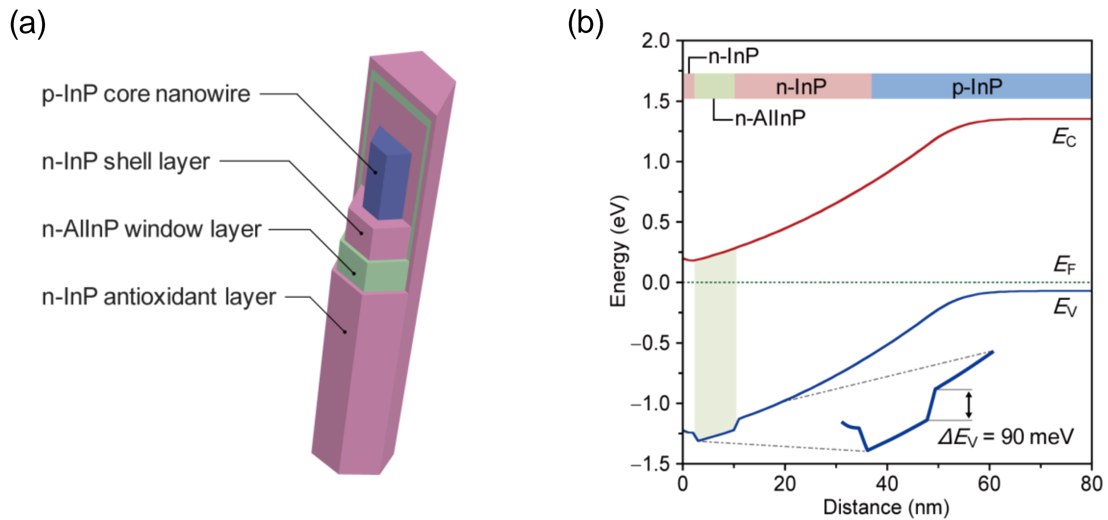

Fig. 6-6 (a) Structure of the CMS nanowire. The *p*-InP core nanowire is wrapped with *n*-InP/*n*-AlInP/*n*-InP multilayers. (b) Band diagram for CMS nanowire solar cells under open-circuit condition (simulated using the one-dimensional Poisson equation). The Fermi level, conduction band minimum, and valence band maximum are denoted by E_F, E_C, and E_V, respectively.

We then designed and fabricated a passivated InP nanowire structure, one with p-InP/n-InP/n-AlInP/n-InP core-multishell (CMS) nanowires, intended to improve the internal quantum efficiency [**Fig. 6-6(a)**]. A nanowire-array structure has a larger surface area than a planar structure, which makes reducing surface recombination more important for improving the conversion efficiency.

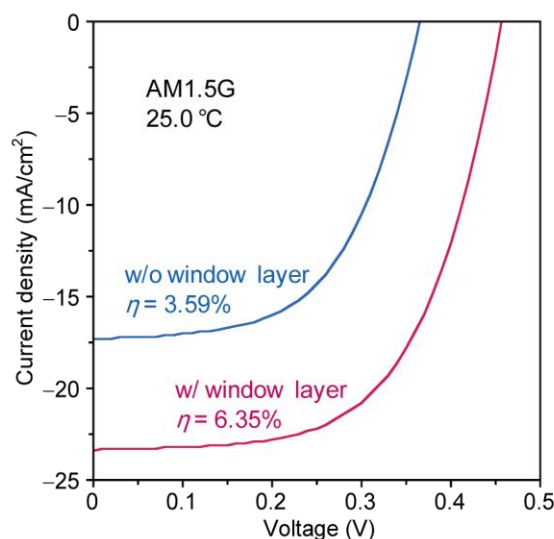

Fig. 6-7 Current density–Voltage characteristics of InP nanowire array solar cells with and without the AlInP window layer under AM1.5G illumination.

Window layers of ternary alloys such as InGaP, AlGaAs, and AlInP have not been used for surface passivation in InP solar cells because of the difficulty in their uniform epitaxial layer growth. Furthermore, there has been no report on the passivation of n-InP solar cells by using a hetero-epitaxial window layer because no lattice-matched wide-band-gap materials are available. Here, we focused on AlP, which according to the model-solid theory [27], has a conduction-band level almost equal to that of InP and has valence-band offset with InP of 1.0 eV. Although AlP is lattice-mismatched with InP ($\Delta a/a = -6.90\%$), AlInP that functions as a window layer can be grown on InP when the Al composition is over 3% and the layer thickness is less than the critical thickness. The band diagram of the CMS nanowire was calculated using the one-dimensional Poisson equation [28] and is shown in **Fig. 6-6(b)**, where one sees that a valence-band potential barrier of 90 meV is formed only at the interfaces between the *n*-$Al_{0.05}In_{0.95}P$ window layer and the *n*-InP shell layer. The potential barrier acts like a mirror reflecting minority carriers in the valence band of the *n*-InP shell layer; thus, surface recombination is reduced. The thicknesses of the *n*-InP shell layer, *n*-AlInP window layer, and outermost *n*-InP layer were about 30, 6, and 2 nm, respectively. The outermost n-InP layer is a cap intended to prevent the oxidation of the AlInP layer. The *n*-AlInP layer was 5% Al, the *n*-InP/*n*-AlInP/*n*-InP layers had a Si concentration of 9×10^{17} atoms/cm^3, and the *p*-InP layer had a Zn concentration of 3×10^{18} atoms/cm^3. These values were estimated from secondary ion mass spectrometry analysis of reference thin film samples in the same growth run. **Figure 6-7** shows the

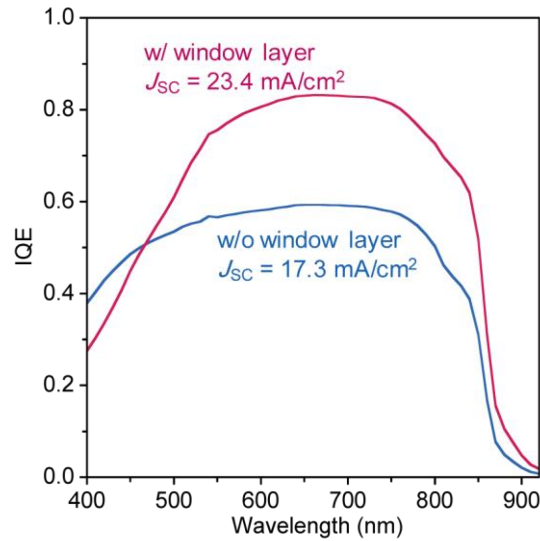

Fig. 6-8 IQE characteristics of InP nanowire solar cells with and without the AlInP window layer.

device performance of CMS nanowire solar cells with and without the window layer. The device with the window layer has an excellent J_{SC} of 23.4 mA/cm^2, a V_{OC} of 0.457 V, and a *FF* of 0.596 (for an overall conversion efficiency of 6.35%), which are higher than those of previously reported nanowire solar cells [6]. The J_{SC} of the CMS nanowire solar cells is close to 80% that of the best InP planar solar cell reported [24], even though their absorption volume is only 8% of the total epitaxial layer thickness of the best planar cell (3.5 µm).

At all wavelengths above 450 nm, the IQE of the CMS nanowire solar cell with the window layer was greater than that of the one without the window layer [**Fig. 6-8**]. This improvement indicates that the AlInP window layer reduces the surface recombination. It seems reasonable to assume that the increased IQE for long wavelengths indicates reduced recombination at the side surfaces of the nanowires, since long-wavelength light is absorbed in the deep region. The decreased IQE at short wavelengths was caused by absorption at the top part of the n-InP anti oxidant layer and n-AlInP window layer, which can probably be decreased by reducing the thicknesses of these layers.

6.5 Conclusion

In summary, we have developed a method of fabricating position-controlled InP nanowire arrays by using catalyst-free SA-MOVPE. Some advantages of this method using an opening mask are that it is a catalyst-free process, is position-controlled, and reduces material wastage. The highly periodic nanowire solar cells reported here demonstrate light absorption enhanced by extremely low reflectance obtained without using anti reflection layers. Furthermore, reducing surface recombination by using a lattice-mismatched AlInP window layer to passivate the n-InP shell layer, we were able to fabricate an array of nanowire solar cells that have a J_{SC} much better than that of previously reported nanowire solar cells. Although it is necessary to optimize both electrical properties of the nanowire and optical properties of the array to improve overall device efficiency, these results represent important progress in the fabrication of nanowire-array-based solar cells.

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Chapter 7 ITO/*p*-InP Heterojunction Nanowire Solar Cells

Heterojunction solar cells were formed with a position-controlled InP nanowire array sputtered with indium tin oxide (ITO). The ITO not only acted as a transparent electrode but also as forming a photovoltaic junction. The devices exhibited an open-circuit voltage of 0.436 V, short-circuit current of 24.8 mA/cm^2, and fill factor of 0.682, giving a power conversion efficiency of 7.37% under AM1.5G illumination. The internal quantum efficiency of the device was higher than that of the world-record InP cell in the short wavelength range.

7.1 Introduction

Photovoltaic devices based on semiconductor nanowire arrays have drawn interest as a possible way of reducing costs and materials while maintaining the power conversion efficiency of solar cells [1-5]. A size- and position-optimized array of nanowires can absorb an amount of light almost equal to that of a bulk structure with an antireflection coating because of its near-field-optics enhanced absorption and anti-reflection effect [6,7]. However, photovoltaics based on nanowire arrays need to have a transparent electrode put on their nanowires before the collecting electrode is formed, because each nanowire independently functions as a solar cell. In many cases, indium tin oxide (ITO) has been used as the transparent electrode since it has high conductivity and transmittance [1-4,8]. We have focused on the ITO because it can act not only as a transparent conductive oxide but also as forming a photovoltaic junction with groups IV and III-V semiconductors [9-11]. In particular, it has been reported that an ITO/InP planar solar cells have a power conversion efficiency of 18.9% [11]. This suggests the possibility of making less costly ITO/ nanowire-array heterojunction solar cells that require only a single-doped nanowire array. Moreover,

the use of one doped nanowire growth layer instead of two would give us more control over the crystal growth conditions [12].

In this study, we experimentally demonstrated an ITO/InP heterojunction nanowire array photovoltaic device. The *p*-doped InP nanowire array was epitaxially grown using selective area growth (SAG), which has the capability of position control. Photovoltaic junctions were formed by ITO sputtering on the *p*-InP nanowire array. The resulting heterojunction nanowire-array cell had low reflectance and excellent quantum efficiency in the short wavelength region.

7.2 Experimental Procedure

The nanowire growth and the fabrication process for the nanowire array solar cells were as previously reported [13]. We grew *p*-type InP nanowires by selective-area MOVPE using a 20-nm-thick SiO_2 mask deposited onto *p*-type InP (111)A substrates ($N_A \sim 5 \times 10^{18}$ cm^{-3}). The SiO_2 pattern was designed to be a triangular periodic array of openings with a diameter, d_0, of 200 nm and pitch, a, of 400 nm in 1.2×1.2 mm^2 regions. The nanowires were grown using metal-organic vapor phase epitaxy. After the growth, the nanowire array was embedded by spin-coating benzocycrobutene (BCB, Dow Chemical). The BCB layer was etched by reactive ion etching (RIE) with CF_4/O_2, exposing the tips of the nanowires. A transparent ITO (SnO_2/In_2O_3 10:90 wt %) layer was then rf sputtered at a rate of 1.1 Å/s for 45 min onto the nanowire array at room temperature and annealed in N_2 at 400 °C for 15 min. The sputtered ITO film typically has a sheet resistance of 10 Ω/□ and an optical transmittance higher than 85% in the wavelength range between 400 nm and 900 nm. U-shaped Ag and alloying Au-Zn electrodes were respectively formed on the ITO layer and back of the substrate. The active device area was 0.62 mm^2 and included approximately 4.5×10^6 nanowires.

7.3 Solar Cells Performances

Figure 7-1(a) shows 20°-tilted scanning electron microscopy (SEM) image of *p*-InP nanowires grown on patterned *p*-InP(111)A substrates. The nanowires were well-defined and highly

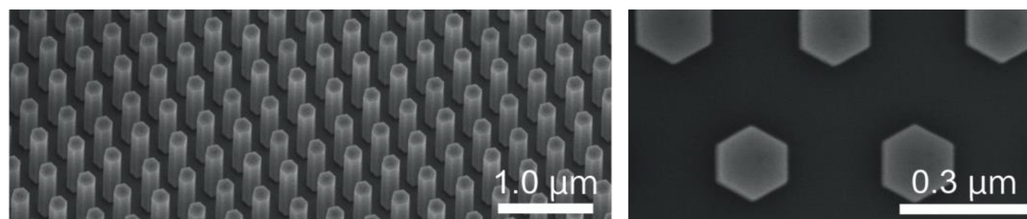

Fig. 7-1 (a) 20°-tilted view SEM image of *p*-InP nanowire array. (b) A top view SEM image of the nanowires.

uniform in length, diameter, shape, and position. The sidewalls of the hexagonal nanowire were {-211} facet surfaces vertical to the substrate, as shown in **Fig. 7-1(b)**. The average height and diameter of nanowires were 1.0 μm and 170 nm, respectively. The geometric fill factor, i.e., the ratio between the footprint area of the nanowire and the area of the unit cell, was 18%. The SEM image in **Fig. 7-2** shows a cross-section of the nanowires after completion of the device processes. The sputtered ITO layer had a dome-shaped morphology, which functioned as a light coupling within the nanowire array [14].

Figure 7-3(a) shows the current density versus voltage (*J*–*V*) characteristics of the fabricated ITO/*p*-InP heterojunction solar cell. They were measured under AM1.5G (1 sun) illumination at 25.0 °C. The illumination intensity was calibrated using a standard silicon photodiode (Bunkoukeiki BS-500). **Figure 7-3(b)** shows the *J*–*V* characteristics of the cell in the dark. The device had good rectifying properties and a rectification ratio greater than 10^4 at ±1.0 V in the dark, which means that a photovoltaic junction formed in it. These rectification properties can be attributed to SAG, which guarantees high crystal quality by preventing any metal from being incorporated during epitaxial

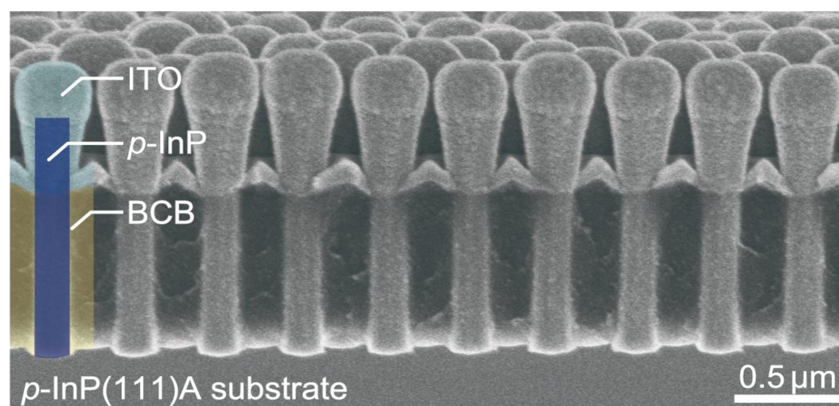

Fig. 7-2 Cross-sectional SEM image of ITO/*p*-InP heterojunction nanowire solar cell.

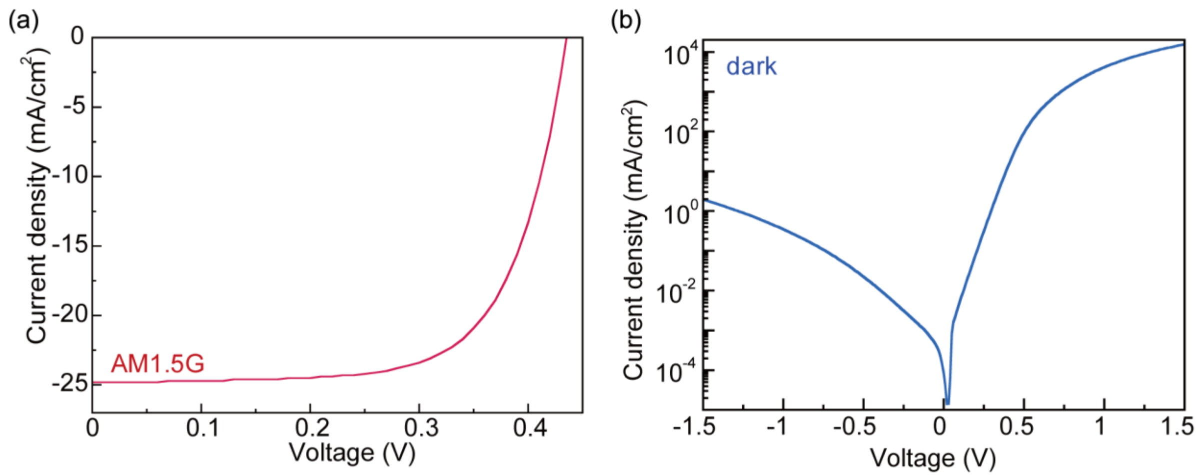

Fig. 7-3 (a) Illuminated (AM1.5G) and (b) dark *J-V* characteristic of the ITO/*p*-InP nanowire cell.

growth [15]. There are several models that could be used to explain the behavior of the ITO/*p*-InP junction, including heterostructure, buried n^+/p homojunction [16], metal-insulator-semiconductor [17], and metal-semi-insulating-semiconductor [18], but the buried n^+/p homojunction model is compelling because the deposition of an ITO layer induces an n^+-defect layer near the surface [16].

The device exhibited an open circuit voltage (V_{OC}) of 0.436 V, a short circuit current density (J_{SC}) of 24.8 mA/cm^2, and a fill factor (FF) of 0.682, for an overall power conversion efficiency (η) of 7.37%. The current density and efficiency were determined from the active area, 82% of which was the space between the nanowires. This high J_{SC} for a nanowire-array-based device resulted from the combination of near-field-optics enhanced absorption and anti-reflection effects [7]. The ideality factor and series resistance determined from the illuminated *J-V* characteristics [19] were 1.6 and 0.21 Ω·cm^2.

To analyze the absorption properties, we investigated the quantum efficiency of the heterojunction cell, as shown in **Fig. 7-4**. In the wavelength range between 370 nm and 730 nm, the internal quantum efficiency (IQE) of the device exceeded 80%, despite the device covering only 18% of the substrate surface. The IQE at shorter wavelengths was much higher than the previous reported InP nanowire solar cell [13], and the device had peak IQE of 0.943 at 490 nm without employing a window layer for reflecting minority carriers moving toward the front ITO layer. Moreover, the IQE of our heterojunction cell was significantly greater than that of the current world record holder for InP planar cells [20] in the range of 300 nm and 570 nm. There were two reasons for this. First, the wide-band-gap ITO layer functioned as a window layer, which reflects minority carriers, for the InP layer; thus, IQE increased because of a reduction in the amount of surface

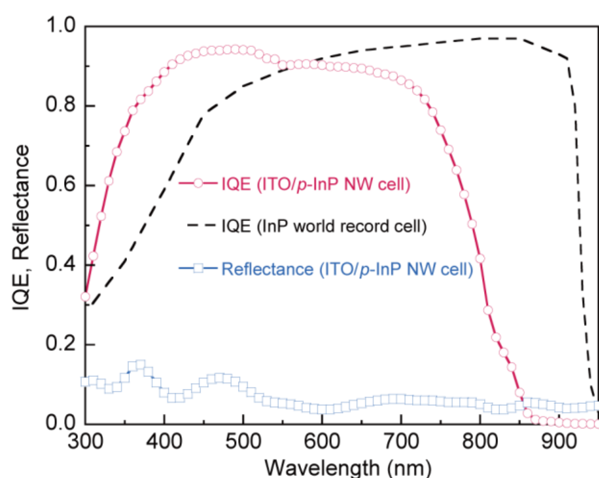

Fig. 7-4 Internal quantum efficiency and reflectance of ITO/p-InP nanowire cell. It is compared with the IQE of the InP-world record planar cell reported in Ref. [20].

recombination. Second, the tips of the InP nanowires, whose average length was 300 nm, were covered by hemispherical caps of ITO. A photovoltaic junction formed not only at the top but also on the sides of the nanowires, and this resulted in an improvement in the separation and collection efficiency of the photogenerated carriers. In addition, more than 98% of the incident light with wavelengths less than 500 nm was absorbed within a depth of 300 nm in the InP, and hence, the IQE at shorter wavelengths increased. The effective reflectance of the device after taking account of the solar spectrum distribution [21] was 6.2%, and it should be emphasized that the device did not have specially designed antireflection coatings. It is thought the lower index of refraction in the nanowire array structure made for a stepped-index antireflection coating [22]. In addition, the ITO layer had a high-refractive index (n ~ 1.95) and suppressed scattering of light.

7.4 Structural and Optical Analysis

The absorption on the low-energy side started to rise from about 870 nm, which is substantially blue-shifted relative to the bulk bandgap of InP (925 nm). To examine the course of the blue-shift, we measured the crystal structure of the InP nanowire by using high-resolution transmission electron microscopy (HR-TEM) at an acceleration voltage of 300 kV along the <-110> incidence, as shown in **Fig. 7-5(a)**. **Figures 7-5(b)-(c)** show the corresponding selective area electron diffraction (SAED) patterns. In the HR-TEM image, the crystal structure in the nanowire

region is clearly different from the substrate region. The SAED pattern at the nanowire indicates the grown *p*-InP nanowire is a pure wurtzite structure without a zincblende structure (**Fig. 7-5(b)**); in contrast, zincblende spots can be seen in the SAED pattern at the interface between the nanowires and the substrate (**Fig. 7-5(c)**).

The wurtzite structure of the nanowires was confirmed by making a reciprocal space mapping results of X-ray diffraction, as shown in **Fig. 7-6(a)**. The (10-1.5) and (331) peaks correspond to wurtzite and zincblende structures. This is consistent with our previous results whose samples were grown under similar growth-temperature and V/III ratio conditions [23]. It is known that bandgap energy of wurtzite InP is about 80 meV higher than that of zincblende [24]. This suggests that the absorption edge on the low-energy side of the heterojunction device is blue-shifted. To clarify the bandgap shift in the *p*-InP nanowires, the wires were studied with micro-photoluminescence (PL) at room temperature (**Fig. 7-6(b)**). The PL spectrum of the InP substrate exhibits a peak at 920 nm (=1.35 eV), while the spectrum of the *p*-InP nanowires had a peak at 885 nm (=1.40 eV). The PL peak of the nanowires was blue-shifted, but it was less than the theoretical predicted 80 meV. This could be explained by the free-to-bound excitons stemming from zinc-doping. In addition, the HR-

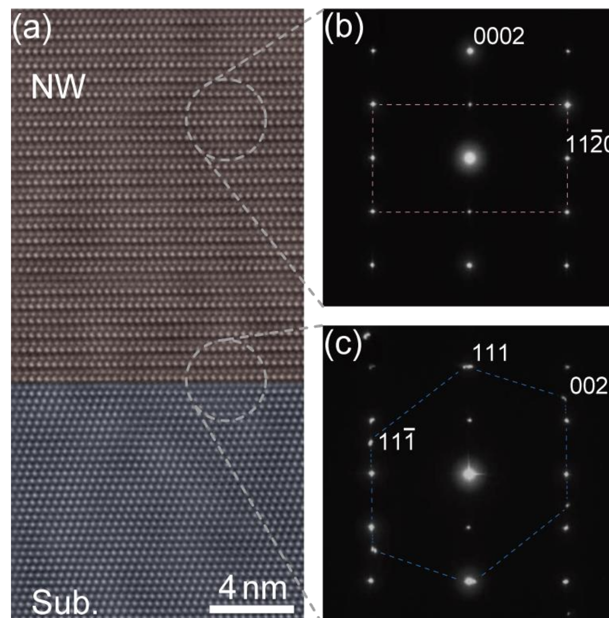

Fig. 7-5 (a) HR-TEM image for a *p*-InP nanowire/substrate interface. The corresponding SAED patterns at the (b) nanowire and (c) nanowire/substrate interface. Incident direction of electron beam is <-110>.

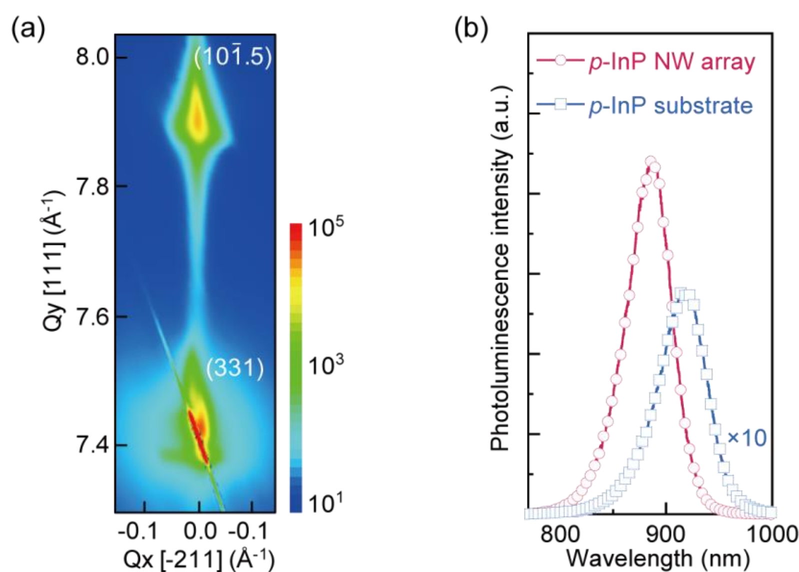

Fig. 7-6 (a) Reciprocal space mapping for the *p*-InP nanowire on the substrate. (b) PL spectra for *p*-InP nanowires and *p*-InP substrate at room temperature.

TEM image shows that the *p*-InP nanowires had no twin and misfit dislocations, suggesting that the grown nanowires were high-quality wurtzite crystals. This resulting low rate of bulk recombination was another source of IQE improvement.

7.5 Conclusion

In conclusion, we demonstrated a heterojunction solar cell that combines a *p*-doped InP nanowire array and a transparent ITO layer. The position-controlled and catalyst-free nanowires were grown using SAG. The fabricated device showed a power conversion efficiency of 7.39% under AM1.5G with a J_{SC} of 24.8 mA/cm^2. Furthermore, the ITO/InP heterojunction cell showed higher IQE than that of the current world-record-holding InP cell in the wavelength range below 570 nm. This new approach of using transparent ITO film not only for electrically connecting the nanowires in parallel but also for forming a photovoltaic junction has great potential in nanowire-based solar cells.

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Chapter 8 Summary and Conclusions

8.1 Summary

The purpose of this work is to investigate a lattice-mismatched growth and characterization of InGaAs ternary-alloy nanowires and demonstrate position-controlled nanowire array solar cells for future photovoltaic applications. Summary and conclusions are shown below.

In chapter 4, the growth temperature dependence and crystal quality of lattice-mismatched InGaAs nanowire arrays on GaAs(111)B substrate by using selective-area metal-organic vapor phase epitaxy (SA-MOVPE) are investigated. Highly uniform InGaAs nanowire arrays without hillock-like depositions were grown at 700 °C, while the hillock-like depositions of 1–3 μm in diameter were observed on the patterned SiO_2 mask areas. The growth rates of the nanowires increased at higher growth temperatures, but the diameters of the nanowires for each mask opening diameter appeared to be roughly equal and independent of the growth temperature. The photoluminescence (PL) peak energy exhibited a blue shift with increasing growth temperature, meaning that the Ga composition in the InGaAs nanowires increased with increasing growth temperature. We estimated the volume portions of GaAs and InAs in the InGaAs nanowire and found that the InAs portion was almost constant between 600 and 700 °C, while the GaAs portion decreased with decreasing the temperature.

The InGaAs nanowire with lattice-mismatch of 2.1% were found to grow coherently on GaAs(111)B substrate without misfit dislocations. From the energy dispersive X-ray line scan of the InGaAs nanowire, the group-III mole fractions were virtually constant along the 2-μm-long nanowire, which indicates that the difference in migration length between In and Ga atoms on the sidewall facets has no effect on the longitudinal composition change in nanowires up to 2 μm. A PL spectrum for the InGaAs nanowires grown on GaAs(111)B showed a strong band-edge emission peak at 1.12 eV, while InGaAs planar layers grown on GaAs(111)B and GaAs(100) exhibited no band-edge emission peak. This indicates that the crystal quality of the heteroepitaxially grown

InGaAs nanowires was better than that of the planar layers, showing promise for fabricating heterostructure photovoltaic cells using a lattice-mismatched material system.

In chapter 5, we demonstrated a growth of position-controlled InP nanowire array by using SA-MOVPE and their photovoltaic application. The fabricated device showed good rectification properties and photovoltaic performance. It exhibited a conversion efficiency of 4.23% under air mass 1.5 global illuminations with an open-circuit voltage (V_{OC}) of 0.674 V, short-circuit current density (J_{SC}) of 11.1 mA/cm^2, and fill-factor (*FF*) of 0.585. The periodic nanowire array solar cells demonstrated the light absorption enhancement effect by low reflectance obtained without applying anti-reflection coatings and absorption of incident light that traveled between the nanowires. Furthermore, we analyzed the dependence of the performance characteristics on the illumination intensity and confirmed that the device was well functioning which is based on a solid state semiconductor physics. Although a number of issues remain to get higher conversion efficiency, the results reported here represent the potency and the capabilities of the nanowire-array-based solar cells.

In chapter 6, surface-passivated InP/AlInP core-multishell nanowire array solar cells are investigated. The effective reflectance of the uniform nanowire array is 3.4%, which is one-tenth that of the planar cell (33.2%). The device with the window layer has an excellent J_{SC} of 23.4 mA/cm^2, a V_{OC} of 0.457 V, and a *FF* of 0.596 (for an overall conversion efficiency of 6.35%). At all wavelengths above 450 nm, the internal quantum efficiency of the cell with the window layer was greater than that of the one without the window layer, indicating that the AlInP window layer reduces the surface recombination. Reducing surface recombination by using a lattice-mismatched AlInP window layer to passivate the n-InP shell layer, we were able to fabricate an array of nanowire solar cells that have a J_{SC} much better than that of the InP nanowire array solar cells reported in chapter 5.

In chapter 7, we demonstrated a heterojunction solar cell that combines a *p*-doped InP nanowire array and a transparent ITO layer. The position-controlled and catalyst-free nanowires were grown using selective area growth. The fabricated device showed a power conversion efficiency of 7.39% under AM1.5G with a J_{SC} of 24.8 mA/cm^2. Furthermore, the ITO/InP heterojunction cell showed higher IQE than that of the current world-record-holding InP cell in the wavelength range below 570 nm. This new approach of using transparent ITO film not only for

electrically connecting the nanowires in parallel but also for forming a photovoltaic junction has great potential in nanowire-based solar cells.

8.2 Outlook for Nanowire-Based Solar Cells

From the early 2000s onward, publications of nanowire-based solar cells have increased dramatically. The structure, which is the vertical semiconductor nanowire arrays, offer the advantages of enhanced light absorption without antireflection coating and improved separation and collection efficiencies of photon-generated carriers. Additionally the nanowire structures stacked vertically have greater latitude for the use of the materials due to accommodating lattice strain in two dimensions, which is better for multi-junction cells to achieve high efficiency. Most papers, however, fabricated solar cells using one nanowire or randomly grown nanowires, thus these did not demonstrate the effect of the nanowire-array architectures. Under these circumstances, our work, which demonstrated the photovoltaic cells based on position-controlled nanowire arrays and their architectural effects, contribute to progress for practical use of nanowire-based solar cells in the future.

The next step is thought to be establishment of the photovoltaic cell detachment and transfer from semiconductor substrate to flexible carrier substrate for cost reduction, light weight, and flexible. Because compound semiconductor substrate is much more expensive than silicon substrate, reusing of the substrate is key factor to achieve the low cost fabrication. Another step is to promote the high efficiency by not only the optimization of structure, doping profile, and growth condition, but also by multi-junction cell and intermediate band cell. The best reported efficiency for nanowire array solar cell is about 14%, much lower than the highest cell with 44.7% efficiency. For the future, these research topics are focused on the field of nanowire-based solar cells.

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5. Awards

[1] 「第 32 回応用物理学会講演奨励賞」, 吉村 正利, 中井 栄治, 冨岡 克広, 福井 孝志, “InP ナノワイヤアレイ太陽電池の表面パッシベーション”, 春季第 59 回応用物理学関係連合講演会, 早稲田大学, 2012 年 3 月.

6. Press release

[1] “InP nanowire solar cells with improved short-wavelength response”, Semiconductor Today, Jan. 7 (2014).