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Current linearity and operation stability in Al₂O₃-gate AlGa_n/Ga_n MOS high electron mobility transistors

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To investigate current linearity and operation stability of metal–oxide–semiconductor (MOS) AlGa_n/Ga_n high electron mobility transistors (HEMTs), we have fabricated and characterized the Al₂O₃-gate MOS-HEMTs without and with a bias annealing in air at 300 °C. Compared with the as-fabricated (unannealed) MOS HEMTs, the bias-annealed devices showed improved linearity of I_D – V_G curves even in the forward bias regime, resulting in increased maximum drain current. Lower subthreshold slope was also observed after bias annealing. From the precise capacitance–voltage analysis on a MOS diode fabricated on the AlGa_n/Ga_n heterostructure, it was found that the bias annealing effectively reduced the state density at the Al₂O₃/AlGa_n interface. This led to efficient modulation of the AlGa_n surface potential close to the conduction band edge, resulting in good gate control of two-dimensional electron gas density even at forward bias. In addition, the bias-annealed MOS HEMT showed small threshold voltage shift after applying forward bias stress and stable operation even at high temperatures. © 2017 The Japan Society of Applied Physics

1. Introduction

GaN-based high electron mobility transistors (HEMTs) have been making steady progress in high-frequency and high-power performances.^{1–5} Electron saturation velocity as high as 2×10^7 cm/s and high two-dimensional electron gas (2DEG) density of over 1×10^{13} cm⁻², originating from spontaneous and piezoelectric polarization fields as well as from large conduction band offset, are well-suited for high power radio frequency (RF) applications. By downscaling of the gate length to sub-100 nm regime in conjunction with state-of-the-art technologies, Shinohara and co-workers^{2,6} have recently achieved ultrahigh-speed operation with record-high f_T of 454 GHz with accompanying power gain cutoff frequency (f_{max}) of 444 GHz on a 20 nm gate HEMT. These are fairly desirable for the fifth generation (5G) communication system where the W-band (75–110 GHz) and the E-band (60–90 GHz) frequency ranges are expected to be used for wireless backhaul of mobile communications.

The 5G wireless system also requires higher efficiency and linearity for RF power transistors. Power amplifiers using Schottky-gate (SG) GaN HEMTs suffer from reduced gain and efficiency with increasing input RF power due to significant gate leakage currents caused by a large input swing that may drive the devices deep into the forward bias regime.⁷ In addition, such high leakage currents seriously affect the operation stability and large signal linearity of power amplifiers. Moreover, SG-HEMTs suffer from the current collapse issues,⁸ which persist even after the combined application of field plate structures and surface passivation schemes. A possible reason for this is negative surface charges induced by the tunneling injection of electrons into surface states via the SG edge. Nishiguchi et al.⁹ and Katsuno et al.¹⁰ pointed out that such charging region can extend as far as 0.5 μm from the gate edge toward the drain electrode in SG AlGa_n/Ga_n HEMTs without surface passivation.

A metal–insulator–semiconductor (MIS) structure is very effective to overcome such problems related to SG structure.

Kanamura et al.⁷ demonstrated that gate leakage current was sufficiently controlled in the AlGa_n/Ga_n MIS-HEMT even under high input power operation. Thus, a MIS-HEMT can accommodate a wider range of input signal sweep, resulting in higher maximum output power. Furthermore, Tajima and Hashizume¹¹ pointed out that the current collapse was significantly reduced in Al₂O₃-gate AlGa_n/Ga_n HEMTs, as compared with SG HEMTs with only surface passivation. In particular, the MIS structure will be absolutely necessary for InAlN/GaN HEMTs. It is known that GaN HEMTs using an InAlN electron-supplying layer are promising because of their high spontaneous polarization and high band offset at the conduction band, for enhancing 2DEG density.¹² In fact, Makiyama et al.¹³ demonstrated an output power density of 3 W/mm at 96 GHz in the GaN HEMT using quaternary InAlGa_n barrier layers. However, large gate leakage current in InAlN/GaN HEMTs often limits their operations. Kotani et al.¹⁴ pointed out that it is difficult to reduce the gate leakage current in SG InAlN/GaN HEMTs due to the large internal electric field in the InAlN barrier layer. Appropriately, the MIS structure is well-suited for addressing the leakage current issue and therefore promoting the performance of InAlN/GaN HEMTs.^{15,16}

Although various kinds of insulator materials have been applied to improve the performance of GaN-based MIS HEMTs, several problems remain unsolved.¹⁷ The most serious problem is the threshold voltage (V_{TH}) instability, as schematically shown in Fig. 1(a). Several papers reported that different bias conditions induce varying degrees of V_{TH} shift in MIS HEMTs.^{18–23} Lu et al.¹⁸ and Johnson et al.²¹ reported that higher positive gate biasing of the MIS HEMTs induces larger V_{TH} shift toward the forward bias direction. There are two possible mechanisms for this issue. Under a high positive gate bias, the Fowler–Nordheim (FN) tunneling mechanism can enhance the gate leakage current. In this case, electrons injected into trap levels in insulators cause excess negative charges, resulting in the V_{TH} shift toward the positive bias direction. The high positive gate bias also



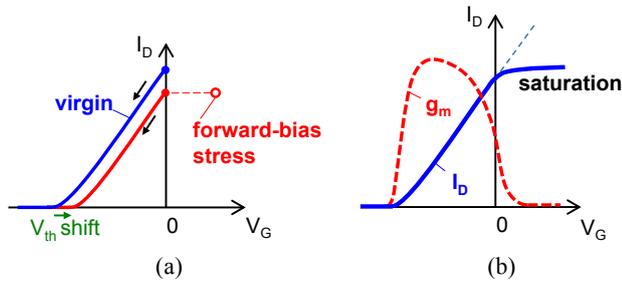


Fig. 1. (Color online) (a) Illustrations of V_{TH} shift due to forward bias stress and (b) I_D saturation behavior at forward bias.

supplies electrons to electronic states at the insulator/barrier (AlGaN or InAlN) interface, and the acceptor-type states produce negative charges when they trap electrons. Due to the long associated time constant for electron emission even at RT, electrons captured at deeper interface states remain trapped during the entire duration of gate sweeping toward the negative bias direction.^{17,24} This also causes the V_{TH} shift toward the positive bias direction in the I_D - V_G characteristics, as schematically shown in Fig. 1(a).

Another problem is an unexpected degradation of current linearity in GaN-based MIS HEMTs. Although a dynamic range of input signal sweeping is one of advantages in MIS HEMTs, some groups reported on the sudden current saturation at forward bias,^{25,26} as shown in Fig. 1(b). It is likely that a high density of electronic states at the insulator/barrier interface, in particular near the conduction band edge, screens the gate electric field and causes a limited control of surface potential of the barrier layer. This prevents further increase in the 2DEG density, leading to pronounced current saturation at forward gate bias. Such degradation of current linearity can be responsible for gain loss and degradation of large signal linearity in power amplifiers.

Accordingly, this paper presents DC characterization of AlGaN/GaN MOS HEMTs using Al_2O_3 focusing on the impact of interface states on current linearity and operation stability. To control electronic states at the Al_2O_3 /AlGaN interface, MOS HEMTs were subjected to a bias annealing under air atmosphere.

2. Device fabrication and reverse-bias annealing processes

2.1 Device structure and fabrication process

Figure 2 schematically shows the cross-section of MOS-HEMT device studied in this work. $Al_{0.24}Ga_{0.76}N$ /GaN heterostructure grown on SiC substrate by metal organic chemical vapor deposition (MOCVD) was used as the starting wafer. The 2DEG density and mobility of the AlGaN/GaN heterostructure were $9.0 \times 10^{12} \text{ cm}^{-2}$ and $1740 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, respectively. Ti/Al/Ti/Au (= 20/50/20/50 nm) source and drain electrodes were deposited on the AlGaN surface, followed by ohmic annealing at 830 °C for 1 min in N_2 ambient. As a surface protection layer during ohmic annealing, a 20-nm-thick SiN film was deposited to prevent damage to the AlGaN surface.²⁷ After the ohmic metallization process, the SiN film was removed using a buffered HF solution. An Al_2O_3 layer with a nominal thickness of 30 nm was then deposited on the AlGaN surface using an

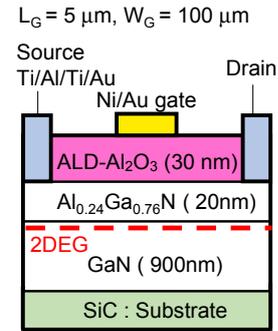


Fig. 2. (Color online) Schematic cross-sectional view of the Al_2O_3 / $Al_{0.24}Ga_{0.76}N$ /GaN MOS HEMT structure.

atomic layer deposition (ALD) system (SUGA-SAL1500) at 300 °C. In the deposition process, water vapor and trimethylaluminum were introduced into a reactor in alternate pulse forms. Each precursor was injected into the reactor for 15 ms, and the purging time was set to 5 s. In this case, the deposition rate is 0.11 nm/cycle, facilitating the formation of Al_2O_3 in a layer-by-layer fashion. Finally, the device fabrication was completed by electron beam evaporation of Ni/Au bilayer and subsequent lift-off process to form the gate electrode. The gate length, gate width, and gate-drain distance were 5, 100, and 10 μm , respectively.

2.2 Reverse-bias annealing process

To improve the interface properties of GaN MIS structures, we have carried out various kinds of control processes including post-deposition and post-metallization annealing processes. As described in Ref. 28, a standard post-deposition annealing at 400–700 °C in N_2 for 30 min was effective in decreasing state densities at the Al_2O_3 /GaN interface. Even in this case, however, the interface state density of $5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ or higher remained, indicating that the post-deposition annealing is insufficient for controlling interface states. We then found that the post-metallization annealing in air at 300 °C for several hours is more effective in achieving better capacitance–voltage (C - V) characteristics than a conventional post-deposition annealing.²⁸ Next, we focused on the occupation condition of interface states during the post-metallization annealing in air, because it can be coupled with change in atomic-bonding configuration at the interface. Then we chose two bias conditions, i.e., an accumulation forward bias (typically +5 V) for occupied interface states with electrons and a deep reverse bias (typically -10 V) for empty interface states. As a result, excellent C - V characteristics with negligible frequency dispersion were observed from the MOS sample after annealing under a reverse bias at 300 °C in air for 3 h.²⁸ The reverse-bias annealing achieved interface state densities less than $8 \times 10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$, probably due to the relaxation of dangling bonds and/or reduction of point defects on the GaN surface (Al_2O_3 /GaN interface). We also observed small shifts of flat-band voltage and stable C - V behavior at 200 °C for bias annealed Al_2O_3 /GaN diodes.²⁸ In this work, we expect that the desirable effects of the reverse-bias annealing can be extended to AlGaN/GaN MOS HEMTs, thereby giving an alternative method in pushing the performance of these devices when applied in high power and high frequency applications.

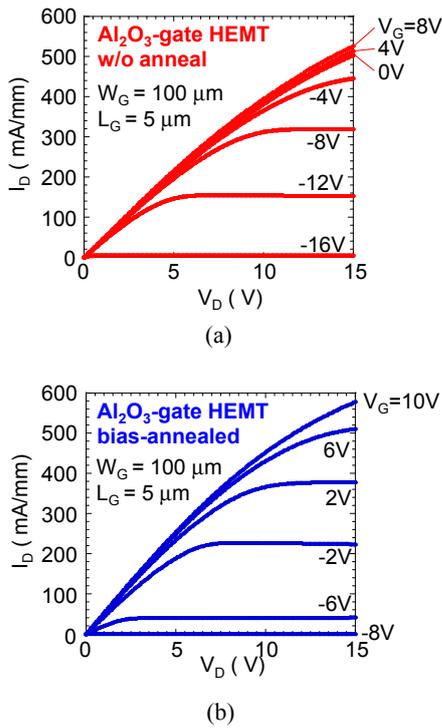


Fig. 3. (Color online) I_D - V_D characteristics of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS HEMTs (a) without and (b) with the bias annealing process.

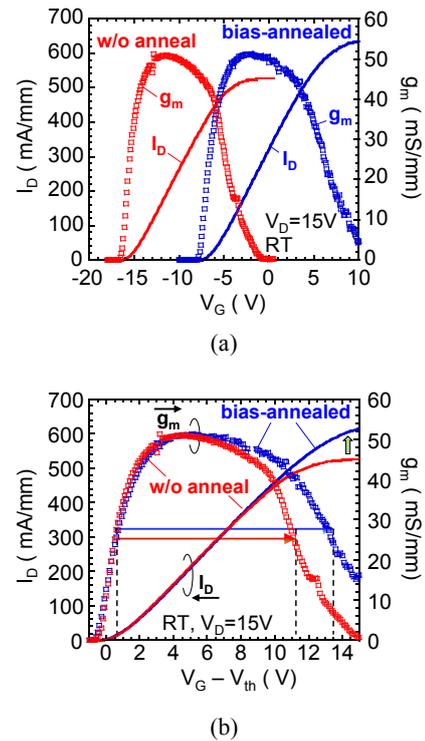


Fig. 4. (Color online) (a) Transfer characteristics of $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS HEMTs without and with the bias annealing process. (b) The data were replotted with respect to $V_G - V_{TH}$.

3. Results and discussion

3.1 I - V characteristics and gate controllability of AlGaIn/GaN MOS-HEMTs

Typical I_D - V_D characteristics of MOS-HEMTs without and with the bias annealing are shown in Fig. 3. Both devices showed relatively good I_D - V_D behavior at low V_G bias. For the MOS-HEMT without annealing, however, suppressed increase in I_D was observed at the gate bias higher than 0V. On the other hand, the MOS-HEMT with the bias annealing showed good gate control of I_D even at forward gate bias, as shown in Fig. 3(b).

The transfer characteristics of MOS-HEMTs without and with the bias annealing are shown in Fig. 4(a). For comparison, their transfer curves as a function of gate overdrive voltage ($V_G - V_{TH}$) are replotted in Fig. 4(b). The bias-annealing process effectively improved the current linearity, particularly in forward bias, resulting in a broader g_m plateau and increased maximum drain current. This effect is important for the MOS-HEMT in terms of the input dynamic range at forward bias. We then calculated the subthreshold slope of MOS-HEMTs from the semi-log scale I_D - V_G characteristics shown in Fig. 5. A high value of subthreshold slope of 148 mV/dec was obtained before the bias annealing. After bias annealing, the subthreshold slope was decreased down to 112 mV/dec. In addition, the V_{TH} change and significant decrease in gate leakage current were observed in the MOS-HEMT after the bias annealing, as shown in Fig. 5. A possible mechanism for these will be discussed later.

To investigate interface properties of the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ gate structures, C - V characterization was performed on MOS diodes fabricated on the same AlGaIn/GaN heterostructures. A circular gate with a diameter of 200 μm was prepared for the MOS diodes. C - V curves obtained using a signal

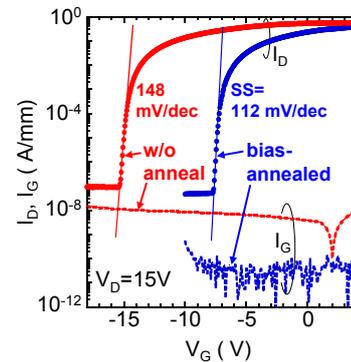


Fig. 5. (Color online) Logarithmic transfer curves and gate leakage current of MOS-HEMTs.

frequency of 1 MHz at RT are shown in Fig. 6(a). Both diodes without and with the bias annealing showed the two-step behavior typically observed in HEMT MOS structures.^{24,29} The first step at reverse bias indicates the depletion of 2DEG at the AlGaIn/GaN interface. The following capacitance plateau corresponds to the equivalent capacitance of Al_2O_3 and AlGaIn layers connected in series. At forward bias, the nearly flat band condition of the AlGaIn layer can lead to the electron spillover from the AlGaIn/GaN to $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interfaces.²⁹ Consequently, the effective capacitance approaches that of the insulator capacitance.

To evaluate the effects of interface states on the C - V characteristics, one-dimensional simulation including self-consistent Poisson-Schrödinger calculations was carried out for the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ structure, taking into account a state density distribution [$D_{it}(E)$] consisting of acceptor- and donor-like states separated by the charge neutrality level

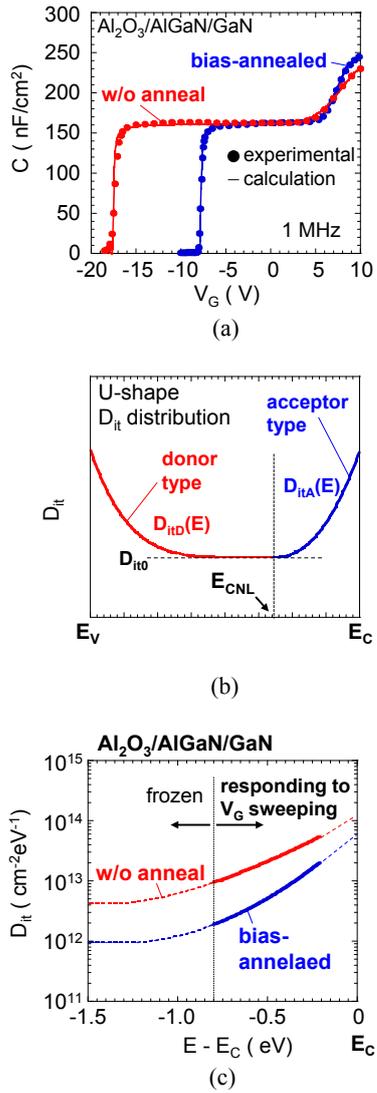


Fig. 6. (Color online) (a) C - V characteristics of the $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MOS diodes. The solid line indicates calculated curves. (b) Schematic illustration of interface state density (D_{it}) distribution used for calculation. (c) D_{it} distributions determined by the fitting of C - V curves.

E_{CNL} ,^{30–32} as schematically shown in Fig. 6(b). Along the insulator–semiconductor interface, the crystalline periodicity of the semiconductor is terminated. In addition, disorder in atomic-bond arrangement can be induced at the semiconductor surface. In this case, the separation of conduction and valence bands becomes insufficient, resulting in the penetration of bonding and anti-bonding states into the forbidden band (bandgap) from valence and conduction bands, respectively.^{33,34} Therefore, the charging character of interface states also reflects those of valence and conduction bands. Namely, a negative charge appears in the conduction band if a state is occupied by an electron (acceptor-like character), while valence band state is positively charged when unoccupied (donor-like character). Thus, it can be assumed that the interface state continuum consists of a mixture of acceptor-like and donor-like states, as schematically shown in Fig. 6(b), and their branch point act as the E_{CNL} . This model is often used as a density distribution of interface states.^{35–37}

For the calculation, we assumed an arbitrary D_{it} distribution using the following equations:³⁰

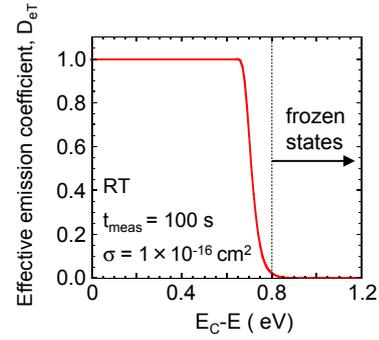


Fig. 7. (Color online) Calculated $D_{eT}(E)$ using $t_{\text{meas}} = 100$ s, $\sigma = 1 \times 10^{-16} \text{ cm}^2$ and $\tau(E)$ obtained from Eq. (2).

$$D_{itA} = D_{it0} \exp\left[\left(\frac{E - E_{CNL}}{E_{0A}}\right)^{n_A}\right], \quad (1a)$$

$$D_{itD} = D_{it0} \exp\left[\left(\frac{E_{CNL} - E}{E_{0D}}\right)^{n_D}\right], \quad (1b)$$

where D_{it0} is the minimum state density. E_0 and n define the curvature of the D_{it} distribution, as shown in Fig. 6(b). In addition, we can estimate electron emission time constant $\tau(E)$ from interface states to the conduction band using Shockley–Read–Hall (SRH) statistics:

$$\tau(E) = \frac{1}{v_{TH}\sigma_{TH}N_C} \exp\left(\frac{E_T}{kT}\right), \quad (2)$$

where v_{TH} , σ_{TH} , N_C , and E_T are electron thermal velocity, capture cross section of interface states, density of state at the conduction band, and interface state energy, respectively. From $\tau(E)$ and the experimental C - V measurement time (t_{meas}), we calculated the effective emission coefficient $D_{eT}(E)$ of interface states:

$$D_{eT}(E) = 1 - \exp\left[-\frac{t_{\text{meas}}}{\tau(E)}\right]. \quad (3)$$

Figure 7 shows the calculated $D_{eT}(E)$ at RT using $t_{\text{meas}} = 100$ s and $\sigma = 1 \times 10^{-16} \text{ cm}^2$.³⁰ According to Eq. (2), $\tau(E)$ of interface states near midgap or deeper are too large at RT, resulting in $D_{eT}(E) = 0$. This means that electrons once captured at such deep interface states remain trapped even when large negative bias is applied to the gate electrode. It is estimated from Fig. 7 that interface states at energies below $E_C - 0.8 \text{ eV}$ behave like “frozen states”. By considering $D_{eT}(E)$ and Fermi–Dirac occupation function, we obtained interface state charges (ionized state density) at a given gate voltage V_G . Then we calculated C - V curve based on the potential and electron density distributions by numerically solving Poisson–Schrödinger equations, and compared experimental and calculated C - V curves. If we observed the discrepancy between them, then the D_{it} distribution was modified and the recalculation was repeatedly carried out. Physical parameters used in the calculation are summarized in Table I.

Using the D_{it} distributions shown in Fig. 6(c), the calculation well reproduced the experimental C - V data, as indicated by solid lines in Fig. 6(a). As described above, only the acceptor-like traps in the energy range indicated by solid lines in Fig. 6(c) can change their charge state accordingly with the gate voltage sweep at RT. Note, in addition, that it is difficult to evaluate the state density distribution at energies

Table I. Parameters used in the calculations. m_0 is the mass of a free electron, q is the elementary charge, and AlGaN denotes $\text{Al}_{0.24}\text{Ga}_{0.76}\text{N}$.

Parameter name	Symbol (unit)	Numerical value (material or interface)
Bandgap at RT	E_G (eV)	3.4 (GaN) ³⁸
		3.89 (AlGaN) ^{38,39}
		7.0 (Al_2O_3) ⁴¹
Effective mass of electron	m_e/m_0	0.20 (GaN)
		0.23 (AlGaN)
Relative permittivity	ϵ	9.5 (GaN)
		9.2 ($\text{Al}_{0.24}\text{Ga}_{0.76}\text{N}$)
		9.0 (Al_2O_3)
Band offset	ΔE_C (eV)	0.34 (AlGaN/GaN) ³⁸
		2.1 ($\text{Al}_2\text{O}_3/\text{AlGaN}$) ⁴¹
Surface barrier height	ϕ_s (eV)	3.4 (Ni/ Al_2O_3) ⁴⁰
Polarization induced sheet charge	n_s (q/cm^2)	8×10^{12} (AlGaN/GaN)
Charge neutrality level	E_{CNL}	$E_C - 1.3$ eV ($\text{Al}_2\text{O}_3/\text{AlGaN}$) ³²
Capture cross section of interface states	σ (cm^2)	1×10^{-16} ³⁰
C-V Measurement duration	t (s)	100

above $E_C - 0.2$ eV from C-V measurements using frequency of 1 MHz, because electron trapping/detrapping processes at such shallow interface states can respond to the measurement AC signal and accordingly give an inaccurate estimate of capacitance. Therefore, state densities at the energies above $E_C - 0.2$ eV were not considered for the present C-V calculation.

As shown in Fig. 6(c), the $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface without annealing showed high interface state densities of over $1 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$. The bias annealing process effectively decreased the state densities, leading to the steeper C-V slope in forward bias shown in Fig. 6(a). The calculated V_{TH} corresponding to the first step in the C-V curve was -7.5 V, very close to that of the MOS-HEMT subjected to bias annealing, as shown in Fig. 6(a). On the other hand, the sample without the annealing showed a V_{TH} shift toward the negative bias direction, probably due to excess positive charges arising from donor-type interface states and/or defect levels in the bulk Al_2O_3 . When a fixed charge of $+1.2 \times 10^{13} \text{ cm}^{-2}$ was assumed in the Al_2O_3 layer or at the $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface, the calculation reproduced the experimental C-V result for the HEMT without annealing, as shown in Fig. 6(a). A possible candidate for a defect level in Al_2O_3 is an oxygen-vacancy related defect.^{42,43} The bias-annealing process decreased such levels, resulting in the V_{TH} recovery toward the expected value. Zhou et al.⁴⁴ also reported similar V_{TH} recovery with a post-deposition annealing in $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$ MOS-HEMTs. As shown in Fig. 5, in addition, we observed decrease in gate leakage current in the MOS-HEMT after the bias annealing. For the GaN-based MIS-HEMTs using Al_2O_3 , SiN_x and AlTiO , it has been reported that the Poole-Frenkel (PF) emission conduction was dominant for gate leakage current.⁴⁵⁻⁴⁸ Similarly to the V_{TH} recovery behavior, there is a possibility the reduction of leakage current arises from decrease in defect levels in the Al_2O_3 layer, contributing to the suppression of the PF hopping conduction.

The C-V analysis showed that the bias annealing process effectively decreased state densities at the $\text{Al}_2\text{O}_3/\text{AlGaN}$

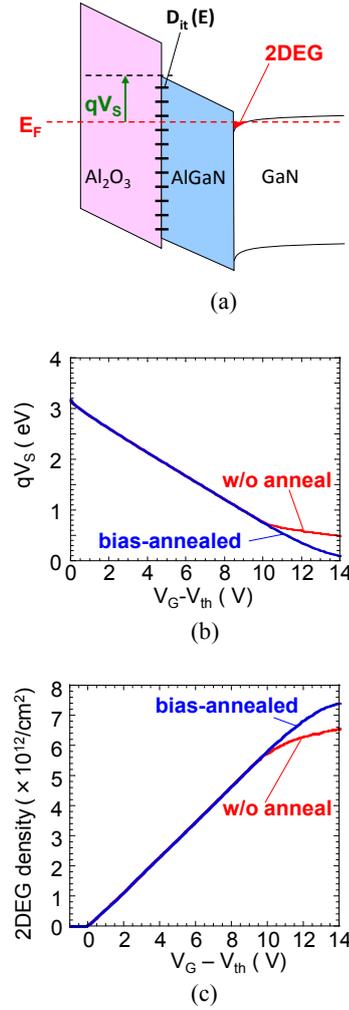


Fig. 8. (Color online) (a) Band diagram of the $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$ structure. V_S indicates the AlGaN surface potential. (b) Calculated V_S as a function of $V_G - V_{\text{TH}}$ with assuming D_{it} distributions shown in Fig. 6. (c) Calculated 2DEG densities as a function of $V_G - V_{\text{TH}}$ for the MOS-HEMTs without and with the bias annealing.

interface, leading to the improvement of current linearity, as shown in Fig. 4. To gain a better insight into the relationship between interface states and gate controllability of the MOS-HEMT, we calculated surface potential (V_S) of AlGaN shown in Fig. 8(a) and the 2DEG density as a function of gate overdrive, taking into account D_{it} distributions obtained from the C-V analysis [Fig. 6(c)]. For the 2DEG density calculation, we used the following equation:^{49,50}

$$\text{2DEG density}_i = \frac{m_e k_B T}{\pi \hbar^2} \ln \left[1 + \exp \left(\frac{E_i - E_f}{k_B T} \right) \right], \quad (4)$$

where m_e is the effective electron mass, k_B is Boltzman's constant, T is the temperature, and i indicates the i th discrete excited level at the AlGaN/GaN interface.

Figure 8(b) shows the calculated V_S as a function of gate overdrive for the MOS-HEMTs without and with the bias annealing. In the gate bias range up to 10 V, both devices showed the same V_S change. This gate voltage corresponds to $qV_S = 0.8$ eV. As mentioned above, interface states at energies below $E_C - 0.8$ eV are considered to be "frozen states", i.e., negligible effect on the V_S control. Beyond $V_G - V_{\text{TH}} = 10$ V, acceptor states shown in Fig. 6(c) are active accordingly with the gate voltage sweeping, and the

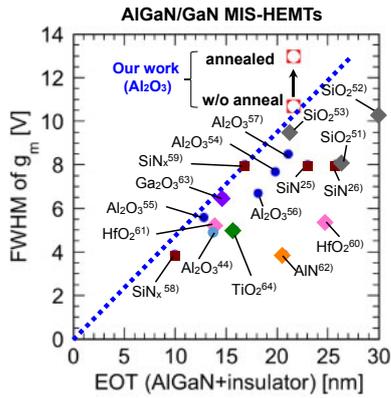


Fig. 9. (Color online) Plots of FWHM in the g_m spectrum as a function of the EOT including insulator and AlGaIn barrier layers for AlGaIn/GaN MIS-HEMTs. The numbers indicate literatures cited.

ionized acceptor charges screen the gate electric field. Thus high-density states prevent V_S modulation (poor potential control) for the MOS-HEMT without the bias annealing. Such V_S behavior is directly related to the control of the 2DEG density, as shown in Fig. 8(c). The limited increase in the 2DEG density with V_G is clearly observed for the MOS-HEMT without the bias annealing. On the other hand, the MOS-HEMT with annealing shows relatively good control of 2DEG by V_G . The calculated results shown in Fig. 8(c) are similar to the measured I_D - V_G curves of MOS-HEMTs shown in Fig. 4(b), indicating that the effective reduction of interface states is responsible for the improved linearity in MOS-HEMT with bias annealing.

It should be mentioned that some papers reported poor current linearity in MIS-type AlGaIn/GaN HEMTs. To investigate current linearity behavior, we tried to plot the full width at half maxima (FWHM) of g_m - V_G profiles as a function of the equivalent oxide thickness (EOT) including insulator and AlGaIn barrier layers. Figure 9 shows comparison of FWHM of g_m for AlGaIn/GaN MIS-HEMTs using SiO_2 ,⁵¹⁻⁵³ Al_2O_3 ,^{44,54-57} SiN ,^{25,26,58,59} HfO_2 ,^{60,61} AlN ,⁶² Ga_2O_3 ,⁶³ and TiO_2 ⁶⁴ dielectric materials. Our data are also included in Fig. 9. It is expected that the FWHM of g_m increases with EOT, and experimental data generally showed this tendency. However, there is a wide scattering of data, indicating that interface properties of insulator/AlGaIn structures are not dependent on the insulator material used but on the bond disorder and/or surface defects on the AlGaIn surface, probably related to fabrication process conditions including deposition methods.^{17,65-67} The broken line is a guide to the eye for the better results reported.^{53,55,59} Our device with the bias annealing showed high FWHM value, demonstrating excellent current linearity in our AlGaIn/GaN MOS-HEMT.

3.2 Operation stability of AlGaIn/GaN MOS-HEMTs

To evaluate operation stability of the MOS-HEMT, the V_{TH} shift after applying forward bias stress was also investigated. For fair comparison, the equivalent stress bias with respect to $V_G - V_{TH}$ was applied to the MOS-HEMTs without and with the bias annealing ($V_G - V_{TH} = 23$ V), as shown in Fig. 10. The gate stress time was 10 s, while keeping $V_D = 15$ V. Then the I_D - V_G characteristics were measured from $V_G = 0$ V toward the negative bias direction, as shown in Fig. 10. The broken lines indicate the transfer curves without the stress

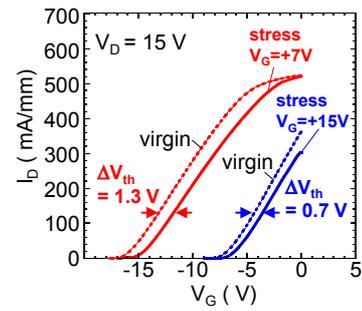


Fig. 10. (Color online) Transfer characteristics before and after the forward bias stress for the MOS-HEMTs without and with the bias annealing.

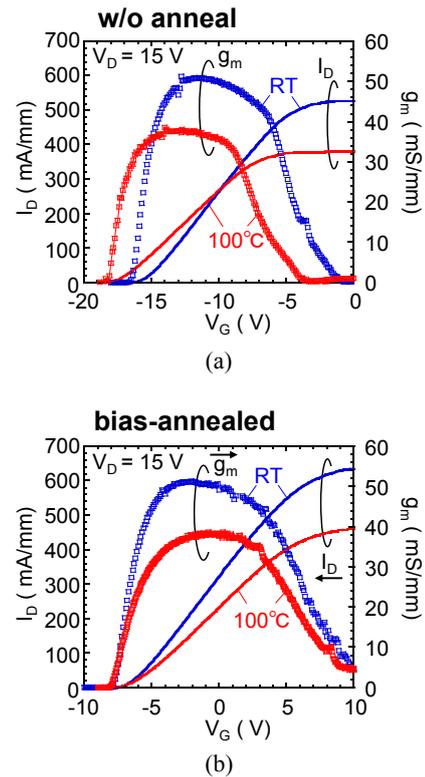


Fig. 11. (Color online) Transfer characteristics measured at RT and 100°C for the MOS-HEMTs (a) without and (b) with the bias annealing.

bias. We observed V_{TH} shift toward the forward bias direction after applying the stress bias for both devices, similar to those reported for AlGaIn/GaN MIS-HEMTs.^{18,19} It is likely due to electron injection into traps in Al_2O_3 and/or states at the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface, producing negative charges. It was found from the C - V analysis as described above that the bias annealing process effectively reduced both interface states and bulk traps in Al_2O_3 , thereby mitigating the V_{TH} shift even after applying the forward bias stress in bias-annealed device, as shown in Fig. 10.

We then measured the transfer characteristics of the devices at a higher temperature of 100°C. As shown in Fig. 11, both devices showed about 30% reduction in g_m and decreased maximum drain current, as compared with those measured at RT. This is consistent with the results reported by Husna et al.⁶⁸ and Suria et al.,⁶⁹ and mainly due to the reduction of electron mobility attributed to optical phonon scattering at high temperatures.^{70,71} As shown in Fig. 11(a), the MOS-HEMT without the annealing showed a deeper V_{TH} at 100°C.

Husna et al.⁶⁸⁾ and Yang et al.⁷²⁾ reported similar V_{TH} shift at high temperature, and pointed out a possibility that some of donor-like defect levels such as oxygen vacancies in Al_2O_3 can detrapp larger number of electrons at elevated temperatures, resulting in excess positive charges driving the V_{TH} toward the negative bias direction. According to the SRH statistics, in addition, deeper interface states can emit electrons to the conduction band at higher temperatures, relatively increasing the number of positive charges at the Al_2O_3 / $AlGaN$ interface. High densities of states for the MOS-HEMT without the annealing, as shown in Fig. 6(c), enhance this charging effect. On the other hand, the V_{TH} of the MOS-HEMT with the bias annealing remained unchanged even at 100 °C, as shown in Fig. 11(b), probably due to the reduction of defect levels in Al_2O_3 and interface states.

4. Conclusions

To improve current linearity and operation stability, bias annealing in air at 300 °C was applied to $AlGaN/GaN$ MOS-HEMTs using Al_2O_3 as gate oxide. The device without annealing showed a sudden current saturation at forward bias. On the other hand, the MOS HEMT with the annealing showed improved current linearity, resulting in the increase in the maximum drain current. Lower subthreshold slope was also observed after the bias annealing. From the precise $C-V$ analysis on the MOS diode fabricated on the $AlGaN/GaN$ heterostructure, it was found that the bias annealing effectively reduced the state density at the $Al_2O_3/AlGaN$ interface. This led to efficient modulation of the $AlGaN$ surface potential closely to the conduction band edge, resulting in good gate control of 2DEG density even at forward bias. In addition, the MOS HEMT with the annealing showed smaller threshold voltage shift after applying forward bias stress. For the device without annealing, the V_{TH} measured at 100 °C was much deeper than that at RT. On the other hand, such temperature-dependent change in the V_{TH} was not observed for the MOS-HEMT with the annealing. We therefore demonstrated that bias annealing in air is effective in improving current linearity and operation stability of $Al_2O_3/AlGaN/GaN$ MOS-HEMTs.

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