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Highly-stable and low-state-density Al₂O₃/GaN interfaces using epitaxial n-GaN layers grown on free-standing GaN substrates

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Interface characterization was carried out on Al₂O₃/GaN structures using epitaxial n-GaN layers grown on free-standing GaN substrates with relatively low dislocation density ($<3 \times 10^6 \text{ cm}^{-2}$). The Al₂O₃ layer was prepared by atomic layer deposition. The as-deposited metal-oxide-semiconductor (MOS) sample showed a significant frequency dispersion and a bump-like feature in capacitance-voltage (C-V) curves at reverse bias, showing high-density interface states in the range of $10^{12} \text{ cm}^{-1} \text{ eV}^{-1}$. On the other hand, excellent C-V characteristics with negligible frequency dispersion were observed from the MOS sample after annealing under a reverse bias at 300 °C in air for 3 h. The reverse-bias-annealed sample showed state densities less than $1 \times 10^{11} \text{ cm}^{-1} \text{ eV}^{-1}$ and small shifts of flat-band voltage. In addition, the C-V curve measured at 200 °C remained essentially similar compared with the room-temperature C-V curves. These results indicate that the present process realizes a stable Al₂O₃/GaN interface with low interface state densities. *Published by AIP Publishing.*
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Significant progress in the crystal growth of GaN and its related semiconductors enables us to obtain a free-standing GaN substrate and a homo-epitaxial GaN layer on the GaN substrate with a relatively low dislocation density (N_{DIS}) of $1 \times 10^6 \text{ cm}^{-2}$ or less. Kyle *et al.*¹ demonstrated that a homo-epitaxial n-GaN ($N_{\text{DIS}} = 2 \times 10^6 \text{ cm}^{-2}$) with a carrier density of $3.7 \times 10^{16} \text{ cm}^{-3}$ achieved a mobility of $1265 \text{ cm}^2/\text{Vs}$ and $3327 \text{ cm}^2/\text{Vs}$ at room temperature (RT) and 113 K, respectively. Recently, a high breakdown voltage over 4 kV and low leakage current were reported for the p⁺n junction with the n-type drift layer of 40 μm fabricated on a GaN substrate with $N_{\text{DIS}} = 1 \times 10^4 \text{ cm}^{-2}$.² Hu *et al.*³ also reported the excellent properties of the GaN p⁺n diodes grown on a GaN substrate with a dislocation density of $\sim 10^6 \text{ cm}^{-2}$. The p⁺n diode with an 8-μm drift layer showed a blocking voltage of over 1.4 kV and an on-state resistance (R_{ON}) of $0.12 \text{ m}\Omega \text{ cm}^2$, giving the highest figure-of-merit ever reported in any semiconductor system.³ In addition, the Schottky diodes on the GaN layers with low dislocation densities showed nearly ideal I-V characteristics according to a simple thermionic field emission model.⁴ These results indicate highly improved crystalline quality of the current n-GaN epitaxial layers grown on the GaN substrates.

The improved crystalline quality of GaN on GaN also has become a driving force for developing vertical-type GaN transistors with metal-insulator (oxide)-semiconductor (MIS or MOS) structures. Kodama *et al.*⁵ successfully fabricated a trench-type GaN field-effect transistor (FET) with a SiN gate. For the trench structure, they used a combination of dry etching and subsequent wet etching with tetramethylammonium hydroxide. Recently, Oka *et al.*⁶ also reported a trench-type

GaN MOSFET with a SiO₂ gate, demonstrating a blocking voltage over 1.2 kV, a threshold voltage (V_{TH}) of 3.5 V, and R_{ON} of $1.8 \text{ m}\Omega \text{ cm}^2$. In these cases, it was expected that the insulated gate on the dry-etched p-GaN surface could realize device operation with an inverted channel. However, the V_{TH} was much lower than the expected value calculated using the Mg doping density and the gate capacitance,^{5,6} indicating insufficient control of GaN surface potential by insulated gates. The control of MIS interfaces remains one of the key issues even for vertical type GaN MISFETs.

Different insulator materials have been applied to GaN-based MIS structures. Gaffey *et al.*⁷ reported that a SiO₂/SiN_x/SiO₂/n-GaN structure prepared by jet vapour deposition with the optimum process condition showed low interface state densities less than of $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at $E_{\text{C}} - 0.8 \text{ eV}$. Matocha *et al.*⁸ and Kim *et al.*⁹ presented low state densities at the SiO₂/n-GaN interfaces prepared by chemical vapor deposition (CVD) at high temperatures (830–900 °C). Kambayashi *et al.*¹⁰ demonstrated an Al₂O₃/SiO₂ bilayer gate structure achieving field-effect mobility as high as $192 \text{ cm}^2/\text{Vs}$ in a recessed GaN channel structure by dry etching. An atomic layer deposition (ALD) process realized good Al₂O₃/n-GaN interface with the relatively low state densities of around $1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ at $E_{\text{C}} - 0.8 \text{ eV}$.^{11,12} Hashizume *et al.*¹³ and Watanabe *et al.*¹⁴ reported that SiN_x/GaN interfaces prepared by CVD with suitable pre-treatments of the GaN surface exhibited low-density interface states. However, insulator/III-N interfacial properties are still not fully controlled. In addition, major studies for the insulator-GaN interfaces have been employed on MIS structures fabricated on hetero-epitaxial GaN layers grown on SiC, Si, and sapphire substrates. There are a limited number of papers reporting on interface properties of MOS structures using a free-standing

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GaN or homo-epitaxial GaN with low dislocation densities.^{15–17} In this letter, accordingly, we report on fabrication and characterization of $\text{Al}_2\text{O}_3/\text{n-GaN}$ structures using homo-epitaxial GaN layers grown on a GaN substrate with a relatively low dislocation density, particularly focusing on interface state densities and the stability of capacitance-voltage (C–V) behavior.

Figure 1 shows an $\text{Al}_2\text{O}_3/\text{n-GaN}$ MOS structure prepared by ALD. We used a homo-epitaxial Si-doped GaN layer with a thickness of 4 μm grown on an $\text{n}^+\text{-GaN}$ substrate with a relatively low dislocation density ($<3 \times 10^6 \text{ cm}^{-2}$). The donor density is $6.2 \times 10^{16} \text{ cm}^{-3}$, which was determined by a C–V method using a Schottky diode. After the pre-treatment of the n-GaN surface in a 30%-HF solution for 1 min, the Al_2O_3 layer with a nominal thickness of 30 nm was deposited on the n-GaN surface using an ALD system (SUGA-SAL1500) at 350 °C. In the deposition process, water vapor and trimethylaluminum were introduced into a reactor in alternate pulse forms. Each precursor was injected into the reactor for 15 ms, and the purging time was set to 5 s. In this case, the deposition rate is 0.11 nm/cycle, indicating the formation of Al_2O_3 in a layer-by-layer fashion. For some samples, a post-deposition annealing was carried out in N_2 for 30 min at 400 °C. A circular Ni/Au ($=20/50 \text{ nm}$) with a diameter of 200 μm was deposited on the Al_2O_3 surface as a gate electrode.

From an ellipsometry measurement, the refractive index of the ALD Al_2O_3 was estimated to be 1.60–1.65, which is close to the values reported for the amorphous Al_2O_3 films prepared by sputtering and ALD methods.^{18,19} Figure 2 shows a cross-sectional transmission electron microscope (TEM) image of the as-deposited $\text{Al}_2\text{O}_3/\text{GaN}$ interface fabricated on the GaN substrate. The sample has an abrupt and flat interface, indicating low-energy and layer-by-layer characteristics resulting from the ALD process. There is no detectable transition layer like native oxide of GaN at the $\text{Al}_2\text{O}_3/\text{GaN}$ interface. In addition, Al_2O_3 is amorphous and remained unchanged, i.e., no phase transformation even after post-deposition annealing process in the temperature range of 300–500 °C. This is consistent with the fact that the phase transformation of Al_2O_3 films from amorphous to crystalline happens at temperature of 800 °C or higher.^{11,20}

Figure 3(a) shows the room-temperature (RT) C–V characteristics of the as-deposited $\text{Al}_2\text{O}_3/\text{n-GaN}/\text{n}^+\text{-GaN}$ diode (without annealing) in a wide measurement frequency range

FIG. 1. Schematic illustration of the $\text{Al}_2\text{O}_3/\text{n-GaN}$ MOS structure fabricated on the GaN substrate.

FIG. 2. Cross-sectional transmission electron microscope (TEM) image of the as-deposited $\text{Al}_2\text{O}_3/\text{n-GaN}$ interface fabricated on the GaN substrate.

of 1 Hz to 1 MHz. The sample showed a significant frequency dispersion at reverse bias. By lowering the frequency of the ac measurement signal, deeper interface states are expected to respond accordingly to an ac signal. This allows more of the states to follow the ac frequency and thereby contribute an additional component to the measured capacitance. Similar frequency dispersions in C–V characteristics were reported for SiO_2/GaN and $\text{Al}_2\text{O}_3/\text{GaN}$ structures.^{7,8,15} In addition, bump-like C–V curves at low frequencies indicate the existence of a discrete level with relatively high density at the GaN surface. On the other hand, excellent C–V characteristics with negligible frequency dispersion were

FIG. 3. Room-temperature (RT) C–V characteristics of MOS diodes fabricated on the GaN substrate (a) without annealing and (b) with annealing in air at 300 °C for 3 h under a reverse bias voltage of -10 V . (c) The RT C–V characteristics of the MOS sample using hetero-epitaxial GaN on the sapphire substrate with annealing in air at 300 °C for 3 h under a reverse bias voltage of -10 V .

observed in the MOS sample after the annealing in air at 300 °C for 3 h under a reverse bias voltage of -10 V, as shown in Fig. 3(b). The C–V curves of the bias-annealed sample are very close to the calculated curve (broken line) with no such bump-like behavior in a very wide frequency range of 1 Hz–1 MHz. There is a difference of flat-band voltage (V_{FB}) between samples without and with the reverse-bias annealing. Again, on the one hand, the annealed sample exhibited a V_{FB} very close to the calculated value; while, on the other hand, the as-deposited sample showed a V_{FB} shift toward the negative bias direction, probably due to excess positive charges arising from donor-type interface states and/or defect levels in the bulk Al_2O_3 . As mentioned below, the bias-annealing process decreased such states and levels, resulting in the V_{FB} recovery to the expected value.

For comparison and benchmarking purposes, we also fabricated and characterized a MOS structure using a hetero-epitaxial GaN with a dislocation density of $1 \times 10^9 \text{ cm}^{-2}$ on the sapphire substrate. The thickness and the donor density of the hetero-epitaxial n-GaN layer are $2.0 \mu\text{m}$ and $6.6 \times 10^{16} \text{ cm}^{-3}$, respectively. The as-deposited $\text{Al}_2\text{O}_3/\text{n-GaN}/\text{sapphire}$ sample showed RT C–V curves with significant frequency dispersion, similar to those of the $\text{Al}_2\text{O}_3/\text{n-GaN}/\text{n}^+\text{-GaN}$ diode [Fig. 3(a)]. The reverse-bias annealing process in air at 300 °C improved C–V characteristics, as shown in Fig. 3(c), also for the $\text{Al}_2\text{O}_3/\text{n-GaN}/\text{sapphire}$ sample. However, the frequency dispersion at low frequencies and less C–V slopes were observed in C–V curves. This indicates an insufficient effect of the reverse-bias annealing on the improvement of interface properties, as compared to the MOS sample fabricated on the GaN substrate.

Figure 4(a) shows the interface state density distributions of $\text{Al}_2\text{O}_3/\text{GaN}$ interfaces determined by applying the

Terman method to 1-MHz C–V results for the $\text{Al}_2\text{O}_3/\text{n-GaN}/\text{n}^+\text{-GaN}$ structure. Note that the time constant of electron emission is extremely long at RT for interface states with deep energies relative to the conduction band edge. We thus plotted the evaluated data within the range $E_C - 0.8 \text{ eV}$ in Fig. 4. The as-deposited sample exhibited relatively high state densities in the range of $10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. In addition, a peak corresponding to a density of $2 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ appeared at around $E_C - 0.6 \text{ eV}$, probably arising from a discrete trap related to the nitrogen-vacancy defects.^{12,21,22} After post-deposition annealing at 400 °C, the interface state density was decreased. Even in this case, however, the state densities of $5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ or higher remained. On the other hand, the reverse-bias annealing in air at 300 °C for 3 h resulted in a significant reduction in state density. In fact, the reverse-bias-annealed sample showed a state density below the detection limit ($<1 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$) except for those energies near the conduction band edge, corresponding to nearly ideal C–V curves without frequency dispersion as shown in Fig. 3(b). The interface state density distribution of the MOS sample using a hetero-epitaxial GaN on the sapphire substrate is shown in Fig. 4(b). Even after the reverse-bias annealing process, the reduction of interface states for the hetero-epitaxial GaN sample was limited in densities of $2 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ or higher. It is likely that a high dislocation density accompanies high-density surface defects and/or disorder in atomic bonding on the GaN surface, leading to the limited improvement of MOS interface properties by the reverse-bias annealing.

We then investigated the stability of the MOS interface with the reverse-bias annealing. Figure 5 shows the leakage current characteristics of the $\text{Al}_2\text{O}_3/\text{n-GaN}/\text{n}^+\text{-GaN}$ structure. A sufficiently low leakage current (close to the detection limit) was observed at reverse bias. As we have confirmed the linear relation of $\log(J/E^2)$ vs $1/E$ (here, J is the current density and E is the electric field), the slight increase in the current at forward bias larger than 10 V is likely due to the Fowler-Nordheim (FN) tunneling mechanism.^{7,13} Figure 6 shows the evolution of the flat-band voltage V_{FB} as a function of the maximum forward bias voltage V_{MF} . In this case, the C–V sweeping was carried out from V_{MF} to -10 V. The reverse-bias annealed sample showed an almost constant V_{FB} , originating from low interface state densities. When the V_{MF} exceeds 10 V, the V_{FB} slightly shifts toward the positive bias direction. In this bias range, as shown in Fig. 5, the leakage current gradually increases. This probably causes electron injection into the Al_2O_3 layer with the

FIG. 4. Interface state density (D_{it}) distributions determined by applying the Terman method to 1-MHz C–V results for (a) $\text{Al}_2\text{O}_3/\text{GaN}/\text{n}^+\text{-GaN}$ and (b) $\text{Al}_2\text{O}_3/\text{GaN}/\text{sapphire}$ structures.

FIG. 5. Gate leakage current of the $\text{Al}_2\text{O}_3/\text{n-GaN}/\text{n}^+\text{-GaN}$ structure annealed in air at 300 °C for 3 h under a reverse bias voltage of -10 V.

FIG. 6. Flat-band voltage V_{FB} as a function of the maximum forward bias voltage V_{MF} for the $\text{Al}_2\text{O}_3/\text{n-GaN}/\text{n}^+\text{-GaN}$ structure annealed in air at 300°C for 3 h under a reverse bias voltage of -10 V .

resultant excess negative charges producing the shift of V_{FB} toward the positive bias direction. However, Fig. 6 showed that the V_{FB} shift was limited within 250 mV, indicating a stable interface behavior of the reverse-bias annealed sample.

Figure 7 shows the C-V characteristics measured at 200°C for the $\text{Al}_2\text{O}_3/\text{n-GaN}/\text{n}^+\text{-GaN}$ structure with the reverse-bias annealing. For high temperature C-V measurements, it is expected that deeper interface states can respond both to bias sweeping and ac signal modulation, causing changes in C-V characteristics compared with those measured at RT. In fact, Matocha *et al.*,^{8,23} Ooyama *et al.*,²⁴ and Long *et al.*¹⁵ reported significant stretch-out of C-V curves, bump-like C-V behavior, and enhanced frequency dispersion for SiO_2/GaN and $\text{Al}_2\text{O}_3/\text{GaN}$ structures at measurement temperatures from 175 to 300°C . Such unstable C-V behavior at high temperatures indicates that relatively high-density interface states can cause operation instability in GaN-based MOSFETs. In our reverse-bias annealed sample, however, the high-temperature C-V behavior remained almost unchanged, as compared with the RT C-V curves shown in Fig. 3(b). In particular, negligible frequency dispersion and the same C-V slope were observed even at high temperature of 200°C . These results indicate that the present process applied on a MOS structure on a high quality and low dislocation density GaN layer realizes a stable MOS structure with low interface state densities. For the practical device application, we applied the present control process to the $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$ HEMT. A preliminary result showed that the present process leads to improved g_m linearity, probably due to the reduction of state densities at the $\text{Al}_2\text{O}_3/\text{AlGaN}$ interface. Thus, we expect that the present annealing process has also favorable impact on $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$ structures.

As shown in Fig. 7, a slight V_{FB} shift (0.3–0.4 V) toward the positive bias direction was observed in the C-V curve

FIG. 7. C-V characteristics measured at 200°C for the $\text{Al}_2\text{O}_3/\text{n-GaN}/\text{n}^+\text{-GaN}$ structure with the reverse-bias annealing.

measured at 200°C , as compared to the RT C-V curve [Fig. 3(b)]. Since the annealed sample showed very low interface state densities and negligible frequency dispersion in C-V curves, it is unlikely that interface states or oxide levels are the ones responsible for the positive V_{FB} shift. The positive V_{FB} shift with increasing temperature was also reported for SiO_2/GaN structures.^{23,25–27} Matocha *et al.*^{23,27} reported that the positive shift was caused by the pyroelectric polarization of GaN because the change in the semiconductor bulk potential and interface trap charges with increasing temperature makes the V_{FB} shift negligible. In fact, they used the V_{FB} shift dependence on temperature for obtaining a pyroelectric charge coefficient of $3.0\text{--}3.9 \times 10^9 \text{ q/cm}^2 \text{ K}$ ($4.8\text{--}5.6 \times 10^{-10} \text{ C/cm}^2 \text{ K}$), close to the calculated data recently reported by Liu *et al.*²⁸ Hence, it is plausible that the pyroelectric polarization charges induce the positive V_{FB} shift with the increasing temperature for C-V curves shown in Fig. 7.

As shown in Fig. 4, the post-deposition annealing process has an effect on reducing state densities, probably due to the relaxation of dangling bonds and/or point defects at the GaN surface ($\text{Al}_2\text{O}_3/\text{GaN}$ interface). A similar effect can take place during the reverse-bias annealing. In addition, there is a possibility that such relaxation of dangling bonds and defects are enhanced under reverse bias condition. In III-V semiconductors with ionic bonding nature, deep levels or gap states often have strong interaction with the host lattice, e.g., EL2 level in GaAs and DX center in AlGaAs,^{29,30} because of their localized wave functions. In this case, an electron occupation state (capture or emission of electron) at a deep level can be coupled with neighboring lattice vibration, causing lattice relaxation or distortion. During the reverse-bias annealing at 300°C , it is expected that interface states and surface defect levels emit electron (empty state). This can change the bonding configuration of neighboring atoms, thereby leading to enhanced relaxation of dangling bonds and defects at the $\text{Al}_2\text{O}_3/\text{GaN}$ interface. In case of the annealing at 300°C under forward bias condition ($V_G = +5\text{ V}$), we confirmed that the interface state density distribution was almost the same with that of the sample with the post-deposition annealing. Thus, the electron occupation condition of interface states during the annealing process is an important factor for controlling interface state densities. Another possibility is the inverse-piezoelectric effect^{31,32} under the reverse-bias annealing. It is predicted from the potential simulation that an electric field of $3\text{--}5 \times 10^5 \text{ V/cm}$ is applied to the $\text{Al}_2\text{O}_3/\text{GaN}$ interface. This induces the inverse-piezoelectric effect, corresponding to 0.5%–1.0% distortion of the GaN lattice constant. Thus, it is probable that such lattice distortion (change in atomic bonding configuration) is beneficial for the relaxation of dangling bonds or surface defects on the GaN surface during the long-time annealing. However, further study is necessary to understand the passivation mechanism on interface states.

Some research groups reported “border trap” effects in insulator-GaN interfaces.^{33,34} They observed a V_{FB} shift or a threshold voltage (V_{TH}) shift depending on the maximum forward bias voltage, thereby proposing an insulator border trap located close to E_C of GaN in energy and spatially near the insulator-GaN interface. However, the forward bias-dependent V_{FB} shift can also be explained by generation of

excess negative charges in bulk insulators caused by electron injection via leakage current. Gaffey *et al.*⁷ reported a possibility that the occupation of electron traps in the insulator by the gate leakage current induces a similar voltage shift. The border trap model is common for traditional III–V MOS system using GaAs, InP, and InGaAs.^{35–38} In those cases, remarkable frequency dispersion at accumulation bias in the experimental C–V curves is the most characteristic feature for the border trap model.^{35–38} Border traps have long time constants as they interact with the conduction band electrons via tunneling, leading to large frequency dispersion even at accumulation bias. As shown in Fig. 3, however, this is not the case for GaN MOS interfaces. The frequency dispersion is not observed at accumulation bias but rather at depletion bias. Similarly, Matocha *et al.*⁸ and Long *et al.*¹⁵ reported C–V frequency dispersion only at depletion bias. In addition, well-controlled GaN MOS interface showed negligible frequency dispersion, as shown in Fig. 3(b). These results indicate the absence of a substantial density of a border traps in the Al₂O₃/GaN interface.

In summary, we carried out the interface characterization on ALD-Al₂O₃/GaN structures using the epitaxial n-GaN layers grown on a GaN substrate with relatively low density of dislocation ($<3 \times 10^6 \text{ cm}^{-2}$). The as-deposited MOS sample showed significant frequency dispersion and a bump-like feature in C–V curves at reverse bias, showing high-density interface states in the range of $10^{12} \text{ cm}^{-1} \text{ eV}^{-1}$. On the other hand, excellent C–V characteristics with negligible frequency dispersion were observed in the MOS sample after annealing under a reverse bias condition at 300 °C in air for 3 h. The reverse-bias-annealed sample showed state densities less than $1 \times 10^{11} \text{ cm}^{-1} \text{ eV}^{-1}$ and small shifts of flat-band voltage. In addition, the C–V behavior observed at 200 °C remained almost unchanged, as compared to the RT C–V curves. These results indicate that the present process applied on a MOS structure on a high quality and low dislocation density GaN layer realizes a stable MOS structure with low interface state densities. However, during fabrication of a practical MOSFET or MOS-HEMT, the GaN or AlGaN surface is subjected to dry-etching, ion-implantation, and high-temperature annealing processes. These fabrication steps degrade the MOS interface properties, i.e., increasing interface state densities or generating surface defects on the GaN surface. It is therefore highly desirable that the final step or subsequent processes will be devoted to interface control of insulated gate structures on the processed GaN or AlGaN surface such as the reverse-bias annealing reported in this work.

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