Highly-stable and low-state-density Al2O3/GaN interfaces using epitaxial n-GaN layers grown on free-standing GaN substrates

Kaneki, Shota; Ohira, Joji; Toiya, Shota; Yatabe, Zenji; Asubar, Joel T.; Hashizume, Tamotsu

Applied physics letters, 109(16): 162104-1-162104-5

2016-10-18

http://hdl.handle.net/2115/67320

This article may be downloaded for personal use only. Any other use requires prior permission of the author and AIP Publishing. The following article appeared in Applied physics letters 109 (16) 162104, and may be found at http://aip.scitation.org/doi/abs/10.1063/1.4965296.
Highly-stable and low-state-density $\text{Al}_2\text{O}_3$/GaN interfaces using epitaxial n-GaN layers grown on free-standing GaN substrates

Shota Kaneki, Joji Ohira, Shota Toiya, Zenji Yatabe, Joel T. Asubar, and Tamotsu Hashizume

Citation: Appl. Phys. Lett. 109, 162104 (2016); doi: 10.1063/1.4965296
View online: http://dx.doi.org/10.1063/1.4965296
View Table of Contents: http://aip.scitation.org/toc/apl/109/16
Published by the American Institute of Physics
Highly-stable and low-state-density Al_{2}O_{3}/GaN interfaces using epitaxial n-GaN layers grown on free-standing GaN substrates

Shota Kaneki,¹ Joji Ohira,¹ Shota Toiya,¹ Zenji Yatabe,² Joel T. Asubar,³ and Tamotsu Hashizume¹(4)

¹Research Center for Integrated Quantum Electronics (RCIQE), Hokkaido University, Sapporo 060-0814, Japan
²Priority Organization for Innovation and Excellence, Kumamoto University, Kumamoto 860-8555, Japan
³Graduate School of Engineering, University of Fukui, Fukui 910-8507, Japan

(Received 31 May 2016; accepted 6 October 2016; published online 18 October 2016)

Interface characterization was carried out on Al_{2}O_{3}/GaN structures using epitaxial n-GaN layers grown on free-standing GaN substrates with relatively low dislocation density (< 3 × 10^{6} cm^{-2}). The Al_{2}O_{3} layer was prepared by atomic layer deposition. The as-deposited metal-oxide-semiconductor (MOS) sample showed a significant frequency dispersion and a bump-like feature in capacitance-voltage (C–V) curves at reverse bias, showing high-density interface states in the range of 10^{12} cm^{-1} eV^{-1}. On the other hand, excellent C–V characteristics with negligible frequency dispersion were observed from the MOS sample after annealing under a reverse bias at 300°C in air for 3 h. The reverse-bias-annealed sample showed state densities less than 1 × 10^{11} cm^{-1} eV^{-1} and small shifts of flat-band voltage. In addition, the C–V curve measured at 200°C remained essentially similar compared with the room-temperature C–V curves. These results indicate that the present process realizes a stable Al_{2}O_{3}/GaN interface with low interface state densities. Published by AIP Publishing.
[http://dx.doi.org/10.1063/1.4965296]

Significant progress in the crystal growth of GaN and its related semiconductors enables us to obtain a free-standing GaN substrate and a homo-epitaxial GaN layer on the GaN substrate with a relatively low dislocation density (NDIS) of 1 × 10^{6} cm^{-2} or less. Kyle et al. demonstrated that a homo-epitaxial n-GaN (NDIS = 2 × 10^{6} cm^{-2}) with a carrier density of 3.7 × 10^{16} cm^{-3} achieved a mobility of 1265 cm^{2}/Vs and 3327 cm^{2}/Vs at room temperature (RT) and 113 K, respectively. Recently, a high breakdown voltage over 4 kV and low leakage current were reported for the p'-n junction with the n-type drift layer of 40 μm fabricated on a GaN substrate with N_{DIS} = 1 × 10^{3} cm^{-2}.2 Hu et al. reported the excellent properties of the GaN p'-n diodes grown on a GaN substrate with a dislocation density of ~10^{10} cm^{-2}. The p'-n diode with an 8-μm drift layer showed a blocking voltage of over 1.4 kV and an on-state resistance (R_{ON}) of 0.12 mΩ cm^{-2}, giving the highest figure-of-merit ever reported in any semiconductor system. In addition, the Schottky diodes on the GaN layers with low dislocation densities showed nearly ideal I–V characteristics according to a simple thermionic field emission model. These results indicate highly improved crystalline quality of the current n-GaN epitaxial layers grown on the GaN substrates.

The improved crystalline quality of GaN on GaN also has become a driving force for developing vertical-type GaN transistors with metal-insulator (oxide)-semiconductor (MIS or MOS) structures. Kodama et al. successfully fabricated a trench-type GaN field-effect transistor (FET) with a SiN gate. For the trench structure, they used a combination of dry etching and subsequent wet etching with tetramethylammonium hydroxide. Recently, Oka et al. also reported a trench-type GaN MOSFET with a SiO_{2} gate, demonstrating a blocking voltage over 1.2 kV, a threshold voltage (V_{TH}) of 3.5 V, and R_{ON} of 1.8 mΩ cm^{-2}. In these cases, it was expected that the insulated gate on the dry-etched p-GaN surface could realize device operation with an inverted channel. However, the V_{TH} was much lower than the expected value calculated using the Mg doping density and the gate capacitance, indicating insufficient control of GaN surface potential by insulated gates. The control of MIS interfaces remains one of the key issues even for vertical type GaN MISFETs.

Different insulator materials have been applied to GaN-based MIS structures. Gaffey et al. reported that a SiO_{2}/SiN_{x}/SiO_{2}/n-GaN structure prepared by jet vapour deposition with the optimum process condition showed low interface state densities less than of 1 × 10^{11} cm^{-2} eV^{-1} at E_{C} −0.8 eV. Matocha et al. and Kim et al. presented low state densities at the SiO_{2}/n-GaN interfaces prepared by chemical vapor deposition (CVD) at high temperatures (830-900°C). Kambayashi et al. demonstrated an Al_{2}O_{3}/SiO_{2} bilayer gate structure achieving field-effect mobility as high as 192 cm^{2}/Vs in a recessed GaN channel structure by dry etching. An atomic layer deposition (ALD) process realized good Al_{2}O_{3}/n-GaN interface with the relatively low state densities of around 1 × 10^{11} cm^{-2} eV^{-1} at E_{C} −0.8 eV. Hashizume et al. and Watanabe et al. reported that SiN_{x}/GaN interfaces prepared by CVD with suitable pre-treatments of the GaN surface exhibited low-density interface states. However, insulator/III-N interfacial properties are still not fully controlled. In addition, major studies for the insulator-GaN interfaces have been employed on MIS structures fabricated on heteroepitaxial GaN layers grown on SiC, Si, and sapphire substrates. There are a limited number of papers reporting on interface properties of MOS structures using a free-standing GaN substrate.
GaN or homo-epitaxial GaN with low dislocation densities.\textsuperscript{15–17} In this letter, accordingly, we report on fabrication and characterization of $\text{Al}_2\text{O}_3$/n-GaN structures using homo-epitaxial GaN layers grown on a GaN substrate with a relatively low dislocation density, particularly focusing on interface state densities and the stability of capacitance-voltage (C–V) behavior.

Figure 1 shows an $\text{Al}_2\text{O}_3$/n-GaN MOS structure prepared by ALD. We used a homo-epitaxial Si-doped GaN layer with a thickness of 4 \textmu m grown on an n$^+$/Ga$_2$O$_3$ substrate with a relatively low dislocation density ($<$ 3 \times 10$^{10}$ cm$^{-2}$). The donor density is 6.2 \times 10^{16} \text{cm}^{-3}, which was determined by a C–V method using a Schottky diode. After the pre-treatment of the n-GaN surface in a 30%-HF solution for 1 min, the $\text{Al}_2\text{O}_3$ layer with a nominal thickness of 30 nm was deposited on the n-GaN surface using an ALD system (SUGA-SAL1500) at 350 °C. In the deposition process, water vapor and trimethylaluminum were introduced into a reactor in alternate pulse forms. Each precursor was injected into the reactor for 15 ms, and the purging time was set to 5 s. In this case, the deposition rate is 0.11 nm/cycle, indicating the formation of $\text{Al}_2\text{O}_3$ in a layer-by-layer fashion. For some samples, a post-deposition annealing was carried out in N$_2$ for 30 min at 400 °C. A circular Ni/Au (20/50 nm) with a diameter of 200 \textmu m was deposited on the $\text{Al}_2\text{O}_3$ surface as a gate electrode.

From an ellipsometry measurement, the refractive index of the ALD $\text{Al}_2\text{O}_3$ was estimated to be 1.60–1.65, which is close to the values reported for the amorphous $\text{Al}_2\text{O}_3$ films prepared by sputtering and ALD methods.\textsuperscript{18,19} Figure 2 shows a cross-sectional transmission electron microscope (TEM) image of the as-deposited $\text{Al}_2\text{O}_3$/Ga$_2$O$_3$ interface fabricated on the GaN substrate. The sample has an abrupt and flat interface, indicating low-energy and layer-by-layer characteristics resulting from the ALD process. There is no detectable transition layer like native oxide of GaN at the $\text{Al}_2\text{O}_3$/Ga$_2$O$_3$ interface. In addition, $\text{Al}_2\text{O}_3$ is amorphous and remained unchanged, i.e., no phase transformation even after post-deposition annealing process in the temperature range of 300–500 °C. This is consistent with the fact that the phase transformation of $\text{Al}_2\text{O}_3$ films from amorphous to crystalline happens at temperature of 800 °C or higher.\textsuperscript{11,20}

Figure 3(a) shows the room-temperature (RT) C–V characteristics of the as-deposited $\text{Al}_2\text{O}_3$/n-GaN/n$^+$-GaN diode (without annealing) in a wide measurement frequency range of 1 Hz to 1 MHz. The sample showed a significant frequency dispersion at reverse bias. By lowering the frequency of the ac measurement signal, deeper interface states are expected to respond accordingly to an ac signal. This allows more of the states to follow the ac frequency and thereby contribute an additional component to the measured capacitance. Similar frequency dispersions in C–V characteristics were reported for SiO$_2$/GaN and $\text{Al}_2\text{O}_3$/GaN structures.\textsuperscript{7,8,15} In addition, bump-like C–V curves at low frequencies indicate the existence of a discrete level with relatively high density at the GaN surface. On the other hand, excellent C–V characteristics with negligible frequency dispersion were
observed in the MOS sample after the annealing in air at 300 °C for 3 h under a reverse bias voltage of −10 V, as shown in Fig. 3(b). The C–V curves of the bias-annealed sample are very close to the calculated curve (broken line) with no such bump-like behavior in a very wide frequency range of 1 Hz–1 MHz. There is a difference of flat-band voltage (VFB) between samples without and with the reverse-bias annealing. Again, on the one hand, the annealed sample exhibited a VFB very close to the calculated value; while, on the other hand, the as-deposited sample showed a VFB shift toward the negative bias direction, probably due to excess positive charges arising from donor-type interface states toward the negative bias direction, probably due to excess air at 300° C. The reverse-bias annealing process in the hetero-epitaxial GaN sample was limited in densities of 5 × 10¹¹ cm⁻² eV⁻¹ or higher remained. On the other hand, the reverse-bias annealing in air at 300 °C for 3 h resulted in a significant reduction in state density. In fact, the reverse-bias-annealed sample showed a state density below the detection limit (<1 × 10¹¹ cm⁻² eV⁻¹) except for those energies near the conduction band edge, corresponding to nearly ideal C–V curves without frequency dispersion as shown in Fig. 3(b). The interface state density distribution of the MOS sample using a hetero-epitaxial GaN on the sapphire substrate is shown in Fig. 4(b). Even after the reverse-bias annealing process, the reduction of interface states for the hetero-epitaxial GaN sample was limited in densities of 2 × 10¹¹ cm⁻² eV⁻¹ or higher. It is likely that a high dislocation density accompanies high-density surface defects and/or disorder in atomic bonding on the GaN surface, leading to the limited improvement of MOS interface properties by the reverse-bias annealing.

We then investigated the stability of the MOS interface with the reverse-bias annealing. Figure 5 shows the leakage current characteristics of the Al₂O₃/n-GaN/n⁺-GaN structure. A sufficiently low leakage current (close to the detection limit) was observed at reverse bias. As we have confirmed the linear relation of log (J/E²) vs 1/E (here, J is the current density and E is the electric field), the slight increase in the current at forward bias larger than 10 V is likely due to the Fowler-Nordheim (FN) tunneling mechanism. Figure 6 shows the evolution of the flat-band voltage VFB as a function of the maximum forward bias voltage VMF. In this case, the C–V sweeping was carried out from VMF to −10 V. The reverse-bias annealed sample showed an almost constant VFB, originating from low interface state densities. When the VMF exceeds 10 V, the VFB slightly shifts toward the positive bias direction. In this bias range, as shown in Fig. 5, the leakage current gradually increases. This probably causes electron injection into the Al₂O₃ layer with the

![FIG. 4. Interface state density (Dₐ) distributions determined by applying the Terman method to 1-MHz C–V results for (a) Al₂O₃/GaN/n⁺-GaN and (b) Al₂O₃/GaN/sapphire structures.](image)

![FIG. 5. Gate leakage current of the Al₂O₃/n-GaN/n⁺-GaN structure annealed in air at 300 °C for 3 h under a reverse bias voltage of −10 V.](image)
resultant excess negative charges producing the shift of $V_{\text{FB}}$ toward the positive bias direction. However, Fig. 6 showed that the $V_{\text{FB}}$ shift was limited within 250 mV, indicating a stable interface behavior of the reverse-bias annealed sample.

Figure 7 shows the C–V characteristics measured at 200 °C for the Al$_2$O$_3$/n-GaN/n$^+$-GaN structure with the reverse-bias annealing. For high temperature C–V measurements, it is expected that deeper interface states can respond both to bias sweeping and ac signal modulation, causing changes in C–V characteristics compared with those measured at RT. In fact, Matocha et al.,23,27 Ooyama et al.,24 and Long et al.,15 reported significant stretch-out of C–V curves, bump-like C–V behavior, and enhanced frequency dispersion for SiO$_2$/GaN and Al$_2$O$_3$/GaN structures at measurement temperatures from 175 to 300 °C. Such unstable C–V behavior at high temperatures indicates that relatively high-density interface states can cause operation instability in GaN-based MOSFETs. In our reverse-bias annealed sample, however, the high-temperature C–V behavior remained almost unchanged, as compared with the RT C–V curves shown in Fig. 3(b). In particular, negligible frequency dispersion and the same C–V slope were observed even at high temperature of 200 °C. These results indicate that the present process applied on a MOS structure on a high quality and low dislocation density GaN layer realizes a stable MOS structure with low interface state densities. For the practical device application, we applied the present control process to the Al$_2$O$_3$/AlGaN/GaN HEMT. A preliminary result showed that the present process leads to improved $g_m$ linearity, probably due to the reduction of state densities at the Al$_2$O$_3$/AlGaN interface. Thus, we expect that the present annealing process has also favorable impact on Al$_2$O$_3$/AlGaN/GaN structures.

As shown in Fig. 7, a slight $V_{\text{FB}}$ shift (0.3–0.4 V) toward the positive bias direction was observed in the C–V curve measured at 200 °C, as compared to the RT C–V curve [Fig. 3(b)]. Since the annealed sample showed very low interface state densities and negligible frequency dispersion in C–V curves, it is unlikely that interface states or oxide levels are the ones responsible for the positive $V_{\text{FB}}$ shift. The positive $V_{\text{FB}}$ shift with increasing temperature was also reported for SiO$_2$/GaN structures.23,25–27 Matocha et al.23,27 reported that the positive shift was caused by the pyroelectric polarization of GaN because the change in the semiconductor bulk potential and interface trap charges with increasing temperature makes the $V_{\text{FB}}$ shift negligible. In fact, they used the $V_{\text{FB}}$ shift dependence on temperature for obtaining a pyroelectric charge coefficient of $3.0–3.9 \times 10^9$ q/cm$^2$ K ($4.8–5.6 \times 10^{-10}$ C/cm$^2$ K), close to the calculated data recently reported by Liu et al.28 Hence, it is plausible that the pyroelectric polarization charges induce the positive $V_{\text{FB}}$ shift with the increasing temperature for C–V curves shown in Fig. 7. As shown in Fig. 4, the post-deposition annealing process has an effect on reducing state densities, probably due to the relaxation of dangling bonds and/or point defects at the GaN surface (Al$_2$O$_3$/GaN interface). A similar effect can take place during the reverse-bias annealing. In addition, there is a possibility that such relaxation of dangling bonds and defects are enhanced under reverse bias condition. In III–V semiconductors with ionic bonding nature, deep levels or gap states often have strong interaction with the host lattice, e.g., EL2 level in GaAs and DX center in AlGaN,29,30 because of their localized wave functions. In this case, an electron occupation state (capture or emission of electron) at a deep level can be coupled with neighboring lattice vibration, causing lattice relaxation or distortion. During the reverse-bias annealing at 300 °C, it is expected that interface states and surface defect levels emit electron (empty state). This can change the bonding configuration of neighboring atoms, thereby leading to enhanced relaxation of dangling bonds and defects at the Al$_2$O$_3$/GaN interface. In case of the annealing at 300 °C under forward bias condition ($V_G = +5$ V), we confirmed that the interface state density distribution was almost the same with that of the sample with the post-deposition annealing. Thus, the electron occupation condition of interface states during the annealing process is an important factor for controlling interface state densities. Another possibility is the inverse-piezoelectric effect31,32 under the reverse-bias annealing. It is predicted from the potential simulation that an electric field of $3–5 \times 10^5$ V/cm is applied to the Al$_2$O$_3$/GaN interface. This induces the inverse-piezoelectric effect, corresponding to 0.5%–1.0% distortion of the GaN lattice constant. Thus, it is probable that such lattice distortion (change in atomic bonding configuration) is beneficial for the relaxation of dangling bonds or surface defects on the GaN surface during the long-time annealing. However, further study is necessary to understand the passivation mechanism on interface states.

Some research groups reported “border trap” effects in insulator-GaN interfaces.33,34 They observed a $V_{\text{FB}}$ shift or a threshold voltage ($V_{\text{TH}}$) shift depending on the maximum forward bias voltage, thereby proposing an insulator border trap located close to $E_C$ of GaN in energy and spatially near the insulator-GaN interface. However, the forward bias-dependent $V_{\text{FB}}$ shift can also be explained by generation of
excess negative charges in bulk insulators caused by electron injection via leakage current. Gaffey et al.\textsuperscript{7} reported a possibility that the occupation of electron traps in the insulator by the gate leakage current induces a similar voltage shift. The border trap model is common for traditional III–V MOS systems using GaAs, InP, and InGaAs.\textsuperscript{35–38} In those cases, remarkable frequency dispersion at accumulation bias in the experimental C–V curves is the most characteristic feature for the border trap model.\textsuperscript{35–38} Border traps have long time constants as they interact with the conduction band electrons via tunneling, leading to large frequency dispersion even at accumulation bias. As shown in Fig. 3, however, this is not the case for GaN MOS interfaces. The frequency dispersion is not observed at accumulation bias but rather at depletion bias. Similarly, Matocha et al.\textsuperscript{10} and Long et al.\textsuperscript{15} reported C–V frequency dispersion only at depletion bias. In addition, well-controlled GaN MOS interface showed negligible frequency dispersion, as shown in Fig. 3(b). These results indicate the absence of a substantial density of a border traps in the Al$_2$O$_3$/GaN interface.

In summary, we carried out the interface characterization on ALD-Al$_2$O$_3$/GaN structures using the epitaxial n-GaN layers grown on a GaN substrate with relatively low density GaN layer realizes a stable MOS structure with low interface state densities. However, during fabrication of a practical MOSFET or MOS-HEMT, the GaN or AlGaN surface is subjected to dry-etching, ion-implantation, and high-temperature annealing processes. These fabrication steps degrade the MOS interface properties, i.e., increasing interface state densities or generating surface defects on the GaN surface. It is therefore highly desirable that the final step or subsequent processes will be devoted to interface control of insulated gate structures on the processed GaN or AlGaN surface such as the reverse-bias annealing reported in this work.

This work was partially supported by JSPS KAKENHI Grant No. JP16H06421 and Council for Science, Technology and Innovation (CSTI), Cross-ministerial Strategic Innovation Promotion Program (SIP), “Next-generation power electronics” (Funding Agency: NEDO).

\textsuperscript{9}E. Kim, N. Soejima, Y. Watanabe, M. Ishikyo, and T. Kachi, Jpn. J. Appl. Phys. 49, 04DF08 (2010).
\textsuperscript{29}G. Vincent and D. Bois, Solid State Commun. 27, 431 (1978).
\textsuperscript{31}J. A. del Alamo and J. Joh, Microelectron. Reliab. 49, 1200 (2009).