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Detection of deep-level defects and reduced carrier concentration in Mg-ion-implanted GaN before high-temperature annealing

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We report experimental results for the detection of deep-level defects in GaN after Mg ion implantation before high-temperature annealing. The n-type GaN samples were grown on GaN free-standing substrates by metalorganic vapor phase epitaxy. Mg ions were implanted at 50 keV with a small dosage of 1.5×10^{11} cm^{-2}, which did not change the conduction type of the n-GaN. By depositing Al_2O_3 and a Ni/Au electrode onto the implanted n-GaN, metal-oxide-semiconductor (MOS) diodes were fabricated and tested. The measured capacitance–voltage (C–V) characteristics showed a particular behavior with a plateau region and a region with an anomalously steep slope. Fitting to the experimental C–V curves by simulation showed the existence of deep-level defects and a reduction of the carrier concentration near the GaN surface. By annealing at 800°C, the density of the deep-level defects was reduced and the carrier concentration partially recovered. https://doi.org/10.1063/1.5017891

GaN is an attractive material that has been used to achieve light-emitting diodes with high luminescence.[1,2] Recently, the application of this material to efficient power electronic devices has attracted interest.[3,4] For this purpose, the device fabrication process will greatly benefit from ion implantation technology. However, the formation of a p-type region on GaN by ion implantation is difficult. The high defect density in GaN grown on a sapphire substrate might have been a reason for the unsuccessful formation of a p-type region. Very recently, the successful formation of p-type regions on GaN epitaxial layers on free-standing GaN substrates by Mg ion implantation has been confirmed by observing the rectifying characteristics of p-n junctions formed by applying multicycle rapid thermal annealing,[5,6] standard high-temperature annealing,[7,8] and coimplantation of the N-face of GaN with Mg and H ions.[9] However, it has been reported that defects remain in the Mg-implanted GaN layer even after high-temperature annealing on the basis of positron annihilation spectroscopy (PAS) and photoluminescence (PL) studies.[10,11] To control the electrical properties of Mg-implanted GaN, an electrical measurement should be carried out to understand the thermal behavior of the defects by starting from a sample before high-temperature annealing for the activation of Mg acceptors. We here report measurement results of the electrical properties of a Mg-implanted GaN layer on a free-standing GaN substrate before high-temperature annealing.

We used metal-oxide-semiconductor (MOS) structures for the test samples to avoid the difficulty in the electrical measurement of a Schottky barrier diode, *i.e.*, the limitation in the bias-dependent charge/discharge of the deep-level defects in the implanted region near the surface. The preparation sequence of the samples is illustrated in Fig. 1. A Si-doped GaN epitaxial layer was grown by metalorganic vapor phase epitaxy on a free-standing n^+-GaN (0001) substrate produced by hydride vapor phase epitaxy. The thickness and carrier concentration of the n-type GaN epitaxial layer were 3 μm and 5×10^{17} cm^{-3}, respectively. Mg ions were implanted at room temperature with an energy

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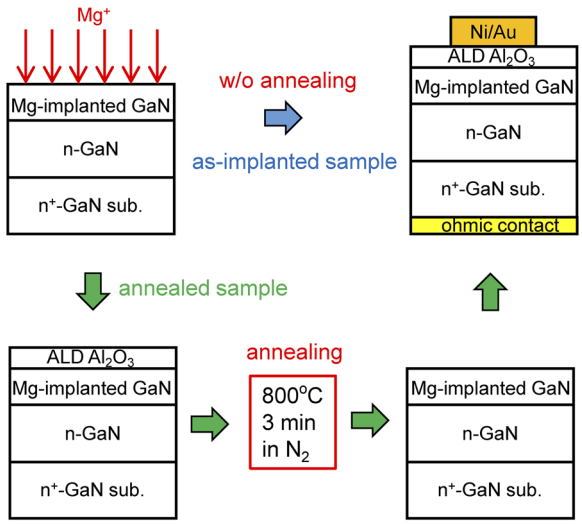

FIG. 1. Sample fabrication sequence.

of 50 keV, a dosage of 1.5×10^{11} cm^{-2}, and an incident angle of 7° with respect to the normal. We fabricated two samples. For one sample, a 30-nm-thick Al_2O_3 layer was deposited by atomic layer deposition (ALD) at 300°C using H_2O and trimethylaluminum, followed by Ni/Au electrode formation using the photolithographic lift-off technique to complete the MOS structure. The other sample was annealed at 800°C for 3 min in a nitrogen flow after the Mg implantation using a 20-nm thick ALD Al_2O_3 layer as a surface protection layer. Then the Al_2O_3 cap layer was removed using buffered HF (BHF, HF:NH_4OH=1:5) solution prior to the deposition of a 30-nm-thick ALD Al_2O_3 layer and Ni/Au electrode formation. For both samples, a back ohmic contact was formed by depositing Ti/Au. Post-metallization annealing (PMA) was carried out at 300°C in air for 3 hours to reduce the interface state density for both samples. Although this PMA method was originally carried out while applying a reverse bias voltage,[12] here a reverse bias voltage was not applied because it might have damaged the implanted sample. The distribution of implanted Mg calculated using TRIM implant simulation software is plotted in Fig. 2. Since the maximum Mg concentration is much lower

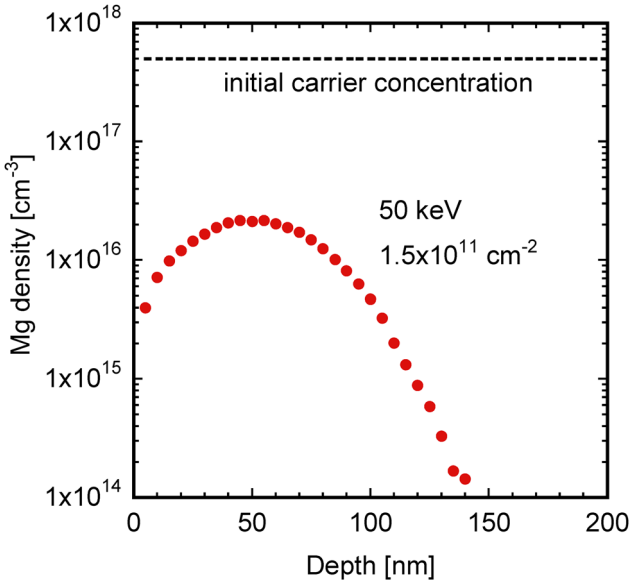

FIG. 2. TRIM simulation result.

than the initial carrier concentration (n-type with Si dopant), the fabricated MOS diodes were tested as n-type MOS diodes. Using this method, we can investigate the electrical characteristics before high-temperature annealing while avoiding the amorphization of GaN. For the completed MOS diodes, capacitance–voltage (C–V) measurement was carried out.

The results of the C–V measurement at frequencies of 1 kHz – 1 MHz and a bias sweep rate of 50 mV/s for the sample with the as-implanted GaN layer are shown in Fig. 3, where an anomalous plateau can be seen, indicating the existence of discrete states in the band gap. The frequency dispersion is small, which indicates that the interface state density at the Al_2O_3/GaN interface due to interface disorder was reduced by PMA. Although the hysteresis is shown for only the 1 MHz curve to avoid complexity, similar hysteresis was observed for each measurement frequency. The hysteresis is larger for a lower capacitance, which indicates the existence of deep-level states. The C–V curve at a higher capacitance shows a steeper slope than that of the ideal curve assuming no implantation, which indicates that the carrier concentration was reduced near the surface of the implanted GaN layer.

To derive the density of interface states and deep-level states from the measured C–V curve, fitting by a simulation assuming the density of interface states is required. We used simulation software developed by Miczek et al.[13,14] The fitting result for the measured 1 MHz C–V curve in the negative to positive direction in Fig. 3 is plotted in Fig. 4(a), where the interface state density, D_{it}, distribution shown in Fig. 4(b) and the carrier concentration profile indicated in Fig. 4(c) were assumed in the simulation. Here the carrier concentration in the implanted region was measured by a fast-bias-sweep C–V measurement in which the interface states could not respond to the bias sweep (1 kV/s). Therefore, the D_{it} was uniquely determined. As described above, the plateau in the C–V curve indicates the existence of discrete states. As indicated by the solid line in Fig. 4(a), the simulation assuming the D_{it} distribution in Fig. 4(b) with a reduced carrier concentration, n, of 6.4×10^{16} cm^{-3} in the near-surface region up to a depth of 100 nm (roughly corresponding to the implanted region of Mg in Fig. 2), as shown in Fig. 4(c), gives an excellent fitting. This result shows that discrete states at an energy of 0.76 eV from the conduction band edge, E_C, appeared upon the Mg ion implantation of GaN, which was accompanied by a reduction of the carrier concentration in the implanted region. Note that the interface states originating from the interface disorder should produce a U-shaped distribution over the entire band gap.[15] Therefore, the detected discrete states should have resulted from the deep-level defects in the GaN layer.

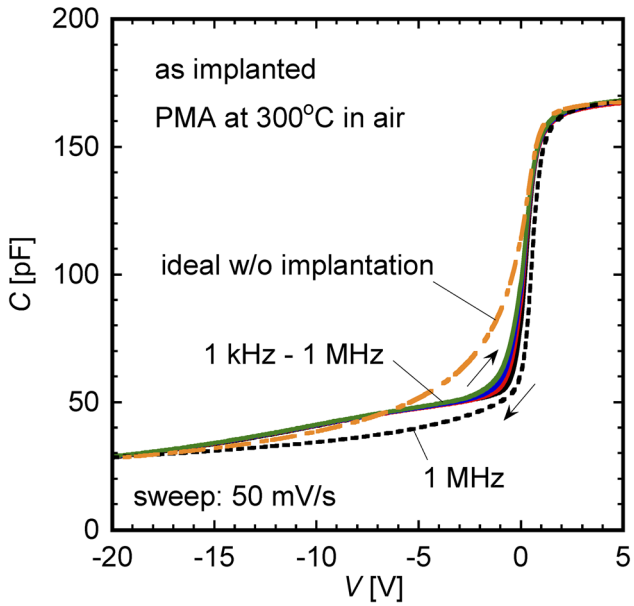

FIG. 3. Measured C–V curve for MOS diode with as-implanted GaN layer.

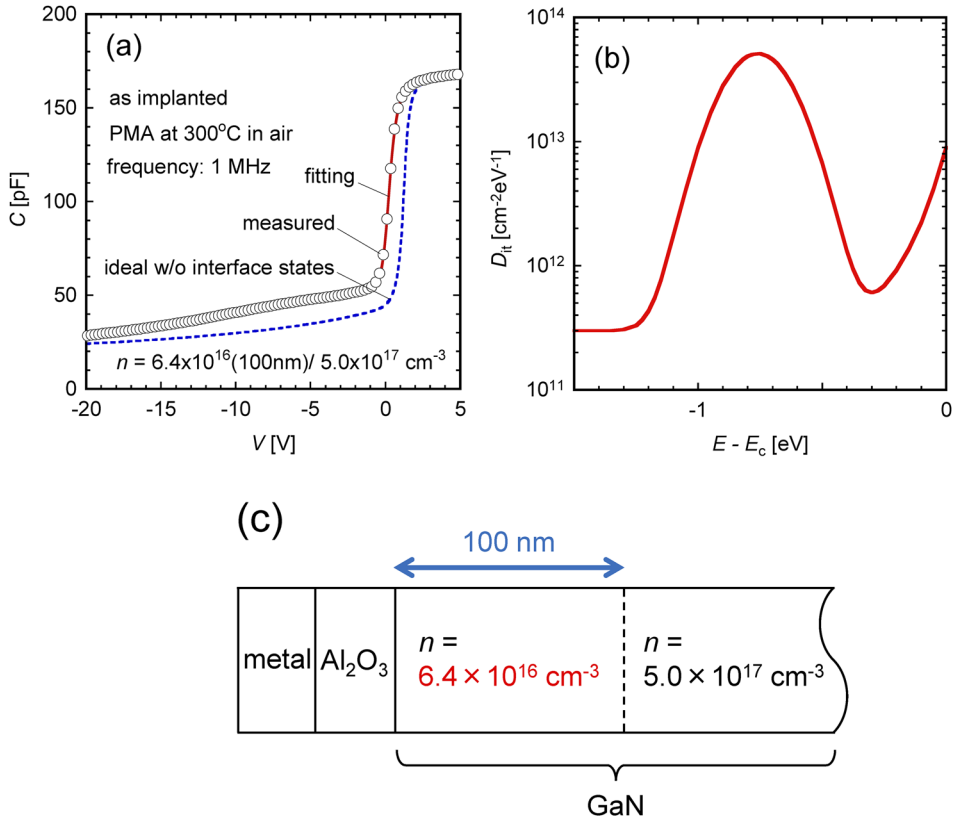

FIG. 4. Simulation results for 1 MHz *C*–*V* curve for MOS diode with as-implanted GaN layer. (a) Fitting result, (b) assumed D_{it} distribution, and (c) assumed carrier concentration profile.

The Mg ion implantation should have produced intrinsic point defects, leading to the generation of the detected discrete states. The TRIM simulation indicates that more than two orders higher density of Ga and N vacancies, V_{Ga} and V_N, respectively, than that of Mg atoms can be produced in GaN by Mg implantation. The volume density of the detected discrete states in Fig. 4(b) can be estimated to be at least 10^{18} cm^{-3}, even assuming a wide distribution in the implanted region (~100 nm from the surface), which is much higher than the Mg atom concentration. Therefore Mg-related defects are unlikely to be the origin of the detected discrete states. In a previous report,[16] deep-level states were detected at $E_C - E = 0.67$ eV after N ion implantation with a dosage of 1×10^{11} cm^{-2} (a similar dosage to the present samples), and the density of the deep-level states was found to decrease after subsequent annealing at 900°C. It was proposed that a possible origin of the deep-level defects was a N interstitial, N_i. However, a theoretical study[17] showed that the N_i produced an acceptor-like defect level at $E_C - E = 0.99$ eV. If this amount of discrepancy in the energy location is allowed, the following discussion is possible. In Fig. 4(a), the ideal curve assuming no interface states is also plotted. Compared with this curve, the plateau of the measured curve appeared on the negative-bias side, which likely indicates that the detected deep-level states are donor-like states.[14] According to the theoretical calculation,[17] a gallium interstitial, Ga_i, produces a donor-like state at $E_C - E = 0.94$ eV. Therefore, Ga_i is a possible candidate for the detected deep-level defects. However, since the interface-fixed charges might have caused a shift of the *C*–*V* curve as large as 10 V, we cannot completely rule out the possibility of the detected states being acceptor-like states, *e.g.*, N_i, V_{Ga}, and Ga antisites.[17] Nevertheless, the shift of the *C*–*V* curve by 10 V requires a high density of interface-fixed charges of 1.5×10^{13} cm^{-2}, which seems unlikely. On the other hand, Ref. 10 reported that the $V_{Ga}(V_N)_2$ complexes were detected by PAS for a sample after Mg implantation before annealing. However, since the dosage was sufficiently low in the present work, a probability of formation of a defect complex should have been low. Anyway, at this stage, we cannot

discuss the energy location in the band gap for the defect levels produced by such large complexes because no theoretical predictions or measurement results have been reported to the best of our knowledge.

To observe the thermal behavior of the detected deep-level defects, annealing at 800°C was carried out. This temperature is considerably lower than that required for Mg activation, typically above 1,200°C, which enables us to investigate whether the reduction in the carrier concentration was caused by defects while avoiding the activation of Mg acceptors. The measured *C*–*V* curve for the MOS diode with GaN annealed at 800°C after implantation is shown in Fig. 5. The frequency dispersion is again small owing to the reduction of the interface states by PMA. Although the wide plateau disappeared, a dip remained in the *C*–*V* curve, which shows that the deep-level states existed even after annealing at 800°C.

Figure 6(a) shows the result of fitting to the *C*–*V* curve measured at 1 MHz for the MOS diode with GaN annealed after implantation. The fitting curve in Fig. 6(a) was calculated assuming the D_{it} distribution plotted in Fig. 6(b) (solid line) and a partially recovered carrier concentration of 2.6×10^{17} cm^{-3} in the near-surface region shown in Fig. 6(c). Again, the carrier concentration in the implanted region was measured by a fast-bias-sweep *C*–*V* measurement. Therefore, the D_{it} was uniquely determined. In Fig. 6(b), the D_{it} distribution for the sample before annealing is also plotted by a broken line. It can be seen that the deep-level state density was reduced markedly. The energy location, $E_C - E = 0.58$ eV, of the detected deep-level states was different from that of the as-implanted sample. Comparing the location of the measured *C*–*V* curve with that of the ideal curve assuming no interface states, also plotted in Fig. 6(b), the detected deep-level states were again likely donor-like states. However, considering the effect of the interface fixed charge on the *C*–*V* curve, there is also a possibility of the detected states being acceptor-like states.

The origin of the detected deep-level states at $E_C - E = 0.58$ eV that appeared after annealing at 800°C may have been related to surface damage. MOS diode samples using n-GaN without implantation were also fabricated in the same way as the implanted samples and tested. The *C*–*V* curve for the sample with 800°C-annealed GaN was similar to that in Fig. 5. Applying the Terman method to this sample, the derived D_{it} indicated similar deep-level states around $E_C - E = 0.6$ eV even after PMA in air. However, no deep-level states were detected for an as-grown GaN MOS diode after PMA. Thus, it is possible that the annealing at 800°C generated the deep-level states near the GaN surface. It has been predicted by calculation that simple defects, V_{Ga} and anti-site defects, produce

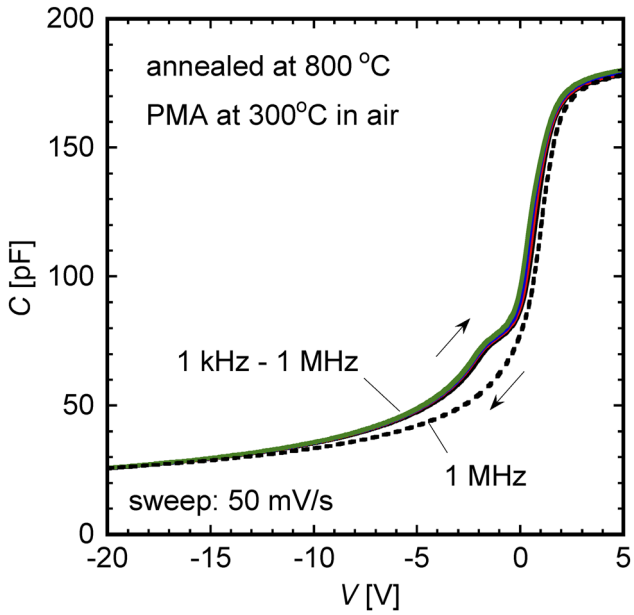

FIG. 5. Measured *C*–*V* curve for MOS diode with GaN layer annealed at 800°C after implantation.

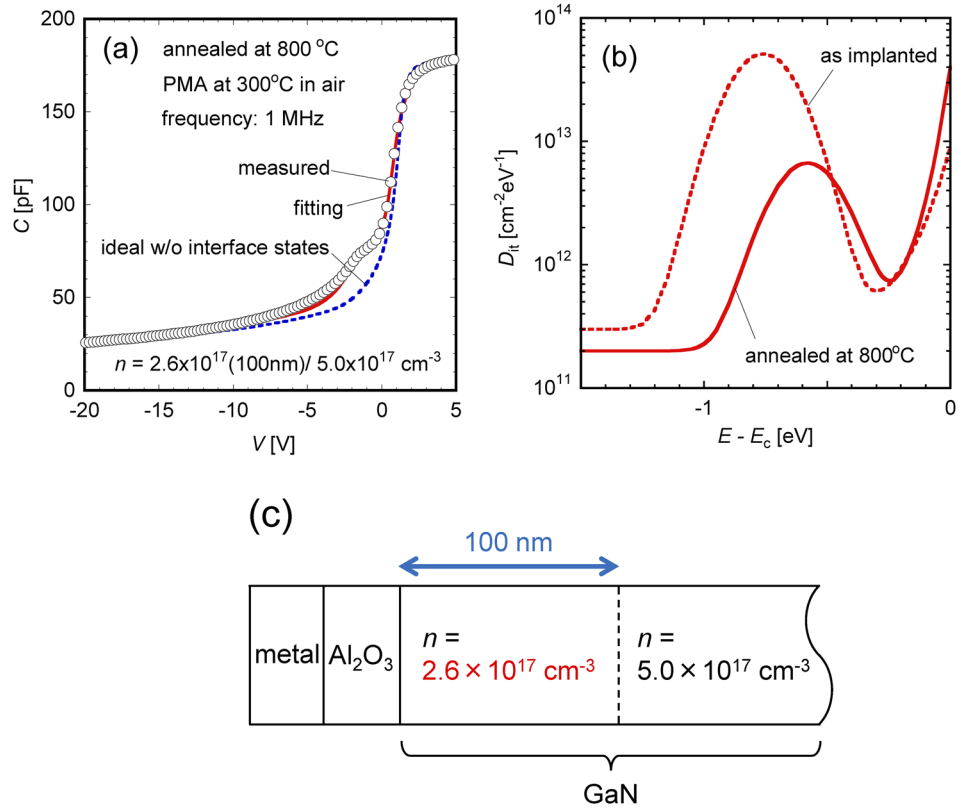

FIG. 6. Simulation results for 1 MHz C–V curve for MOS diode with GaN layer annealed at 800°C after implantation. (a) Fitting result, (b) assumed D_{it} distribution, and (c) assumed carrier concentration profile.

states near this energy location,[17] while some V_N-related defects are also likely to be the origin considering the annealing temperature.

The measured C–V curves indicated that the reduction and recovery of the carrier concentration occurred upon the implantation and subsequent annealing, respectively. There is a possibility that the defects generated by the Mg ion implantation caused carrier compensation. Since several types of deep-level states have been predicted to be located at the mid-gap and near the valence band,[17] we cannot determine the origin of the observed reduction in the carrier density at this stage.

In summary, we investigated the electrical behavior of Mg-ion-implanted GaN using MOS diodes. Anomalous behavior of the C–V characteristics was observed for the MOS diode consisting of as-implanted GaN, which was interpreted as the existence of deep-level states and the reduction of the carrier concentration in the implanted region. In the MOS diode consisting of GaN annealed at 800°C after Mg ion implantation, the carrier concentration was recovered and the deep-level state density decreased upon annealing. Possible origins of the defect states and the reduction in the carrier concentration have been discussed.

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