Implementation of a noise-coexistence threshold logic architecture on a GaAs-based nanowire FET network

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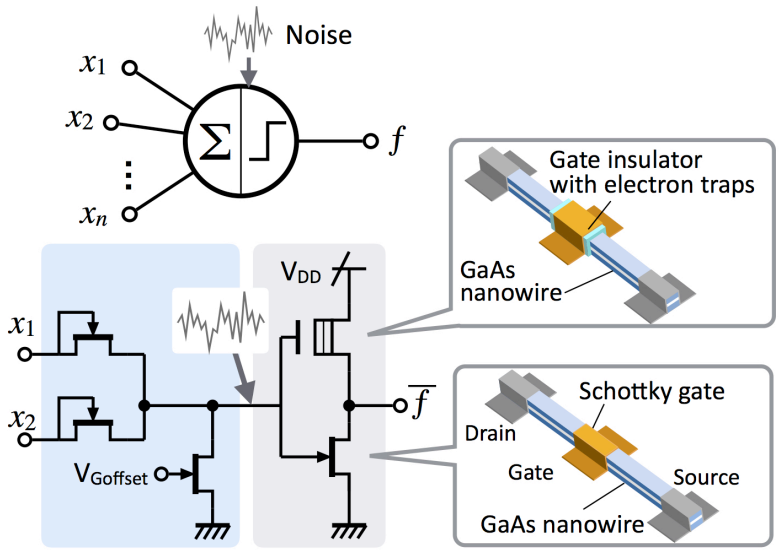

Implementation of a noise-coexistence threshold logic architecture on a GaAs-based nanowire FET network

We study reconfigurable and noise-coexistence information processing system utilizing nanostructures. We implement a threshold logic circuit and a double threshold function using a GaAs-based nanowire field-effect transistor (FET) network. A noise coexistence capability is based on a noise-assisted state transition in a threshold function in a threshold logic element. We fabricate a circuit reconfigurable between NAND and NOR functions. A hysteresis transfer characteristic with double threshold is realized in the GaAs nanowire by using a silicon nitride (SiN) as the gate insulator. We introduce a unique inverter design using the SiN-gate FET as a load to achieve the transfer characteristic with clockwise hysteresis, similar to a Schmitt trigger.

Keywords: word; Semiconductor nanowire network, threshold logic, hysteresis, noise

Introduction

A reconfigurability of a circuitry and its ability to operate in noisy condition are attractive options for ultra-low-power information processing systems. Highly energy-efficient information processing of the biological systems is understood to partly arise from these strategies [1,2]. In a high-density implementation utilizing semiconductor nanostructures and single molecule networks, both the logical and physical architectures of the system should be simple as possible. The threshold logic [3,4] is the one of the possible logic architectures having a simple structure and reconfigurable capability. In this system, a fundamental Boolean function is represented by a summer and a threshold device and the function can be changed by shifting the threshold value. A potential approach for the noise coexistence is to use the noise-induced phenomenon in the threshold system such as stochastic resonance (SR), where the response to a weak signal

is optimized by adding noise [5,6]. The combination of the threshold logic and the stochastic resonance is known as logical stochastic resonance [7,8]. In this paper, we investigate the implementation of the threshold logic circuit by integrating nanowire field-effect transistor (FET) together with double threshold function. The double threshold function having an appropriate hysteresis loop is known to show better SR response with a signal-to-noise ratio gain [9]. For implementation of such device and circuit, we apply our circuit technology using a GaAs-based nanowire network structure [10-16]. Previously we demonstrated a NOR gate operation of the threshold logic circuit, although the changing function has not been achieved yet [17]. Our unique technique to cause the stochastic resonance in the nanowire FET [18,19] is also applied to the inverter for the threshold function.

Concept and design

The basic concept of the threshold logic circuit in this study is shown in **Fig. 1**. A simple threshold logic element consists of a summer and a threshold transfer function as shown in **Fig. 1(a)**. The output f of the element is "1" when the sum of the multiple inputs exceeds the threshold value θ, else "0" [3,4]. Namely,

$$\text{If } \sum_i x_i \geq \theta \text{ then } f = 1 \text{ else } f = 0, \qquad (1)$$

where x_i is the input and θ is a threshold value. In this study a two-variable binary logic, $i = \{0, 1\}$, is considered. As shown in the waveforms in the right of **Fig. 1(a)**, if the threshold is low, $\theta = \theta_L$, the circuit operates as an OR gate, else if the threshold is high, $\theta = \theta_H$, it operates as an AND gate.

Our design of a two-variable threshold logic circuit using the GaAs-based

nanowire FETs is shown in **Fig. 1(b)**. This circuit is designed using only the n-channel FETs, whereas the conventional Si CMOS (complementary metal-oxide-semiconductor) architecture uses both n- and p-channel FETs that makes the physical structure and the fabrication process complicated. The input voltage signal are converted to the current and summed at the node on the basis of Kirchhoff's laws. The current sum is again converted to the voltage signal through a resistor FET in the middle of the diagram, then the voltage is inputted to an inverter operating as a threshold function. Then the output of the circuit gives the invert of f and the system operates as NOR or NAND gate. The input level of the inverter can be adjusted by changing the conductance of the resistor FET through adjusting its gate voltage, V_{Goffset}. The relative threshold between the inverter and the input signal is changed by V_{Goffset} and the logic function can be changed.

The mechanism for the noise coexistence of this system is in the inverter shown in **Fig. 1(b)**. This inverter consists of a silicon-nitride (SiN) insulated-gate FET as a load FET and a conventional Schottky-gate nanowire FET as a driver, whereas previously we discussed the inverter using the SiN-gate FET as the driver [17]. The double threshold characteristic is obtained owing to the thin SiN insulator having electron traps. Gate voltage-dependent charging and discharging of the electron traps causes the hysteresis in the transfer characteristic [13,20]. It shows a clockwise hysteresis loop. The conductance of the FET is changed to inhibit the signal transmission by the increased input signal. The inverter having the SiN-gate FET as the driver also shows the inhibitory response even though it exhibits double threshold voltage transfer curve. To obtain the enhanced stochastic resonance response, we need an inverter having a clockwise hysteresis like a Schmitt trigger. Then we use the SiN-gate FET as the load of the inverter and the input signal is also given to it. If the input signal exceeds the high threshold, the driver FET turns on and the load FET moves to

the low conductance state simultaneously. Then the threshold of the inverter shifts to low one. This means that the increased input signal promotes the system to respond to the weak signal.

Device and circuit fabrication

We fabricated a threshold logic circuit with a conventional inverter for demonstrating the changing the logic function. The inverters integrating a nanowire SiN-gate nanowire FET and a conventional FET were also fabricated and characterized. **Figure 2** shows a scanning electron microscope (SEM) image of the two-variable threshold logic circuit together with the circuit diagram and a magnified view of a FET. The GaAs nanowires were formed by electron beam (EB) lithography and H_2SO_4-based wet chemical etching of an AlGaAs/GaAs modulation doped heterostructure on a (001) GaAs substrate, where (001) is direction index of crystal plane. It had two-dimensional electron gas in the AlGaAs/GaAs interface, which had high electron mobility of 5,000 cm^2/Vs at room temperature and contributed the abrupt threshold transfer characteristic of the FET. The nanowire directions were <-110> for the FET channel and <110> for the FET-to-FET wiring, where <-110> and <110> are crystal plane indices. Then a 10-nm SiN insulator was deposited by ECR (electron cyclotron resonance) plasma-enhanced chemical vapor deposition (CVD) at a substrate temperature of 260 °C. After that, the SiN layer was partly removed in the the Schottky gate and ohmic contact portions by buffered hydrogen fluoride through the resist mask. The ohmic contacts for the source and drain electrodes were formed on the nanowires by EB lithography, germanium/gold/nickel (Ge/Au/Ni) metal-stack deposition, lift-off, and alloying. The gate metal was formed on the nanowires by EB lithography, platinum palladium (PtPd) deposition, and lift off. Typically the fabricated nanowire width was 200 nm and the metal gate length was 250 nm.

Threshold logic circuit operation

The operation of the fabricated two-input threshold logic circuit was examined with the supply voltage, V_{DD}, of 0.3 V, the FET gate voltage for current-to-voltage conversion, $V_{Goffset}$, of 0.2 V, and the gate voltage for the load FET in the inverter, V_{GL}, of 0.3 V. The voltage swing of the input signals was 0.9 V and the frequency was 100 Hz. **Figures** 3**(a)** and 3**(b)** show the measured waveforms of the summed signals in the case of $V_{Goffset}$ = 0.20 V and 0.42 V, respectively. The outputs showed the three-level values reflecting the sum of the inputs. They were not exactly proportional to the inputs, because the FET for the current-to-voltage conversion pulled up the drain potential of the the FETs for the voltage-current conversion in the input stage. The output voltage was decreased approximately 30% by increasing $V_{Goffset}$. **Figure 3(c)** shows the voltage transfer curve of the inverter for the threshold function. The threshold voltage was around 0.2 V. The inverter output would give high when the input voltage less than 0.2 V. The differential gain was 0.75. This small gain was attributed to the relatively low V_{DD}.

Figure 4 shows the measured input and output waveforms of the threshold logic operation of the fabricated circuit. Obtained results successfully demonstrated the change of the logic functions by adjusting the voltage swing of the output of the sum through $V_{Goffset}$. When $V_{Goffset}$ = 0.20 V and the output of the sum was high, the system operated as NOR gate, where the circuit output was high only when the both inputs were low. On the other hand, when $V_{Goffset}$ = 0.42 V and the output of the sum was a little bit low, the system operated as NAND gate, where the circuit output was low only when both inputs were high. However the output voltage swing was much smaller than the input voltage swing. The nonlinearity of the summing operation and the low voltage gain of the inverter attributed to the insufficient output voltage swing. Adjusting the

input voltage swing and supply voltage of the inverter would increase the output voltage swing.

Double threshold function and noise-assisted switching of the inverter

Figure 5 shows an example of the measured transfer characteristic of the fabricated SiN-insulated-gate GaAs nanowire FET. It exhibited clear hysteresis curve with double threshold. The direction of the hysteresis curve was clockwise. The interval between the two threshold depended on the electron trap density in the SiN insulator, which was changed with the insulator formation process condition [20]. From the separate experiments, the state holding time for high and low drain current states, corresponding to the time constants of the discharging and charging the electron trap, were in a second order. The longer holding time of the low current state than that of the high state was observed, suggesting that the trap tended to hold the electron rather than empty.

We compared the two types of the inverters having a conventional Schottky gate FET and a SiN-gate FET. **Figure 6(a**) shows the measured transfer characteristic of the inverter in which the SiN-gate FET was used as a driver FET as shown in the left of the figure. The inverter exhibited the double threshold and the direction of the hysteresis was anticlockwise. This meant that an increased input signal shifted the threshold from low to high and the system response was inhibited by the input. On the other hand, the inverter having a SiN-gate FET as the load as shown in **Fig. 1(b)**, the transfer curve exhibited the clockwise hysteresis. This is similar to the Schmitt trigger inverter, which appears the stochastic resonance response having the SNR (signal-to-noise ratio) gain to the weak signal [9]. It is noted that the input was also given to the gate of the load FET in this inverter and the hysteresis of the SiN-gate FET reflected in the inverter transfer

characteristic. In this configuration, a large input signal increased the load resistance and shifted the threshold of the inverter from high to low. Then the system response was promoted by the increased input.

We examined the time-domain response to the small signal in the fabricated inverter in **Fig. 6(b)**. **Figure 7(a)** shows the input-output waveforms of the inverter for the signal with pre-pulsation to assist the state switching. The input voltage swing was 0.5 V, which was insufficient to switch the states of the SiN-gate FET whose thresholds were -1 V and +0.1 V. The width and the amplitude of the pre-pulsation was 0.2 s and ±1.5 V, respectively. When the input was low, the inverter gave the ideal high level. On the other hand, when the input was high, the output once dropped and then gradually increased to 0.5 V after pre-pulsation. This transient arose from the state holding time of the SiN-gate FET. The load FET gradually changed the state from OFF to ON after the positive pulsation for turn off this FET.

Then we used Gaussian noise for assisting the state transition, instead of the pre-pulse. The standard deviation of the noise amplitude, V_{rms}, was 0.3 V and the bandwidth was 15 MHz. The obtained input-output waveforms are shown in **Fig. 7(b)**. In this graph, the noise was imposed from 10 s. It should be noted that the data was averaged in the measurement system at each time point and the noise appeared small in this plot compared to the imposed one. Before imposing the noise, the output of the inverter could not sufficiently decrease to low level when the input was high. However, imposing the noise, the output clearly decreased to almost zero when the input was high. The logic swing could be almost the same to V_{DD} = 0.5 V. This result demonstrated that our inverter with configuration in **Fig. 1(b)** could respond to the small input by imposing noise, confirming the potential for operating the threshold logic circuit with

low voltage even under noisy condition. The mechanism of the such stable switching is the noise-assisted state transition. The imposed noise with an appropriate amplitude assisted the small signal for "high" to cross the high threshold, but did not assisted it to cross the low threshold. In the case of the input signal for "low", the similar situation took place. The frequent threshold crossing owing to the small noise autocorrelation time, approximately 0.07 μs in this experiment, made it possible to effectively keep the state after switching, even with the short state holding time of the SiN-gate FET around ms. Therefore an optimal noise intensity exists for switching, like the stochastic resonance.

Conclusions

For a low-power information processing system coexisting with noise, we investigated a threshold logic circuit and double threshold function on a GaAs-based nanowire field-effect transistor (FET) network. Both NOR and NAND logic gate operations were demonstrated in the fabricated circuit by adjusting the relative threshold value. Double threshold function was implemented on the GaAs nanowire by inserting silicon-nitride insulator containing electron traps in the gate of the FET. Two types of the inverter circuit having different hysteresis loop directions were fabricated and characterized. The inverter with clockwise hysteresis was found to respond to the small signal by imposing noise. The noise coexistence capability of the threshold logic circuit arose from the noise-assisted switching in the double threshold device.

Acknowledgements

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Figure 1. (a) Basic element and operation of the threshold logic and (b) circuit diagram of the two-variable threshold logic with double threshold function implemented using GaAs-based nanowire FETs with conventional Schottky gate and SiN insulated gate.

Figure 2. Scanning electron microscope image of the fabricated two-variable threshold logic circuit integrating GaAs-based nanowire FETs with its schematic.

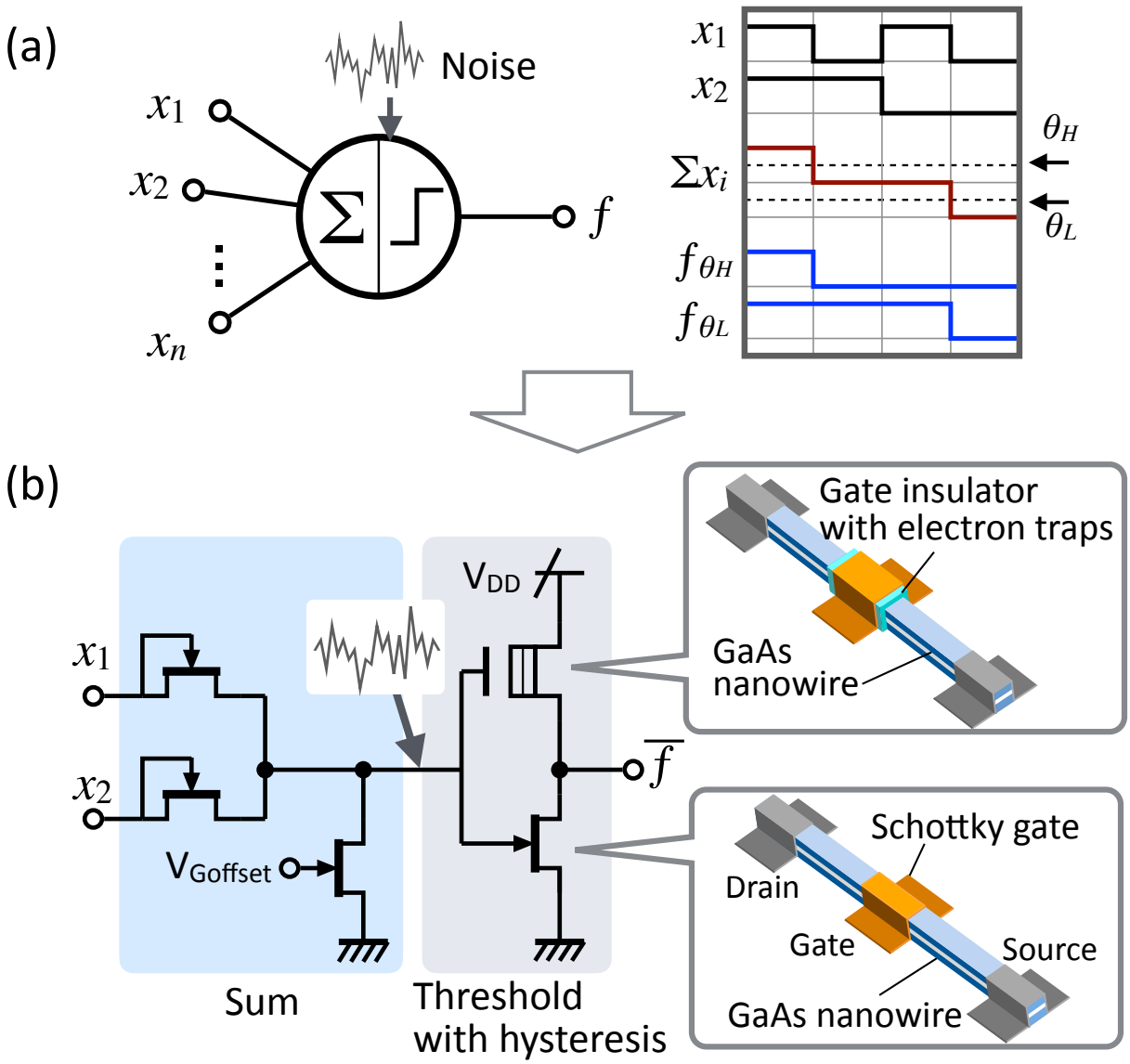
Figure 3. Waveforms of the inputs and the output of the sum for V_{Goffset} of (a) 0.20 V and (b) 0.42 V, and (c) voltage transfer characteristic of the inverter integrating the two Schottky-gate nanowire FETs.

Figure 4. Measured input and output waveforms of the fabricated threshold logic circuit for (a) NOR operation at V_{Goffset} = 0.20 V and (b) NAND operation at V_{Goffset} = 0.42 V.

Figure 5. Transfer characteristic of a fabricated SiN-gate FET with schematics of its charge states.

Figure 6. Measured transfer characteristics of the fabricated double threshold inverters having a SiN-gate nanowire FET (a) as the driver and (b) as the load.

Figure 7. Input and output waveforms of the double threshold inverter with an SiN-gate nanowire FET for the load: (a) imposing pre-pulses on the input for the charge state switching and (b) imposing Gaussian noise on the input.



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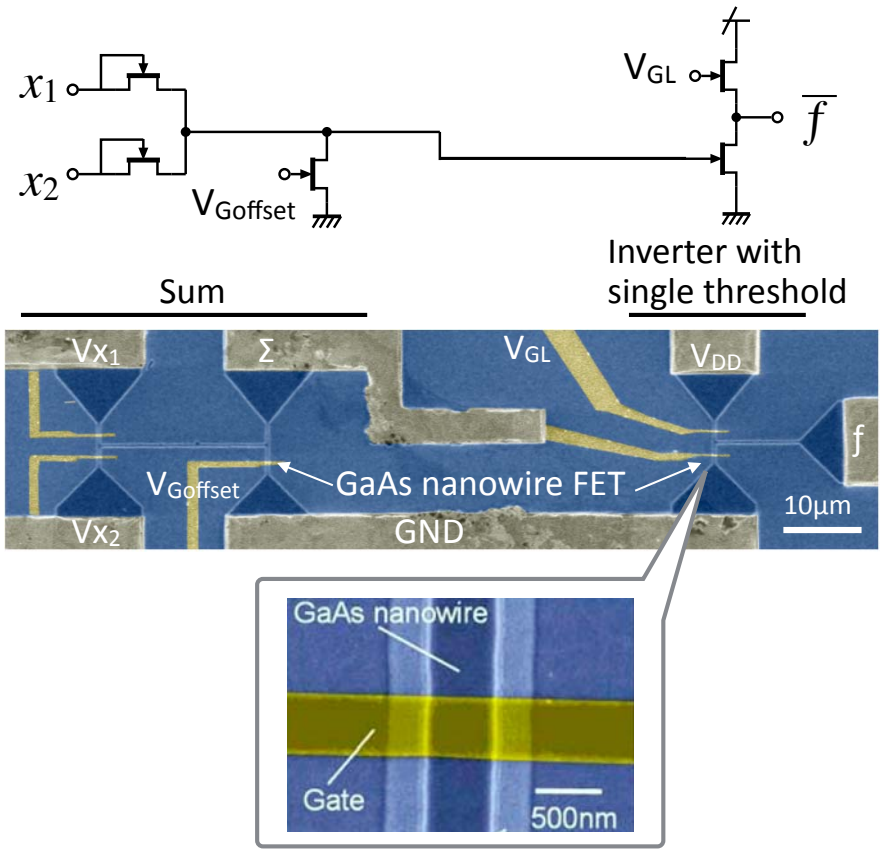

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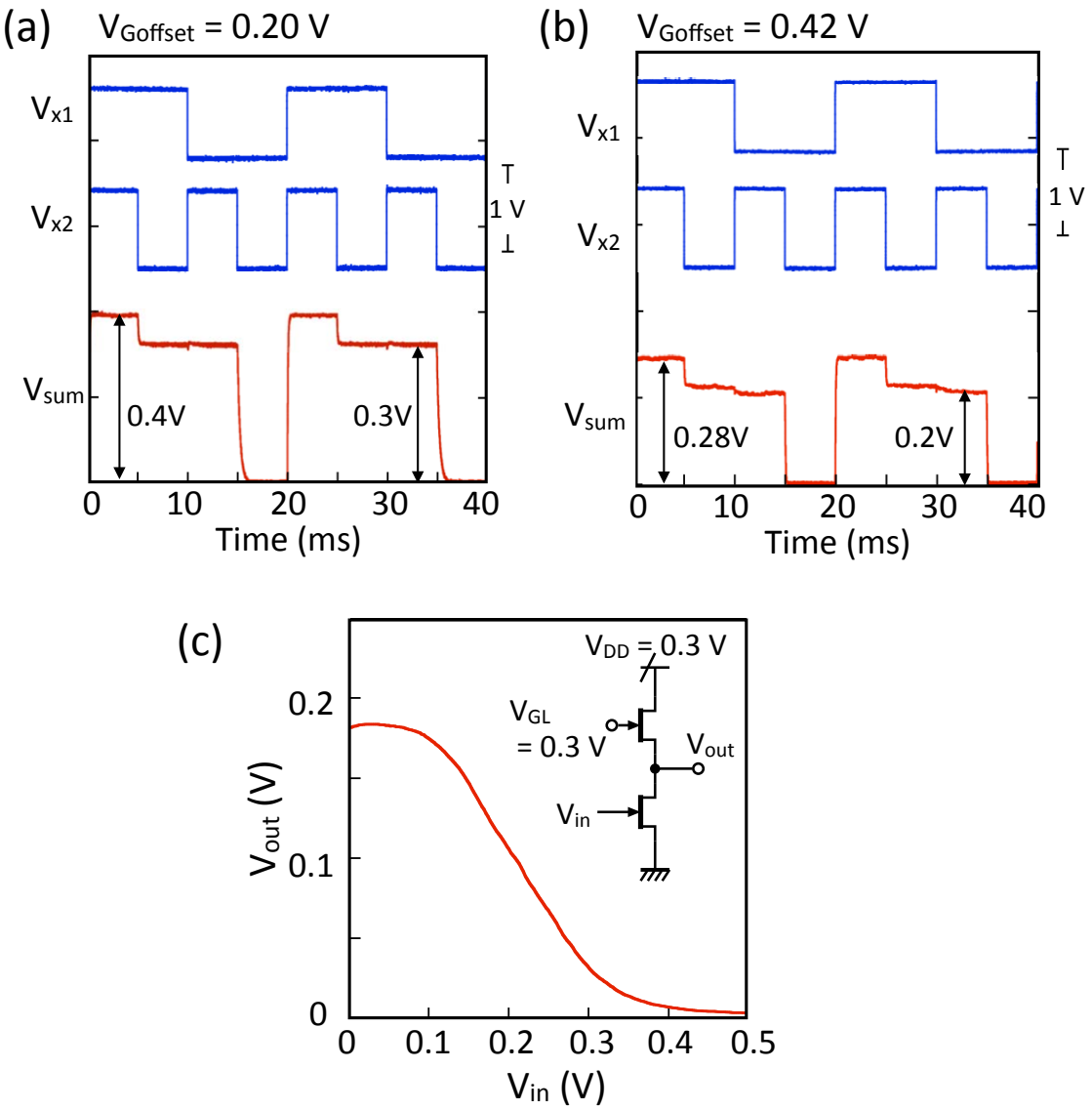

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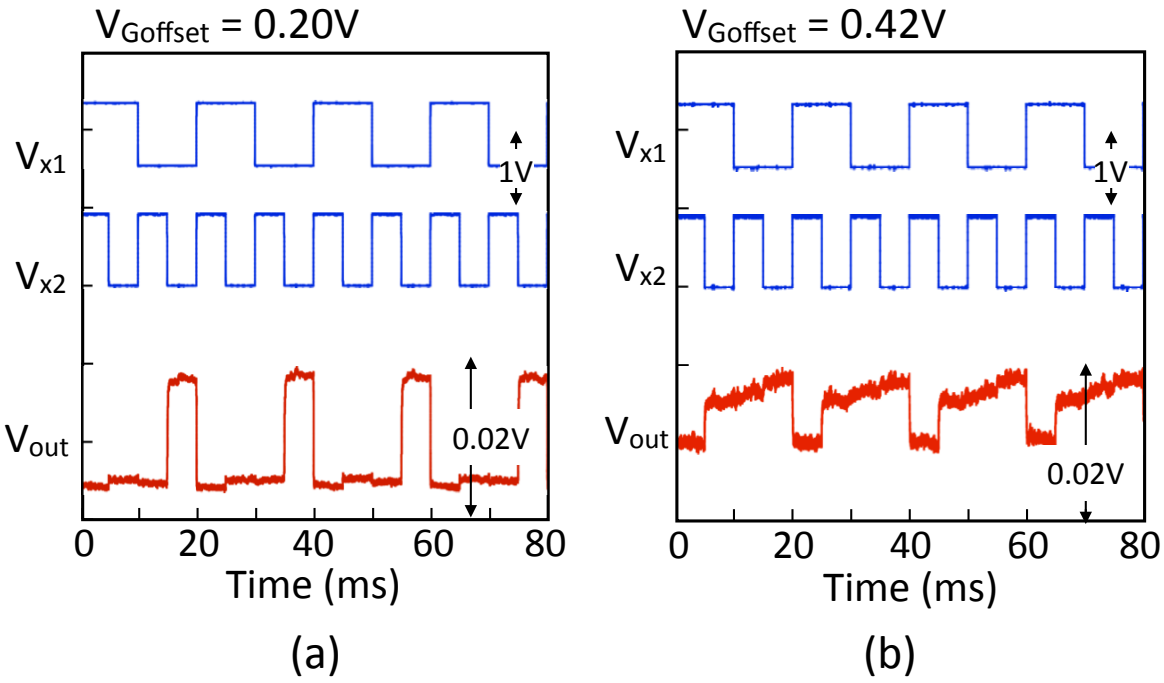

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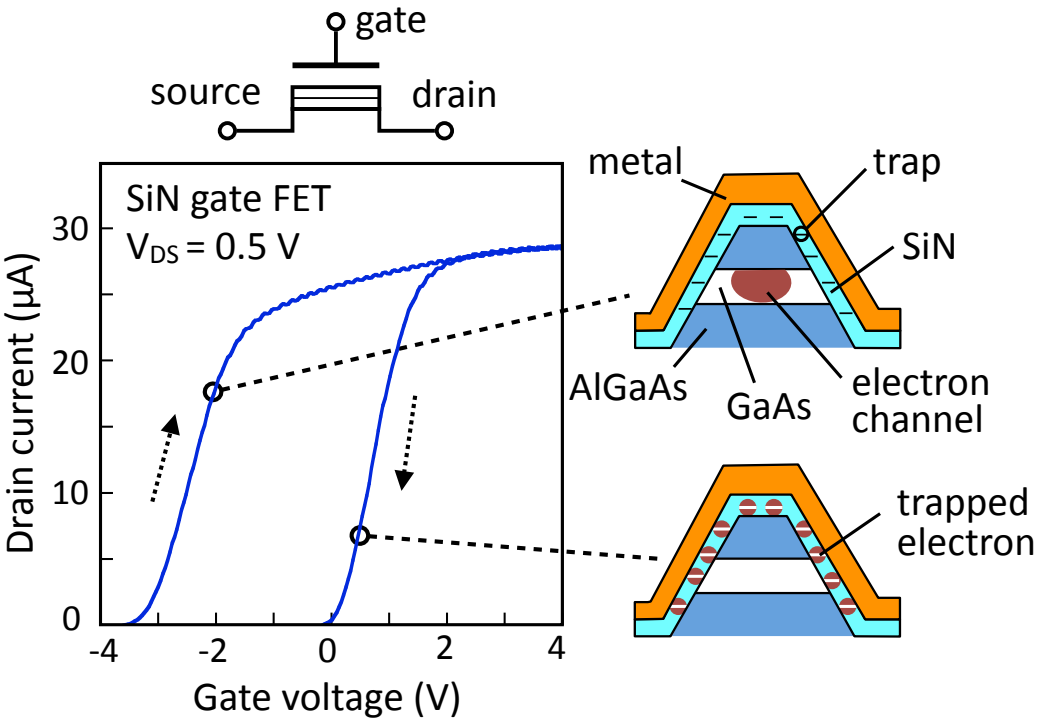

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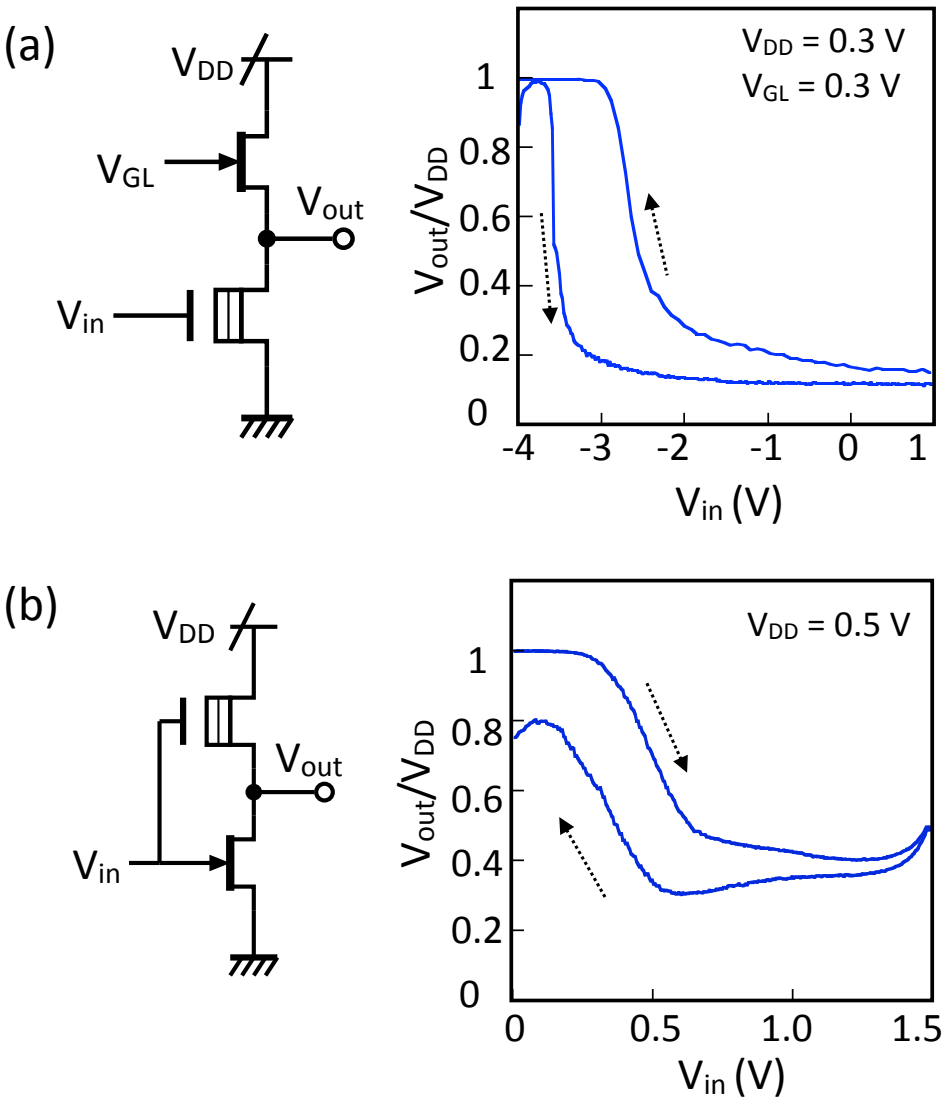

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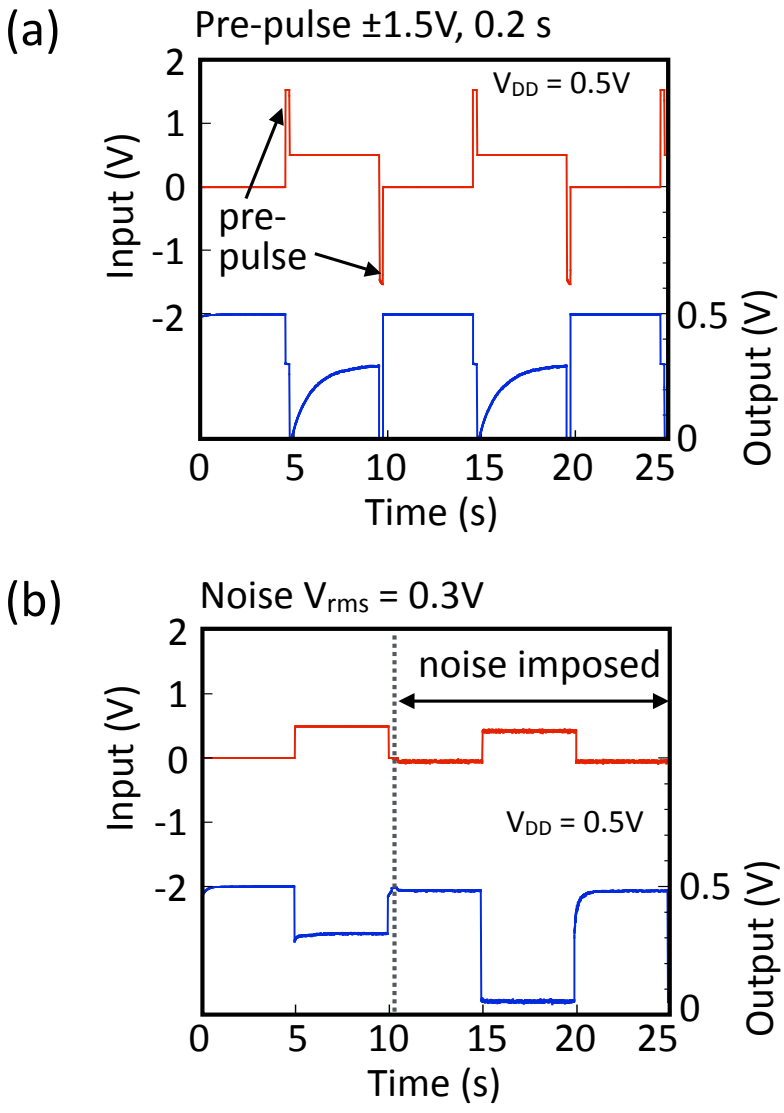

Figure 7 Kuroda et al.