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Reduction of interface state density at SiO_2/InAlN interface by inserting ultrathin Al_2O_3 and plasma oxide interlayers

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SiO_2/InAlN interfaces formed by plasma-enhanced chemical vapor deposition were investigated. X-ray photoelectron spectroscopy showed that the direct deposition of SiO_2 onto an InAlN surface led to the oxidation of the InAlN surface. The interface state density, D_{it}, was on the order of 10^{12} $cm^{-2}eV^{-1}$ (5×10^{12} $cm^{-2}eV^{-1}$ at 0.3 eV from the conduction band edge, E_c), which indicated the possibility of improving the interface properties. Reduction of the interface state density was attempted using an Al_2O_3 interlayer and a plasma oxide interlayer. The insertion of a 2-nm-thick Al_2O_3 interlayer to prevent surface oxidation by plasma reduced D_{it} slightly. A marked reduction in D_{it} to less than 10^{11} $cm^{-2}eV^{-1}$ deeper than 0.3 eV from E_c, however, was achieved by the intentional formation of a 1-nm-thick plasma oxide layer, formed by N_2O plasma oxidation, as an interlayer between SiO_2 and InAlN.

1. Introduction A lattice-matched InAlN/GaN interface provides a high-density two-dimensional electron gas (2DEG) generated by the high density of polarization-induced interface charges and the large conduction band offset [1]. Therefore InAlN is a promising material for achieving a high-power and high-frequency GaN high-electron-mobility transistor (HEMT) that can switch or control a large current flow. In the actual application of InAlN to HEMTs, the utilization of an insulator is important for suppressing the gate leakage current [2], especially for a very thin barrier layer, to obtain enhancement-mode HEMTs. It has also been reported that the electron mobility in an insulated-gate HEMT is higher than that in a Schottky barrier gate HEMT [2]. Actually, the high-power and high-frequency performances of metal-oxide-semiconductor (MOS) HEMTs have been reported [2-7]. So far, several insulators have been investigated for combination with InAlN, including Al_2O_3 [2, 8-11], ZrO_2 [9, 12, 13], $GdScO_3$ [9], HfO_2 [12], SiO_2 [14], plasma oxides [3-7], and thermal oxides [15, 16]. Among these insulators, SiO_2 has the largest band gap with a proven track record in Si-based electronics. However, a method for controlling the SiO_2/InAlN interface has not been investigated.

Among the several deposition methods developed for SiO_2, chemical vapor deposition (CVD) is the most widely used method to deposit a high-quality SiO_2 film. However, the topmost surface of the host semiconductor is usually oxidized in an uncontrolled manner during the deposition of SiO_2, which might lead to disorder of the interface, resulting in the generation of interface states. To reduce the interface state density, the disorder at the interface should be avoided. To clarify the effect of deposition on the interface, one of the CVD methods should be examined. Here we applied plasma-enhanced chemical vapor deposition (PECVD), which is one of the most frequently used methods for the deposition of SiO_2 films. Nevertheless, the present results for the interface chemical reaction and its control can also serve a useful reference for other CVD methods.

In this study, we investigated SiO_2/InAlN interfaces formed by PECVD and attempted to reduce the interface state density, D_{it}. X-ray photoelectron spectroscopy (XPS) indicated that the direct deposition of SiO_2 led to the oxidation of the InAlN surface. D_{it} on the order of 10^{12} $cm^{-2}eV^{-1}$ was measured for the SiO_2/InAlN interface. Then we attempted to control the interface to reduce D_{it}. Compared

with the direct deposition of SiO_2 onto an InAlN surface, the insertion of an ultrathin Al_2O_3 interlayer reduced D_{it} slightly. However, a marked reduction was achieved by using a plasma oxide interlayer.

2. Experimental An MOVPE-grown Si-doped (2×10^{18} cm^{-3}) thick (160 nm) $In_{0.17}Al_{0.83}N$/2-μm-thick GaN buffer layer on a sapphire substrate was used for MOS diodes. The structure of the fabricated MOS diodes is shown in Fig. 1. Since the InAlN layer is sufficiently thick and highly doped, the depletion layer width is smaller than the InAlN layer thickness. Therefore, this diode can be used as an ordinary MOS diode. The fabrication sequence is as follows. Before the deposition of an insulator, the surface oxide was removed by buffered hydrofluoric acid (BHF, $HF:NH_4F$=1:5). A SiN layer of 20 nm was deposited by electron cyclotron resonance chemical vapor deposition (ECRCVD) at 400 °C. An ohmic contact electrode of Ti (20 nm)/Al (50 nm)/Ni (20 nm)/Au (50 nm) was then formed by photolithography. Then the sample was annealed at 850 °C for 1 min in a nitrogen flow with the InAlN surface protected by the SiN layer, which was followed by SiN removal with BHF. A SiO_2 layer (20–30 nm) was deposited by PECVD at 300 °C with a plasma power of 40 W using N_2O and SiH_4. Finally, a Ni/Au electrode was formed. For the samples with interlayers, prior to the SiO_2 deposition, an Al_2O_3 interlayer (2 nm) was deposited by atomic layer deposition (ALD) using trimethylaluminum (TMA) and H_2O, while a plasma oxide interlayer (1 nm) was formed by N_2O plasma at 300 °C with a plasma power of 40 W. A sample without an interlayer was also fabricated for comparison.

The XPS investigation of the SiO_2/InAlN interface was carried out using a sample with an ultrathin SiO_2 layer deposited onto a 30-nm-thick InAlN layer grown by MOVPE on a sapphire substrate via a 2-μm-thick GaN buffer layer. A monochromated Al-kα X-ray source (1486.6 eV) was used. The charge-up error in the binding energy was corrected by setting the C 1s spectral peak to 285.0 eV. Unless otherwise noted, the photoelectron exit angle, θ, was fixed at 45°. If necessary, θ was varied by rotating the sample. The photoelectron escape depth changed accordingly as

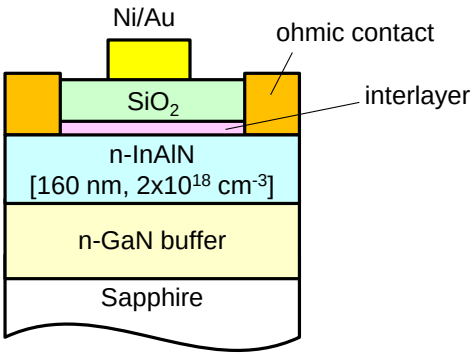


Figure 1 Structure of MOS diode.

$$\lambda = \lambda_0 \sin\theta\,, \tag{1}$$

where λ_0 is the inelastic mean free path calculated using the theory in Refs. 17 and 18. Since the material parameters for the N_2O plasma oxide were unknown, the escape depth for the plasma oxide layer was assumed to be the same as that for the Al_2O_3 layer as a first approximation.

Capacitance–voltage (C–V) measurement was carried out at a bias voltage sweep rate of 25 mV/s. Interface state density, D_{it}, distributions were derived from the 1 MHz C–V curves by using the high-frequency method described in Ref. 19. The insulator capacitance, C_I, was determined from the accumulation capacitance of the Si MOS diodes that were simultaneously fabricated with the same deposition sequence. The doping density was determined from the deep depletion region at the high negative bias region of the measured 1 MHz C–V curve.

3. Results and discussion To investigate the effect of SiO_2 deposition on interface chemical bonding, XPS analysis was carried out. Clear evidence of oxidation at the interface was observed in the O 1s spectra. The XPS O 1s spectra obtained from the BHF-treated InAlN surface and the ultrathin (2.6 nm) SiO_2/InAlN interface are shown in Fig. 2 (a). Here the spectrum for the SiO_2/InAlN interface was obtained at θ = 90°, for which the photoelectron escape depth was 2.9 nm. The energy position, shape, and intensity of the O 1s spectrum from the InAlN surface before deposition, immediately after the BHF treatment, coincided with those for the O 1s spectrum from the HF-treated gold surface, which indicated that the corresponding component can be attributed to absorbed water molecules [20]. On the other hand, as shown in Fig. 2 (b), compared with the spectrum from a thick SiO_2 layer, the O 1s spectrum from the ultrathin SiO_2/InAlN sample included an additional small shoulder peak on the lower-energy side. This shoulder peak can be

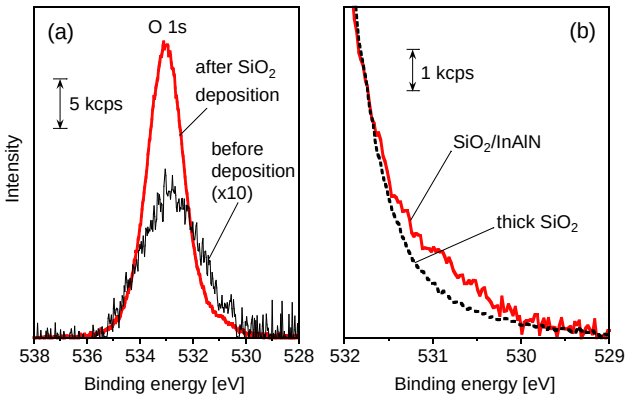
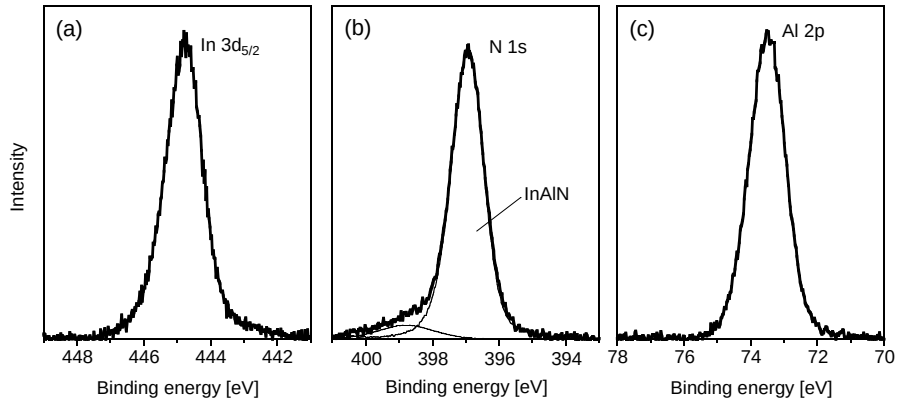


Figure 2 XPS O 1s spectra. (a) Comparison between the spectra of a BHF-treated InAlN surface and an ultrathin SiO_2/InAlN structure. (b) Comparison between the spectra from a thick SiO_2 layer and the ultrathin SiO_2/InAlN structure.

Figure 3 XPS spectra for ultrathin SiO_2 /InAlN structure. (a) In 3d, (b) N 1s, and (c) Al 2p spectra.



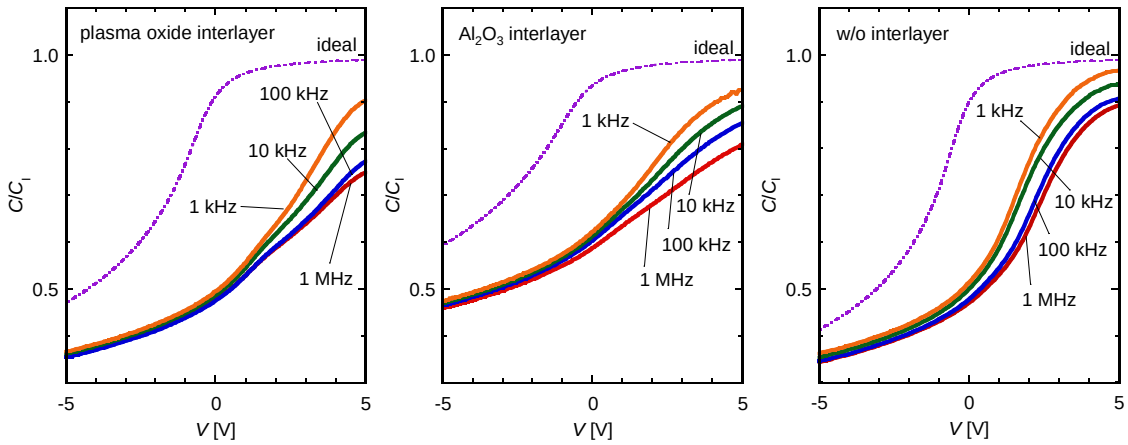


Figure 4 C-V curves for (a) SiO_2/InAlN sample, (b) sample with Al_2O_3 interlayer, and (c) sample with plasma oxide interlayer.

mainly attributed to Al-O bonding (531 eV), while no discernible Al-O bonding component was observed before the deposition of SiO_2. Thus, the surface of the InAlN was oxidized during the deposition. However, as shown in Fig. 3, no oxide components were detected in the Al 2p and In 3d core-level spectra from the SiO_2/InAlN interface, presumably due to the sub-monolayer thickness of the native oxide layer, resulting in signals that were too faint to be detected. Therefore, the native oxide layer that formed at the interface during the SiO_2 deposition was very thin (0.3 nm or less). In Fig. 3 (b), the higher-energy component in the N 1s spectrum is presumably due to absorbed NO_x molecules.

The C–V characteristics for the SiO_2 /InAlN MOS diode sample without an interlayer are shown in Fig. 4 (a). The hysteresis was negligible (not shown). Here the ideal curve is calculated assuming that the flat band voltage is obtained at zero bias. It is also assumed that the polarization charge is fully compensated. This is because the origin and generation mechanism of charge at the insulator/III-nitride interface are under debate [21-24]. In particular, the interface charge density may change with the interface bonding as discussed in Ref. 21. Therefore, we cannot determine the exact ideal value of the Al_2O_3/InAlN interface polarization charge density. Here the interface polarization charge is considered to be included in the interface fixed charge to shift the measured C–V curves horizontally relative to the ideal curve. Even though the SiO_2 layer was directly deposited onto the semiconductor surface by PECVD, the resultant C–V characteristic did not suffer from severe Fermi level pinning. Combined with the XPS results, this result indicates the robustness of the InAlN surface to the plasma deposition process. Nevertheless, the steepness of the C–V curve is low. The D_{it} distribution derived from the C–V curve is plotted in Fig. 5. A D_{it} of 5×10^{12} $cm^{-2}eV^{-1}$ at 0.3 eV from the conduction band edge,

E_C, was obtained for the directly deposited SiO_2/InAlN sample. (This energy point can be common metric for all samples.) It may be possible to improve the interface properties by controlling the oxidation at the interface. In particular, it should be clarified

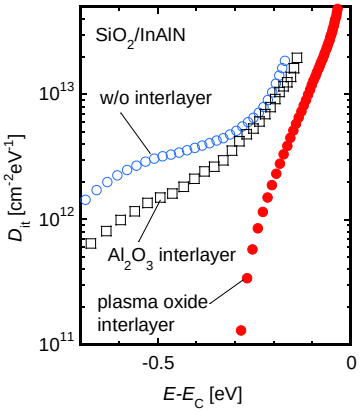
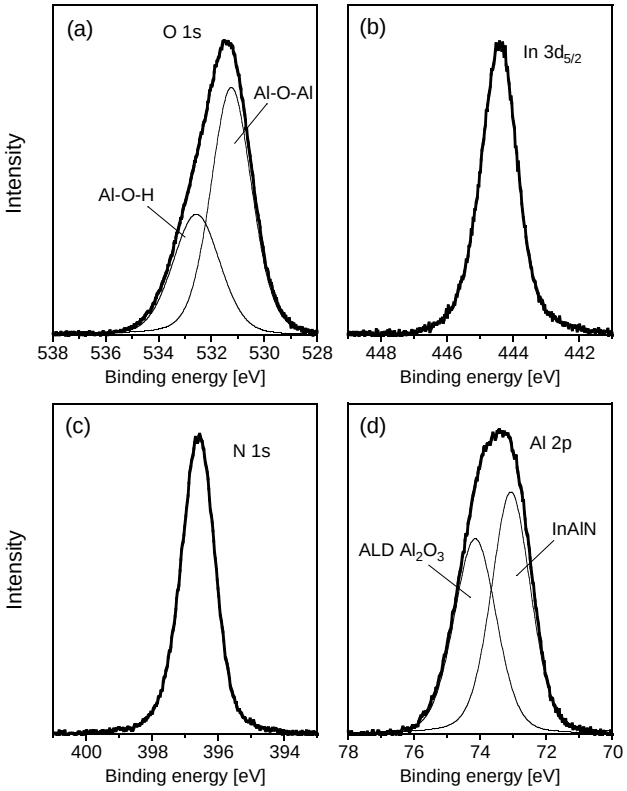


Figure 5 Summary of D_{it} distribution derived from C-V curves.

whether plasma oxidation has an adverse effect on the interface properties. We thus attempted to control the interface properties.

We attempted to improve the interface properties by inserting an ultrathin interlayer to minimize the plasma oxidation of the InAlN surface. An ultrathin ALD Al_2O_3 layer was chosen because an Al_2O_3/InAlN interface has been reported to show good properties [2, 8-11]. Figure 6 shows the XPS O 1s, In 3d, N 1s, and Al 2p core-level spectra obtained from the ultrathin Al_2O_3/InAlN interface. The thickness of the Al_2O_3 ultrathin layer was 2 nm. No clear sign of oxidation was observed in the In 3d and N 1s core-level spectra. The O 1s spectrum has two components, which can be attributed to Al-O-Al bonding and Al-O-H bonding [25, 26]. For Al 2p, since the chemical shift between the hydroxide and oxide components is too small to separate them [26], the oxide components merged to form one peak here. Considering the thickness of the oxidized layer discussed for Fig. 3, the oxidation of the InAlN surface is likely to have been minimized by the Al_2O_3 interlayer during SiO_2 deposition. The minimization of the InAlN surface oxidation should lead to a change in the interface properties. The C-V characteristic, shown in Fig. 4 (b) for the MOS diode with the ultrathin Al_2O_3 interlayer, was slightly improved. The hysteresis was negligible again (not shown). As shown in Fig. 5, a D_{it} value lower than that of the SiO_2/InAlN sample without the interlayer was obtained for the sample with the Al_2O_3 interlayer. The minimization of the InAlN surface oxidation led to a slight improvement of the interface properties.

A significant result was obtained by the formation of a native oxide interlayer by N_2O plasma oxidation. Figure 7 shows the XPS spectra obtained for the plasma-oxidized InAlN surface. The oxide components can be clearly observed in the Al 2p and In 3d spectra, while no oxide components can be seen in the N 1s spectrum. Therefore, by the present plasma oxidation, an oxide layer containing no nitrogen oxide was formed. The thickness was estimated to be about 1 nm from the decay of the spectral intensity. On



the other hand, the O 1s spectrum consisted of four components indi-

Figure 6 XPS spectra for ultrathin Al_2O_3 /InAlN structure. (a) O 1s, (b) In 3d, (c) N 1s, and (d) Al 2p spectra.

cated by A to D in Fig. 7 (a). Components A and B can be attributed to the In and Al oxides, while components C and D should be attributed to the In and Al hydroxides or their oxygen-deficient region [27-29]. The completed MOS diode, after the deposition of a thick SiO_2 layer, exhibited a C-V curve with a steep change in capacitance as indicated in Fig. 4 (c). A markedly reduced D_{it}, as shown in Fig. 5, was obtained with a value on the order of 10^{11} $cm^{-2}eV^{-1}$ near $E - E_c = -0.3$ eV. Empirically, the detection limit of D_{it} was found to be 1×10^{11} $cm^{-2}eV^{-1}$, and the derived D_{it} was lower than the detection limit deep inside the band gap ($E - E_c < -0.3$ eV). The C–V curves do not saturate at a negative bias because the band gap of InAlN is too large to allow the formation of an inversion layer. According to a simple calculation using Shockley–Read–Hall statistics, the time constant at 0.7 eV from E_c is about 1 s. Since the bias voltage sweep was sufficiently slow, *i.e.*, 25 mV/s, we can derive D_{it} in the range of 0.7 eV from E_c without any

effect of deep depletion when D_{it} is sufficiently high. Therefore, the observed rapid reduction of D_{it} around $E - E_c = -0.3$ eV is due to the low D_{it}. The large shift of the measured C–V curves from the ideal curve is due to the difference in the work function between metal and InAlN, and the interface/oxide fixed charge including the interface polarization charge, which is independent of D_{it}. Although the frequency dispersion is less

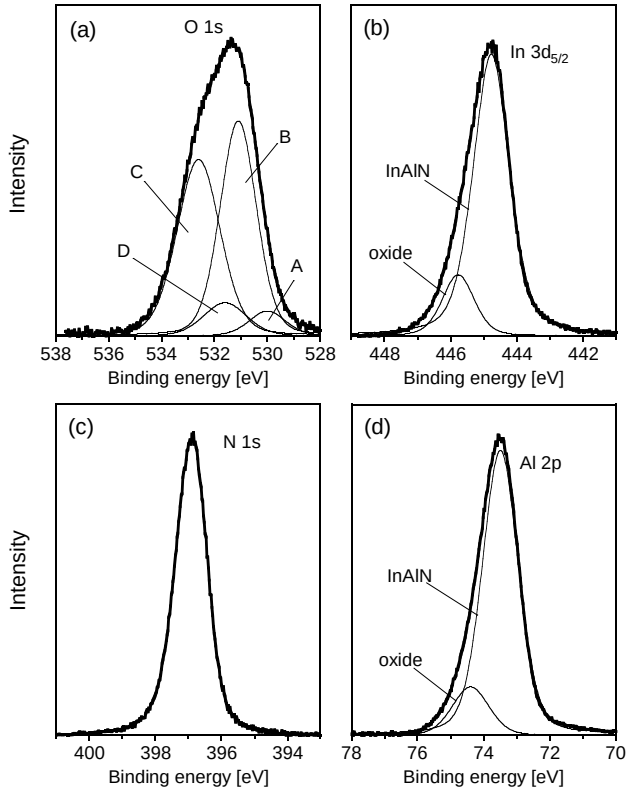


Figure 7 XPS spectra for ultrathin plasma oxide /InAlN structure. (a) O 1s, (b) In 3d, (c) N 1s, and (d) Al 2p spectra.

than that in other samples, the hysteresis was increased to ~1 V (not shown). However, the hysteresis for the plasma oxide interlayer sample was counterclockwise, which most likely resulted from the mobile ions and not from the interface state charge [30, 31]. Although the origin of the mobile ions is not clear, they might have originated from the intermingling of extrinsic contamination during the surface chemical treatment prior to the interface formation. The residual frequency dispersion may have possibly resulted from the lateral nonuniform distribution of the interface states, which is still high near the conduction band ($E - E_c > -0.2$ eV). More specifically, there is a possibility that pinning spots distributed randomly where the Fermi level was pinned locally in a small (nm-size) spot [32]. Nevertheless, the average characteristics can be derived from the high-frequency C–V curve. Therefore, neither the hysteresis nor the frequency dispersion is a rebuttal of the low D_{it} deep inside the band gap. Thus, the obtained result indicates that the plasma oxide/InAlN interface is a promising interface, although the plasma oxide formation process should be optimized further.

It should be stressed that the unintentional surface oxidation by plasma led to the highest D_{it} among our three samples. Presumably this was because the oxidized layer was too thin to form an ordered insulator–semiconductor interface. Therefore, the protection of the InAlN surface during the SiO_2 deposition using an ALD Al_2O_3 interlayer led to a reduction of D_{it}. The substrate temperature during ALD for Al_2O_3 was 300 °C. Although postdeposition annealing was not carried out, samples were heated at 300 °C for about 10 min in a gas mixture of N_2O and SiH_4 before the PECVD. The optimization of postdeposition annealing may improve the interface properties. Recently, it has been reported for Al_2O_3/GaN interfaces, formed by the same ALD technique, that bias annealing in air at 300 °C for several hours reduced D_{it} markedly [33]. Therefore, the Al_2O_3/InAlN interface may be improved by the same bias annealing method, although this is beyond the scope of this work. On the other hand, the intentional plasma oxidation resulted in the formation of an oxide layer with a sufficient thickness, which led to a further reduction of D_{it}. It is highly likely that the disorder of the interface was reduced by forming a sufficiently thick native oxide layer. Actually, using the native oxide layer as an interlayer is also an efficient means of forming excellent insulator–semiconductor interfaces for other semiconductors [34-36]. To achieve a low D_{it}, however, a low-damage process is conventionally used, *i.e.*, an electrochemical process [34, 35]. The recently reported plasma oxidation of a GaAs surface to form a good insulator–semiconductor interface [36] is a noteworthy means of increasing the flexibility of the interface formation process. For InAlN, the reduction in the DC-RF dispersion in an InAlN barrier GaN HEMT has been achieved by using an ultrathin (2 nm) plasma oxide layer in the access region without using a thicker dielectric film [37]. This result indicates the reduction of the surface states by plasma oxidation. Also, despite the formation of a native oxide layer by a plasma process in this study, D_{it} was reduced. On the basis of the previous reports on the successful operation of high-frequency HEMTs using a plasma oxide gate insulator [3-7], the present results indicate the usefulness of the plasma oxidation process.

4. Summary SiO_2/InAlN interfaces formed by PECVD were investigated. Compared with the direct deposition of SiO_2 onto an InAlN surface, the insertion of an Al_2O_3 interlayer reduced D_{it} slightly. The suppression of uncontrolled surface oxidation led to a slight reduction of D_{it}. However, a greater reduction was achieved by using a plasma oxide interlayer, which resulted in D_{it} of lower than 10^{11} $cm^{-2}eV^{-1}$ deeper than 0.3 eV from E_c. It is highly likely that the disorder of the interface was reduced by forming a sufficiently thick native oxide layer.

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