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Author(s)	Sato, Taketomo; Toguchi, Masachika; Komatsu, Yuto; Uemura, Keisuke
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Low-damage Etching for AlGaIn/GaN HEMTs Using Photo-electrochemical Reactions

Taketomo Sato, Masachika Toguchi, Yuto Komatsu, and Keisuke Uemura

Abstract—This paper describes our recent efforts to optimize photo-electrochemical (PEC) etching for fabricating recessed-gate aluminum gallium nitride/gallium nitride (AlGaIn/GaN) high-electron-mobility transistors (HEMTs). Selecting the proper light wavelength and voltage conditions enabled PEC etching on AlGaIn/GaN heterostructures to produce smooth and flat surfaces. Self-termination phenomena observed under optimal PEC condition were useful for precisely controlling the etching depth in the AlGaIn layer. Two types of HEMTs, i.e., Schottky-gate and metal-insulator-semiconductor (MIS)-gate, were fabricated. A recessed-gate AlGaIn/GaN structure fabricated with PEC etching showed positive threshold voltage, and its variation was very small with a standard deviation of only 0.019 V for the Schottky-gate HEMTs and 0.032 V for the MIS-gate HEMTs. A recessed-gate structure with PEC etching showed better current transport controllability with a small subthreshold-slope than that of planar-gate and dry-etched-gate AlGaIn/GaN structures.

Index Terms—AlGaIn/GaN heterostructures, HEMTs, low damage etching, photo-electrochemical reactions.

I. INTRODUCTION

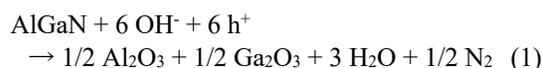
GALLIUM nitride (GaN)-based electron devices are promising for high-power and high-frequency application due to their superior electrical properties over silicon (Si) such as high-breakdown electric field and high saturation electron velocity. Aluminum gallium nitride (AlGaIn)/GaN high-electron-mobility transistors (HEMTs) have simultaneously achieved high blocking voltage and low on-state resistance in their device operation by using two-dimensional electron gasses (2DEGs) yielded at the AlGaIn/GaN heterointerface. Such HEMTs are basically normally-on devices having a negative threshold voltage (V_{th}). However, from the fail-safe viewpoint of power-switching devices, it is necessary to attain normally-off operation. One promising approach to achieve normally-off operation is adopting a recessed-gate structure [1,2], which can be

fabricated by thinning the AlGaIn layer beneath the gate electrode. The dry etching process is commonly used for thinning AlGaIn layers, in which the etching is carried out by applying plasma of an appropriate gas mixture containing a chemically reactive element. However, dry-etched surfaces tend to be negatively affected by various types of damage due to the bombardment of reactive ions and radicals [3,4]. These types of damage and defects induce high-density surface and interface states in the forbidden band, which leads to severe operational-stability problems such as gate leakage, current collapse, and V_{th} instability.

One alternative approach to the dry-etching process is the low-energy photo-electrochemical (PEC) etching process. After early studies by Minsky [5] and Youtsey [6], various PEC etching processes have been reported for GaN [7-9] and AlGaIn [10] with growing interest in damage-less etching. Our PEC etching [11-14], which is carried out using the pulsed bias, is a cyclic process consisting of anodic oxidation and subsequent dissolution of the resulting oxide in an electrolyte. We reported that the dry-etching damage was effectively removed from n-GaN surfaces with the PEC process without causing any additional damage [11]. By tuning the PEC conditions, such as anodic voltage and illumination, we were able to precisely control the V_{th} and improve the current transport controllability in recessed-gate AlGaIn/GaN HEMTs [14]. In this study, we evaluated the electrical properties of Schottky-gate and metal-insulator-semiconductor (MIS)-gate HEMTs fabricated simultaneously on the same chip using the PEC process. We discuss the on-chip uniformity of the V_{th} in this paper.

II. BASIC PRINCIPLE OF PEC ETCHING

Typically, wet-chemical etching of III-V compounds involves using an oxidant to oxidize the surface, followed by dissolution of its oxide into a pH-controlled solution. For example, the mixture of hydrogen peroxide (H_2O_2) and an acid solution, such as sulfuric acid (H_2SO_4) or hydrochloric acid (HCl), are commonly used as the etching solution for gallium arsenide (GaAs) and indium phosphide (InP). In the case of PEC etching, the surface is etched by repeating the anodic oxidation and its dissolution into the electrolyte, as schematically shown in Fig 1(a). By applying the anodic bias in the electrolyte, the AlGaIn surface is oxidized as



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The authors are with Research Center for Integrated Quantum Electronics (RCIQE), Hokkaido University, Sapporo, 060-0813 Japan (e-mail: taketomo@rciqe.hokudai.ac.jp).

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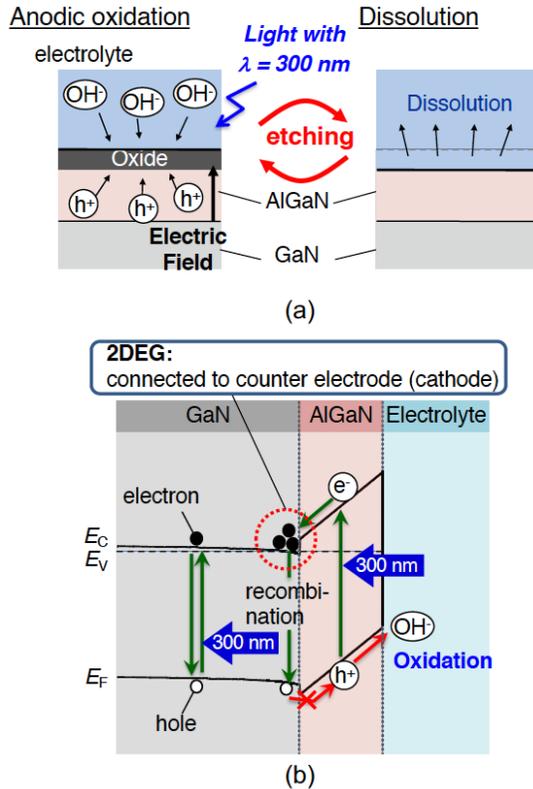


Fig. 1. Schematics of (a) the PEC etching principle and (b) the potential distribution of electrolyte/AlGaIn/GaN structure.

The aluminum oxide (Al₂O₃) and gallium oxide (Ga₂O₃) are immediately dissolved into the alkali or acid solution. PEC etching is attractive for nitride semiconductors since standard chemical etching is not applicable due to its high thermal- and chemical stability.

To precisely control the etching depth, the pulsed-light mode or/and pulsed-bias mode has been frequently applied for the PEC etching process. The pulsed mode is also very effective for producing a smooth surface morphology since the density of holes is kept constant at the interface between the electrolyte and GaN via the hole-relaxation during the pulsed-off interval [7,9].

Figure 1(b) schematically shows the potential distribution of the electrolyte/AlGaIn/GaN structure. As is the nature of the AlGaIn/GaN heterointerface, a high electric field is induced in the AlGaIn layer, resulting in the generation of a high-density 2DEG. At a light wavelength (λ) of 300 nm, which is absorbed in both AlGaIn and GaN layers, photo-electrons and holes are transferred by the internal electric field to the 2DEG and electrolyte/AlGaIn interface, respectively. Accordingly, oxidation current flows even at a relatively low bias. Photo-carriers generated in the GaN layer cannot flow due to the existence of the 2DEG and the potential barrier at the AlGaIn/GaN interface. At $\lambda = 360$ nm (not shown here), which penetrates the AlGaIn layer and is absorbed in the GaN layer, oxidation current is observed under the larger anodic bias. This is because the amount of electrons concentrated in the 2DEG decreases with the increased reverse bias applied to the AlGaIn/GaN heterostructure. In such a situation, photo holes can flow toward the electrolyte/AlGaIn interface and cause

oxidation reactions. Thus, we can regulate the supply of photo holes by selecting the appropriate λ and anodic bias.

III. EXPERIMENTAL

For the PEC etching of AlGaIn/GaN heterostructures, we used a standard electrochemical cell, which consisted of the sample to be etched as the working electrode (WE), a platinum counter electrode (CE), and silver/silver chloride reference electrode (RE), as shown in Fig. 2(a). To remove the anodic oxide formed on the sample surface, we used a mixture of 1 mol/L H₂SO₄ and 1 mol/L H₃PO₄ as the electrolyte. As previously mentioned, the anodic bias and λ are important to regulate the amount of photo holes. We irradiated monochromatic light passing through band-path filters from the top of the sample using a xenon lamp as the light source. The power intensity of the light (P_{IN}) was adjusted using a Newport power meter (Model 843-R). The potential of the WE with respect to the RE was precisely controlled using a potentiostat with a Princeton Applied Research Versa STAT 4. We applied the etching bias (V_{EC}) in the pulsed mode to obtain a smooth and flat surface after PEC etching. The timing of etching stop was determined by monitoring the transient of the etching current density (J_{EC}).

An i-Al_{0.25}Ga_{0.75}N/i-GaN heterostructure grown on a Si or SiC substrate was used as the starting wafer, as shown in Fig. 2(b). The initial thickness of the AlGaIn barrier layer was 25 nm. A Ti/Al/Ti/Au (20/50/20/50 nm) multilayer ohmic electrode was formed using the electron-beam evaporation method followed by annealing at 800°C for 1 min in N₂ ambient. Then,

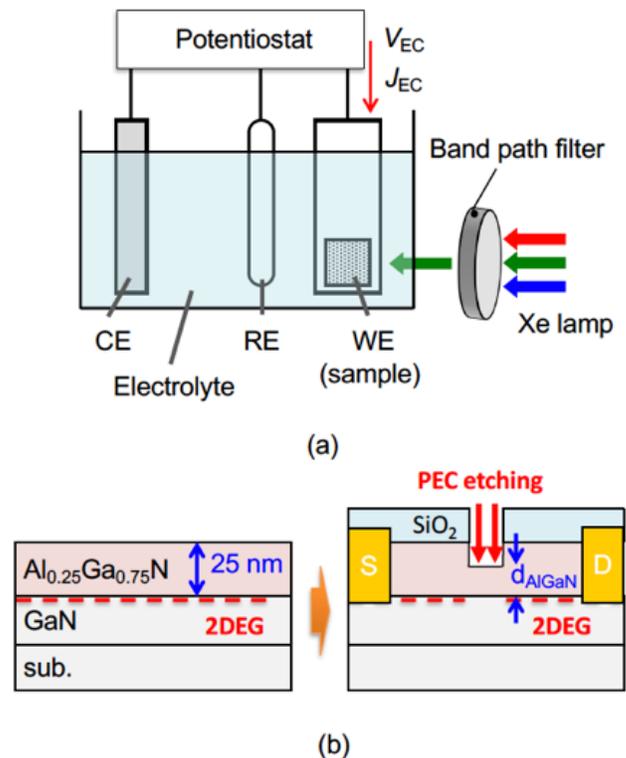


Fig. 2. Schematics of (a) the experimental setup for the PEC etching and (b) the sample structure.

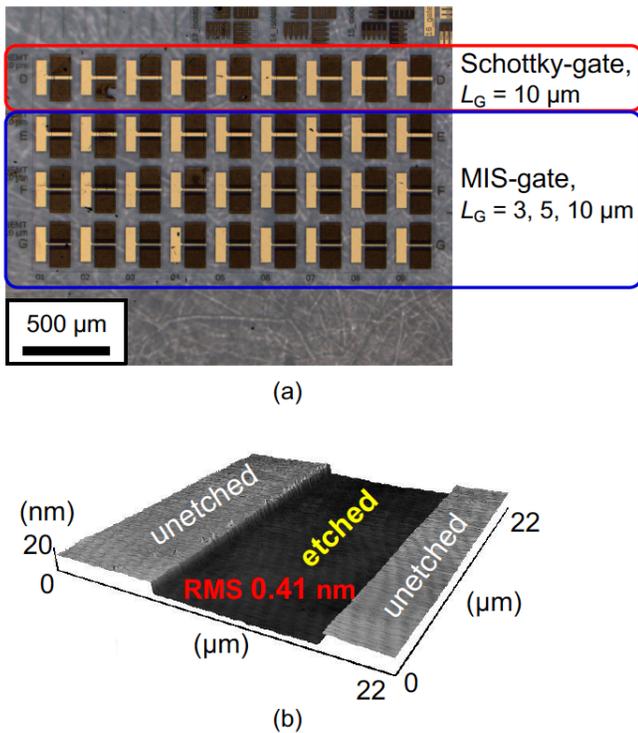


Fig. 3. Top view of device layout of AlGaIn/GaN HEMTs and (b) AFM image of the recessed-gate region prepared by PEC etching with $\lambda = 300$ nm.

a SiO₂ film (100 nm) was formed by sputtering and lithography to define the etching region. The sample to be etched was set on a Teflon holder and the ohmic electrodes were connected to the outer circuit via the embedded wires. The oxidation currents were supplied via the 2DEG channel, in which the open region was selectively reacted with the electrolyte. The key point is how we can control the thickness of the AlGaIn layer (d_{AlGaIn}) beneath the gate electrode. Before device fabrication, we investigated the basic properties of PEC etching by changing the V_{EC} and λ in terms of the photo-carrier regulation. After optimizing the PEC condition, we fabricated Schottky-gate and MIS-gate HEMTs to evaluate the effect of PEC etching on the electrical properties of the AlGaIn/GaN heterostructures. For the MIS-gate HEMTs, we deposited an Al₂O₃ film with a nominal 30-nm thickness onto the AlGaIn surface using an atomic layer deposition (ALD) system (SUGA-SAL1500) at 300°C. We then conducted post deposition annealing (PDA) at 400°C in N₂ ambient to improve the Al₂O₃ film quality and/or the Al₂O₃/AlGaIn interface.

IV. BASIC PEC-ETCHING PROPERTIES ON ALGAIN/GAN HETERO-STRUCTURES

The device-layout prepared on AlGaIn/GaN heterostructure samples is shown in Fig. 3(a), where 9 Schottky-gate HEMTs and 27 MIS-gate HEMTs having different gate lengths (L_G) of 3, 5, and 10 μm were implemented on one chip. To optimize the PEC condition, we first carried out PEC etching on the AlGaIn/GaN samples by comparing two types of illumination with different λ , i.e., $\lambda = 360$ nm, the photon energy ($h\nu$) of which corresponds to the bandgap energy (E_g) of GaN (3.4 eV)

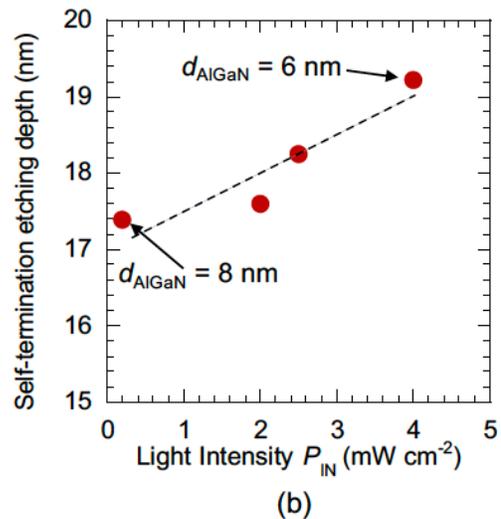
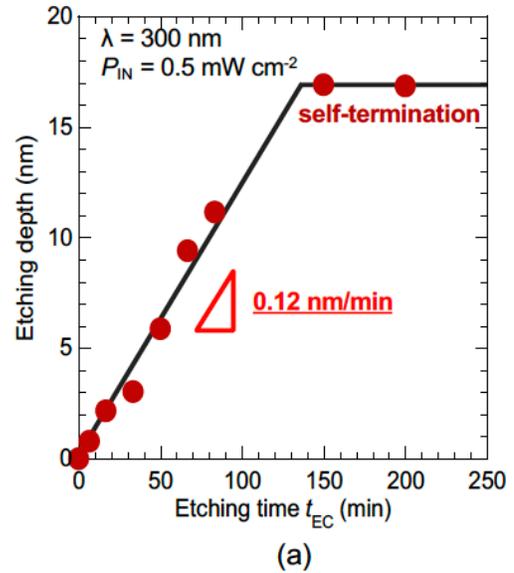


Fig. 4. Relationship between etching depth and etching time and (b) relationship between self-termination depth and P_{IN} .

used as a channel layer, and $\lambda = 300$ nm, the $h\nu$ of which corresponds to the E_g of AlGaIn (4.1 eV) used as a top barrier layer. After PEC etching at $\lambda = 360$ nm, small pores of about 100 nm in diameter were observed, where the pore-etching depth of about 250 nm penetrated through the top AlGaIn layer.

However, we were able to clearly observe the etched step between the masked and un-masked regions after PEC etching at $\lambda = 300$ nm. Figure 3(b) shows a typical atomic force microscopy (AFM) image of a sample after PEC etching at $\lambda = 300$ nm, $P_{\text{IN}} = 1.0$ mW/cm², and $V_{\text{EC}} = -0.2$ V. An overall flat surface was obtained in the etched region, in which the root mean square roughness was only 0.41 nm. The PEC etching rate to the AlGaIn layer increased with an increase in the photocurrents under higher V_{EC} . However, the pore-etching was observed for V_{EC} over 0.5 V, similar to PEC etching at $\lambda = 360$ nm. Such inhomogeneous etching was caused because the large amount of holes supplied not only from the AlGaIn layer but also from the GaN layer due to the high-electric field induced at the AlGaIn/GaN interface. We found that the V_{EC} in the range of

-0.5–0.5 V was the optimal bias condition to obtain a smooth etched surface. These results indicate that the use of the photo holes generated in the AlGa_N layer is important in the recess etching of AlGa_N/Ga_N heterostructures.

To clarify the effect of P_{IN} on the etching of the AlGa_N/Ga_N samples, we conducted basic PEC measurements [14]. The photocurrent transients were obtained during PEC etching at $\lambda = 300$ nm at which the data were compared by changing the P_{IN} . The photocurrents first increased to certain values with time then decreased for all samples. It should also be noted that the photocurrents increased as the P_{IN} increased. This result indicates that the etching rate of the top AlGa_N layer increased with the P_{IN} according to Faraday's law.

The etching rate is the most important parameter to fabricate recessed-gate AlGa_N/Ga_N HEMTs since the V_{th} is determined by the etching depth of the top AlGa_N layer. Figure 4(a) shows the relationship between etching depth and time obtained on the sample etched at $\lambda = 300$ nm and $P_{IN} = 0.5$ mW/cm². Etching depth increased linearly with etching time at the initial stage. However, the etching did not proceed more than a specific depth below the initial 25 nm AlGa_N-layer thickness. Figure 4(b) shows the relationship between self-termination depth and P_{IN} . We found that the self-termination depth increased with P_{IN} , indicating this phenomenon is related to the amount of photo holes generated in the AlGa_N layer. As previously mentioned, photo holes generated in the AlGa_N layer are transferred to the electrolyte/AlGa_N interface by an internal electric field. They cause oxidation reactions of AlGa_N, and the resulting oxides dissolve in the electrolyte. Since photo holes generated in the AlGa_N layer decrease due to the thinning of the layer, etching reactions are suppressed at a specific AlGa_N-layer thickness, which cannot generate sufficient photo holes for surface oxidation. The self-termination behavior is consistent with the results on photocurrent transients in which the current value strongly depended on the P_{IN} and eventually decreased to 0 as the processing time increased. The AlGa_N layer thinning also leads to the depletion of the 2DEG channel, which means automatic interruption of the electrochemical currents; thus, self-termination occurred. Self-termination may help in suppressing unintentional variations in recess depth.

V. ELECTRICAL PROPERTIES OF RECESSED-GATE ALGaN/GaN HEMTs PREPARED WITH PEC ETCHING

On the basis of the knowledge described in the previous section, we fabricated AlGa_N/Ga_N HEMTs having a recessed-gate structure by using the optimal PEC condition as previously reported [14] and evaluated the electrical properties of 29 HEMTs formed on the same chip. Figures 5(a) and (b) show the typical drain current-voltage (I_D - V_D) characteristics of planar-gate and recessed-gate AlGa_N/Ga_N Schottky HEMTs with a L_G of 10 μ m, respectively. Both samples showed good I - V curves with constant saturation currents and pinch-off behavior. As shown in Fig. 5(a), the I_D became almost 0 at a V_G of -3.0 V. However, the V_{th} of the recessed-gate-type HEMTs with $d_{AlGaN} = 8.0$ nm was roughly estimated to be about 0.2 V, which shifted to the positive direction, as shown in Fig. 5(b). These results clearly indicate that normally-off operation was achieved by thinning the top AlGa_N layer with the PEC etching.

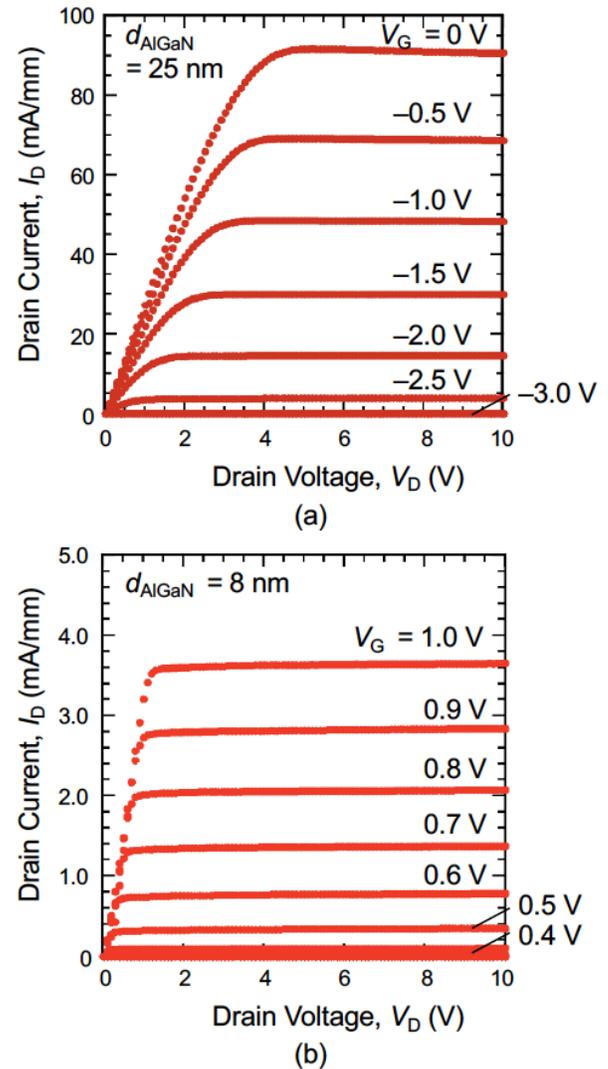
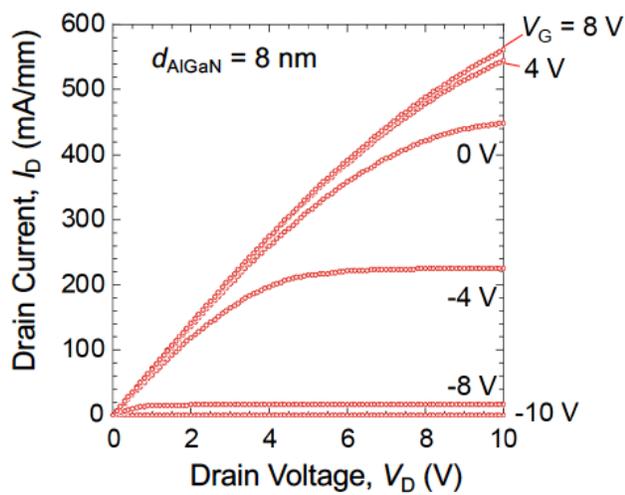


Fig. 5. I_D - V_D characteristics of Schottky-gate AlGa_N/Ga_N HEMTs for (a) planar-gate device and (b) recessed-gate device with $d_{AlGaN} = 8$ nm.

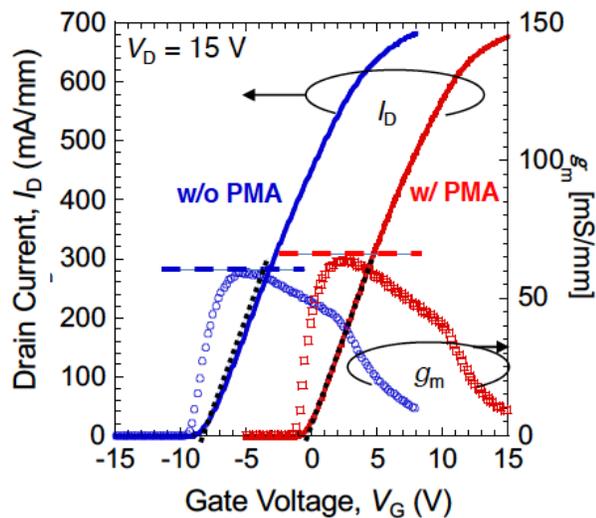
Figure 6(a) shows the I_D - V_D characteristics of the recessed-gate AlGaIn/GaN MIS-HEMTs with a L_G of 5 μm and nominal Al_2O_3 thickness of 30 nm. Similar to the case of the Schottky-gate HEMTs, the MIS-gate HEMTs showed good I - V curves with constant saturation currents and pinch-off behavior. The recessed gate structure having d_{AlGaIn} of 8 nm, which was the same as that of the Schottky-gate HEMTs, was formed by PEC etching. However, the V_{th} of the MIS-gate HEMTs was about -10 V, which was much lower than the expected value obtained with the Schottky-gate HEMTs, as seen in Fig. 5(b). Several groups have reported that the gate controllability of AlGaIn/GaN MIS-gate HEMTs enhances by reducing the interface-state density after some post-annealing processes after oxide layer deposition [15–18]. To improve the electrical properties of MIS-gate HEMTs, we carried out the post metallization annealing (PMA) process [19]. Figure 6(b) compares the transfer characteristics of the recessed-gate AlGaIn/GaN MIS-gate HEMTs for two types of devices

conducted with and without the PMA process. The PMA successfully made the V_{th} shift in the forward bias regime and enhanced the maximum transconductance value (g_m) from 60 to 66 mS/mm. A possible mechanism for the positive V_{th} shift and g_m enhancement after PMA may originate from the decrease in oxygen-related defects in the $\text{Al}_2\text{O}_3/\text{AlGaIn}$ system and subsequent shrinkage of the ALD- Al_2O_3 film caused by the relaxation of dangling bonds [19,20].

The self-termination of PEC etching described in the previous section is attractive to control the V_{th} and its uniformity of recessed-gate-type HEMTs. Figure 7(a) shows the log I_D - V_G characteristics of such HEMTs formed on one chip using the PEC etching process. The d_{AlGaIn} and L_G of the HEMTs were designed to be 8 nm and 10 μm , respectively. The I_D - V_G curves well overlapped both for the Schottky-gate and MIS-gate HEMTs, showing good uniformity of device performance. Furthermore, the MIS-gate HEMTs effectively reduced the leakage current and enabled high-current drive with a large gate

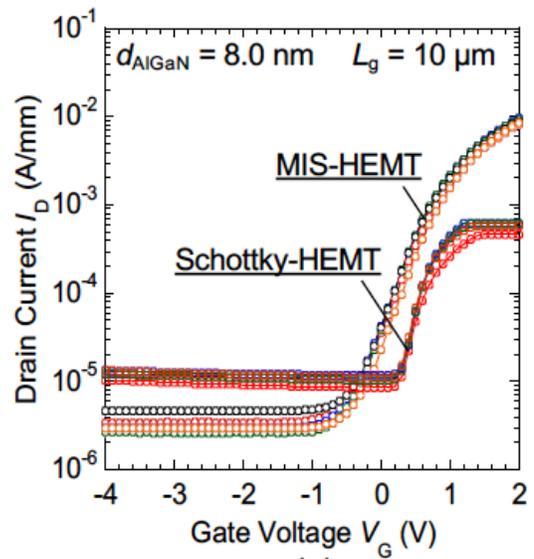


(a)

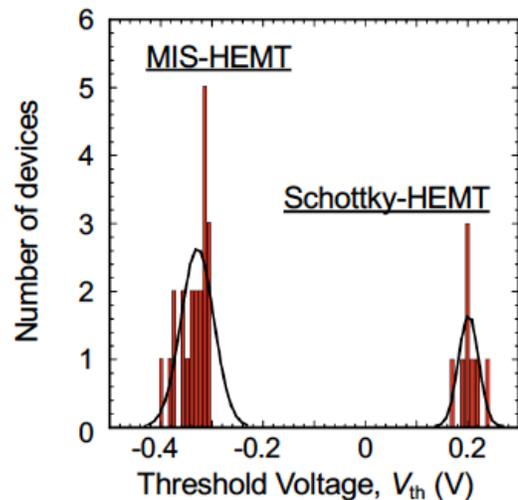


(b)

Fig. 6. (a) I_D - V_D characteristics of recessed-gate AlGaIn MIS-HEMTs with $d_{\text{AlGaIn}} = 8$ nm before PMA process and (b) comparison of their transfer characteristics before and after PMA process.



(a)



(b)

Fig. 7. (a) I_D - V_D characteristics of recessed-gate AlGaIn Schottky-HEMTs with $d_{\text{AlGaIn}} = 8$ nm and (b) histogram of V_{th} values.

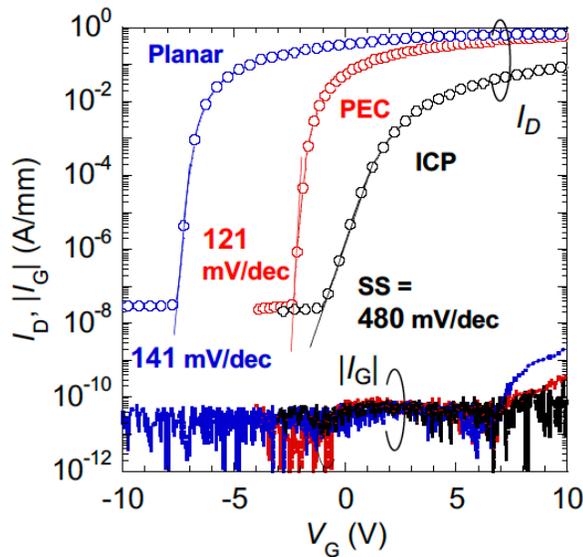


Fig. 8. Transfer characteristics of planar-gate, PEC-etched and dry-etched gate $\text{Al}_2\text{O}_3/\text{AlGaN}/\text{GaN}$ MIS-HEMTs in the saturated region ($V_{DS}=15$ V).

swing, compared with the Schottky-gate HEMTs. The histogram of the V_{th} values obtained for the Schottky-gate and MIS-gate HEMTs is shown in Fig. 7(b), where the V_{th} was defined as the V_G obtained at $I_D = 10^{-6}$ A. We found that the variation in V_{th} was very small for both types of HEMTs, where the standard deviations of 0.019 and 0.032 V were obtained for the Schottky-gate and MIS-gate HEMTs, respectively. For the MIS-gate HEMTs, further improvement was expected by optimizing the device process including the formation of the gate insulator and subsequent annealing process.

Finally, we compared the electrical properties of the PEC-etched-gate HEMTs with those of dry-etched- and unetched planar-gate HEMTs. The dry etching process that we used was inductively-coupled-plasma reactive-ion-etching (ICP-RIE), which was conducted on the AlGaN/GaN heterostructure using a BCl_3/Cl_2 gas mixture. Figure 8 shows semi-log plots of I_D - V_G and $|I_G$ - V_G characteristics measured for the three types of HEMTs at $V_D = 15$ V. We found that the $|I_G|$ was effectively reduced by the MIS-gate HEMTs into the range of 10^{-11} A/mm, which was much smaller than that obtained from the Schottky-gate HEMTs. However, there was a large difference in the sub-threshold slope (SS) obtained from the I_D - V_G characteristics. We obtained an SS of 141 mV/dec for the planar-gate HEMT, whereas the dry-etched-gate HEMT showed a much larger SS of 480 mV/dec. This indicates that the ICP-RIE inevitably resulted in plasma-related-damage to the AlGaN surfaces and/or beneath the 2DEG channel. However, the PEC-etched-gate HEMTs showed the lowest SS of 121 mV/dec, which indicates that the top of the AlGaN layer was etched in accordance with the nature of the low-energy PEC process.

VI. CONCLUSION

We introduced our recent work on PEC etching optimized for fabricating recessed-gate AlGaN/GaN HEMTs. Photo holes generated in the AlGaN layer caused homogeneous and flat etching, in which self-termination was observed. Using light

intensity enabled us to control the depth of self-termination etching. As a consequence, we obtained the desired AlGaN -layer thickness. The PEC-etched Schottky-gate and MIS-gate HEMTs showed good I - V characteristics with constant saturation current and pinch-off behavior and small variation in the V_{th} on one chip. For the MIS-gate HEMTs, the PMA process further improved g_m and SS, compared with those of planar-gate and dry-etched-gate MIS-gate HEMTs. These results suggest that no significant damage was induced in the AlGaN/GaN heterostructures during the PEC etching process. We can conclude that PEC etching is preferable for fabricating recessed-gate structures.

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