Impact of Low-Temperature Annealing on Defect Levels Generated by Mg-Ion-Implanted GaN

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The impact of low-temperature annealing on Mg-ion-implanted GaN with a low dosage (1.5×10^{11} cm^{-2}) has been investigated using MOS diodes. Low-temperature annealing was carried out for Mg-ion-implanted GaN in the temperature range from 400°C to 700°C before forming the insulator/semiconductor interface of the tested MOS diodes. Upon annealing, the hysteresis and the slope of the capacitance–voltage (*C–V*) curves, which were affected by deep levels in the GaN bulk, were changed with the annealing temperature. In particular, the shape of *C–V* curve was changed by annealing at a temperature as low as 500°C. The *C–V* curves were found to be reproducible by a simulation in which the dominant deep levels were assumed to be located at 0.1 eV and 0.7 eV below the conduction band edge. Considering the low recovery temperature and low dosage, the possibility of the existence of simple defects after implantation is discussed.

1. Introduction

GaN has been used in the development of optoelectronic devices, especially light-emitting diodes[1, 2]. It is also a promising material for constructing high-power electronic devices[3,4] because it has a wide bandgap, a high breakdown field, a high electron saturation velocity, and even a high electron mobility at a heterointerface with III-nitride alloys such as AlGaN and InAlN. To construct a high-power device, ion implantation technology is a convenient method when applicable. However, for GaN, the formation of a p-type region by ion implantation is difficult. Although Mg ion implantation is considered to be the most promising method of forming a p-type region, the activation ratio is usually low even if the large activation energy of 160 meV[5–7] is taken into account. Recently, the successful formation of a p-type region in GaN by Mg ion implantation has been reported[8–15]. Nevertheless, the achievement of the theoretical upper limit of the activation ratio, which is as high as 10%, has only been reported in the case of using a particular type of rapid thermal annealing (RTA), *i.e.*, multicycle RTA, in which the temperature was raised up to 1,350°C in N_2 overpressure[11]. Using a conventional RTA technique up to 1,250°C, the highest activation ratio has been reported to be 2.3%[15]. To employ Mg ion implantation as a useful technology, a means of controlling the defects should be found. Narita et al. performed coimplantation with Mg and H ions to enhance the substitution of Ga by Mg while suppressing carrier compensation by N vacancies, V_N, resulting in the suppression of the forward leakage current and the dispersion of current in the fabricated p-n junction diodes[14]. On the basis of a positron annihilation spectroscopy (PAS) study, Uedono et al. found that a complex of a Ga vacancy, V_{Ga}, and a V_N is dominant after Mg ion implantation and that vacancies agglomerate upon high-temperature annealing above 1,000°C[16, 17]. A common result among these preceding reports is that a high temperature above 1,200°C is necessary to control the defects and to activate the Mg atoms as acceptors. In addition, the dosage or concentration of the implanted Mg atoms was relatively high in these reports. An investigation of the impact of low-temperature annealing on defect levels in lightly implanted GaN may provide another clue to control defects.

We previously reported that a deep level located at 0.76 eV below the conduction band edge, E_C, (E_C – 0.76 eV), was detected using a MOS diode fabricated on lightly

Mg-ion-implanted GaN without high-temperature (>1,200ºC) annealing for activating Mg acceptors[18]. Alfieri et al. also reported the results of deep-level transient spectroscopy (DLTS) for lightly Mg-ion-implanted GaN, in which deep levels between E_C – 0.2 eV and E_C – 1.2 eV were detected before and after annealing at temperatures up to 1,000ºC[19]. However, the optimum annealing temperature for reducing the defect concentration has not been clarified. It is possible that another type of defect is generated by annealing, especially at the GaN surface. To clarify the thermal behavior of the defects generated by Mg ion implantation, the defects generated by implantation should be separated from those generated by annealing.

In this report, we investigated the impact of low-temperature annealing on the defect levels generated in lightly Mg-ion-implanted GaN before high-temperature annealing using MOS structures. Since a MOS diode can provide information on the near-surface region when it is biased to an accumulation voltage, the energy levels near E_C can be detected even at room temperature. This feature makes it advantageous over a Schottky barrier diode.

2. Experimental

Samples were prepared as shown in Fig. 1 (a) and described as follows. A Si-doped n-GaN layer (3 μm thick, $n = 5\times10^{17}$ cm^{-3}) was grown on a free-standing n$^+$-GaN substrate via an n$^+$-GaN buffer layer by metalorganic chemical vapor deposition. Mg ion implantation was carried out at room temperature with an energy of 50 keV, an angle of 7º, and a dosage of 1.5×10^{11} cm^{-2}. TRIM simulation results for this condition are shown in Fig. 1 (b). The maximum Mg concentration was estimated to be ~2×10^{16} cm^{-3}. However, the concentrations of V_{Ga} and V_N were calculated to be much higher values of ~1×10^{19} cm^{-3} and ~6×10^{18} cm^{-3} at the maximum, respectively. Therefore, the detection of deep levels should be straightforward for the sample prepared here. After ion implantation, a 20-nm-thick Al_2O_3 layer was deposited by atomic layer deposition (ALD) using trimethylaluminum and H_2O at a substrate temperature of 300ºC. Annealing was carried out at 400 – 800ºC in N_2 flow using an Al_2O_3 surface protection layer, which was followed by the removal of the Al_2O_3 layer by wet etching with a solution of HF:NH_4F = 1:5. Then, a 30-nm-thick ALD Al_2O_3 layer was deposited again, which was followed by the metallization of a top electrode of Ni/Au to form a MOS structure and a back ohmic

contact of Ti/Au. Finally, post-metallization annealing (PMA) for reducing the interface states[20, 21] was carried out at 300ºC in air. For comparison, a MOS diode sample without cap annealing above 300ºC was also prepared. This sample is hereafter referred to as the "300ºC-annealed sample" because the ALD and PMA were done at 300ºC. Furthermore, samples without Mg ion implantation were also fabricated in the same process sequence. For the completed MOS diodes, capacitance–voltage (*C–V*) measurement was carried out at a frequency of 1 MHz. Then, a simulation for reproducing the *C–V* curves was performed to obtain information on the defect levels.

3. Results and discussion

3.1 Impact of annealing on n-GaN samples without Mg ion implantation

Low-temperature annealing after ion implantation might be an efficient way of reducing the concentration of defects in the implanted region. Therefore, the thermal behavior of the defects can be investigated by annealing. However, annealing at an excessively high temperature can generate another type of defect, particularly at the GaN surface, which results in the distortion of the *C–V* curves of the tested MOS diodes by the interface defects. To determine the upper-limit temperature, n-GaN samples without Mg ion implantation were annealed.

The measured *C–V* curves are shown in Fig. 2. The 300ºC-annealed sample without implantation showed excellent *C–V* characteristics without hysteresis as shown in Fig. 2 (a). The shape of the *C–V* curve is almost the same as the ideal curve (indicated by the broken lines). These excellent characteristics were obtained by PMA as reported in Refs. 20 and 21. However, we found that annealing at 800ºC, even before the formation of the interface, deteriorated the *C–V* characteristics, as shown in Fig. 2 (b), where a large hysteresis and a large bump appeared. The interface state density D_{it} distribution was evaluated for both samples using the Terman method[22]. Since the D_{it} distribution of the 300ºC-annealed sample was below the detection limit in the energy range where the Terman method can be applied, the result only for the 800ºC-annealed sample is plotted in Fig. 2 (c). The 800ºC-annealed sample exhibited a high D_{it} distribution with a discrete state at 0.63 eV. Usually, a U-shaped D_{it} distribution in a band gap should be observed[23–26]. However, when the concentration of a specific defect in the vicinity of the surface is very

high, a discrete type of interface state can be observed[27, 28]. Therefore, the discrete level observed here should have originated from a surface defect generated during the 800°C annealing.

On the basis of these results, we determined that the annealing temperature should be lower than 800°C. The upper-limit temperature of 800°C might have resulted from poly-crystallization in the Al_2O_3 layer[29, 30]. In the present sample fabrication process, however, the Al_2O_3 cap layer was removed after 800°C annealing. Therefore, it is highly likely that a defect was introduced in the vicinity of the GaN surface by 800°C annealing, and that the detected interface defect existed on the GaN side of the interface of the finally completed MOS structure. Although a SiN layer can be used as a cap layer at 800°C without generating the surface defect[30], we used ALD Al_2O_3 layer because the surface damage during deposition was prevented by ALD. Using plasma CVD or sputtering, the GaN surface might be damaged, which may persist after low-temperature annealing and may affect the characteristics of the completed MOS diodes. As described later, the temperature range up to 700°C was sufficient for investigating the thermal behavior of the defects generated by Mg ion implantation.

3.2 Impact of annealing on Mg-ion-implanted GaN samples

Next, we investigated the impact of low-temperature annealing on implanted samples. As shown in Figs. 3 (a) and (b), after annealing at 300°C and 400°C, the *C–V* characteristics have an anomalously steep region compared with the ideal curve assuming no implantation, resulting in a sharply bent shape. This cannot be explained by only assuming the existence of high-density interface states. Instead, this can be explained by the existence of a defect level that compensates the donor. Therefore, deep acceptor-like levels are considered to have existed in the bulk of the Mg-ion-implanted GaN layer. Considering the hysteresis caused by a bias sweep of 50 mV/s (one 50 mV step per s), the time constant for the corresponding deep levels is roughly estimated to be on the order of 1 to 100 s. The time constant of the electron emission from a deep levels can be estimated by[19, 31]

$$\tau = \frac{1}{\sigma v_{th} N_C} exp\left(\frac{E_C - E_T}{kT}\right), \quad (1)$$

where σ is the capture cross section, v_{th} is the electron thermal velocity, N_C is the effective density of states at the conduction band bottom, E_T is the energy of the deep level, k is the Boltzmann constant, and T is the temperature. If we consider that the measured σ [19, 32–34] is usually on the order of 1×10^{-15} cm^{-2} to 1×10^{-16} cm^{-2}, ($E_C - E_T$) for the dominant deep level is roughly estimated to be 0.6 – 0.8 eV below E_C.

The *C–V* curves obtained for the samples annealed at 500ºC and 600ºC are shown in Figs. 4 (a) and (b), respectively. In this temperature range, improved *C–V* characteristics can be seen. The *C–V* curves have rounded shapes, while the hysteresis is also minimized for these samples. It should be noted that annealing at a temperature as low as 500ºC affected the electric properties of implanted GaN. Nevertheless, the anomalously steep region still existed for both *C–V* curves. Therefore, the defects are considered to have been partially recovered in this temperature range.

Annealing at a higher temperature resulted in more pronounced changes in *C–V* characteristics. The result for the sample annealed at 700ºC is shown in Fig. 5, where it can be seen that the anomalously steep region has been minimized. A slight increase in hysteresis and the appearance of a small bump can be seen, which are highly likely to have resulted from the interface defect generated at the GaN surface by annealing. Therefore, a slight amount of the interface or surface defects on the GaN side were generated by annealing at 700ºC. Nevertheless, the shape of the *C–V* curve measured for the sample annealed at 700ºC is the most similar to the ideal curve, which means that annealing at 700ºC is efficient for reducing the concentration of defects generated by Mg ion implantation. This result indicated that the concentration of the bulk defects generated by implantation were reduced at a temperature much lower than that used for activation of Mg, which is typically above 1,200ºC.

3.3 Simulation results to find dominant levels

We carried out a simulation to reproduce the *C–V* curve on a computer using a simulator developed previously by K. Nishiguchi[21, 35]. In our previous work[18], we assumed a D_{it} distribution and a reduction in carrier concentration to fit the experimental curve without assuming a bulk deep level. Here, the simulation was carried out by

assuming the D_{it} distribution and the deep levels in the GaN bulk. To simplify the simulation, the profile of the deep-level distribution in the bulk was assumed to be an exponential function.

The simulation result for the 300°C-annealed sample is shown in Fig. 6 (a), where the D_{it} distribution shown in Fig. 6 (b) and the profile of bulk deep levels shown in Fig. 6 (c) were assumed. Excellent fitting was obtained by the simulation without assuming a high D_{it}. Here, it was necessary to assume the co-existence of a donor-like deep level at E_C – 0.1 eV and an acceptor-like deep level at E_C – 0.7 eV to reproduce the measured *C–V* curves. The existence of an acceptor-like deep level at E_C – 0.7 eV as the main deep level is in good agreement with a recent DLTS study, where the dominant acceptor-like deep levels were detected around E_C – 0.7 eV in GaN after Mg ion implantation under similar conditions[19]. In addition, a deep level at E_C – 0.67 eV that disappeared upon annealing at 900°C was also detected by DLTS for N-implanted GaN[36], although the implanted element was not Mg. Furthermore, our previous assumption of a deep level at E_C – 0.76 eV in a different type of simulation[18] is also in good agreement with the current results. In Fig. 6 (c), the TRIM simulation results of V_{Ga} and V_N concentration profiles for the as-implanted situation shown in Fig. 1 (b) are also plotted, which is discussed later.

Excellent fitting was also obtained for the sample annealed at 700°C, as shown in Fig. 7 (a), by assuming the D_{it} distribution plotted in Fig. 7 (b) and the profile of bulk deep levels plotted in Fig. 7 (c). The D_{it} distribution includes the surface defect level that was found for the sample annealed at 800°C without Mg ion implantation, as shown in Fig. 2 (b), in order to reproduce the small bump in the *C–V* curve. It should be noted that there was no need to assume the donor-like level. The assumption of an acceptor-like deep level at E_C – 0.7 eV with low D_{it} was sufficient to fit the *C–V* curves.

We found that the assumption of the donor-like deep level at E_C – 0.1 eV is not necessary to fit the experimental curve for the samples annealed at 500°C and higher. Consequently, it is likely that the concentration of the donor-like defects was reduced down to the detection limit upon annealing at 500°C. On the basis of the results of an iterative simulation by assuming the same decay depth with that of the E_C – 0.7 eV level, the maximum donor-like-state concentration not to obstruct curve fitting is plotted in Fig. 7 (c) as an example detection limit. According to the previous reports on electron-irradiated

GaN, V_N was found to recover at 300°C in a PAS study[37] and the deep level corresponding to V_N is located 0.1 – 0.2 eV below E_C[38–40]. Therefore, considering the recovery temperature and the location in the band gap, the donor-like deep level at E_C – 0.1 eV may be assigned to a defect related to V_N. On the other hand, the concentration of acceptor-like deep levels at E_C – 0.7 eV was reduced by almost one order at 700°C. Considering that the recovery temperature is as low as 700°C and that the dosage is low, the origin of the acceptor-like deep level might be a simple defect such as V_{Ga}. Actually, it has been found that V_{Ga} recovered at 500 – 800°C on the basis of a PAS study for electron-irradiated GaN[37)]. According to Fig. 6 (c), the concentration of E_C – 0.7 eV levels in the sample without 700°C annealing is comparable with that of V_{Ga} calculated by the TRIM simulation for the as-implanted situation, although the thermal treatment is different. Heating at 300°C during ALD and PMA might have resulted in the reduction in the concentration of V_N-related defects. Therefore the assignment described above is reasonable. In addition, the simulation in the present work is appropriate. However, a recent PAS study showed that the complex defect of V_{Ga} and V_N is dominant after Mg ion implantation[16, 17], although the dosage is much higher than that in this work. Therefore, the complex defect cannot be completely ruled out at this stage.

4. Conclusions

The impact of low-temperature annealing on Mg-ion-implanted GaN with a low dosage (1.5×10^{11} cm^{-2}) was investigated using MOS diodes. Low-temperature annealing was carried out for Mg-ion-implanted GaN in the temperature range from 400°C to 700°C before the formation of the insulator/semiconductor interface of the tested MOS diodes. The *C–V* characteristics, which were affected by deep levels in the GaN bulk, changed with the annealing temperature. In particular, the shape of *C–V* curve was changed by annealing at a temperature as low as 500°C. We found by the simulation of the *C–V* curves that the deep levels at E_C – 0.1 eV and at E_C – 0.7 eV explained the observed phenomena. Considering the low recovery temperature and low dosage, the possibility of the existence of simple defects after implantation was discussed.

Acknowledgments

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Figure Captions

Fig. 1. (a) Sequence of sample preparation. For comparison, samples without process (A) and/or process (B) were also fabricated. (b) TRIM simulation results for concentration of implanted Mg, generated V_{Ga}, and V_N.

Fig. 2. Measured *C–V* characteristics and D_{it} distributions for the samples without Mg ion implantation. (a) *C–V* characteristics for 300°C-annealed sample. (b) *C–V* characteristics for 800°C-annealed sample. (c) D_{it} distributions.

Fig. 3. Measured *C–V* characteristics for the Mg-ion-implanted samples. (a) 300°C-annealed sample. (b) 400°C-annealed sample.

Fig. 4. Measured *C–V* characteristics for the Mg-ion-implanted samples. (a) 500°C-annealed sample. (b) 600°C-annealed sample.

Fig. 5. Measured *C–V* characteristics for the Mg-ion-implanted samples with annealing at 700°C.

Fig. 6. Simulation result for *C–V* characteristics of the implanted sample after 300°C annealing. (a) *C– V* curves. (b) Assumed D_{it} distribution. (c) Assumed profile of bulk deep levels in comparison with the TRIM simulation results shown in Fig. 1 (b).

Fig. 7. Simulation result for *C–V* characteristics of the implanted sample after 700°C annealing. (a) *C– V* curves. (b) Assumed D_{it} distribution. (c) Assumed profile of bulk deep levels. The fine dotted line shows an example detection limit profile.

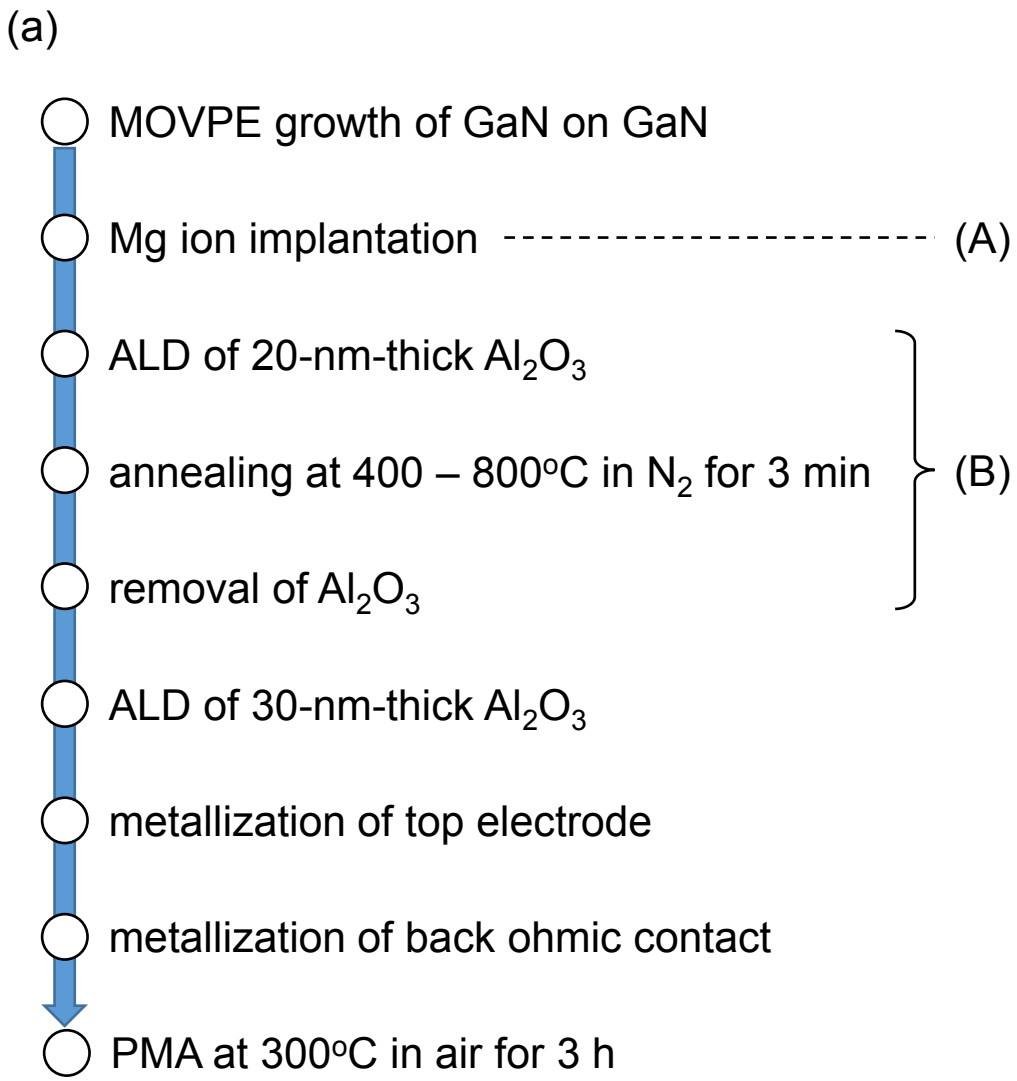
(a)
MOVPE growth of GaN on GaN
Mg ion implantation
(A)
ALD of 20-nm-thick Al_2O_3
annealing at 400 – 800°C in N_2 for 3 min
removal of Al_2O_3
(B)
ALD of 30-nm-thick Al_2O_3
metallization of top electrode
metallization of back ohmic contact
PMA at 300°C in air for 3 h

Fig.1.

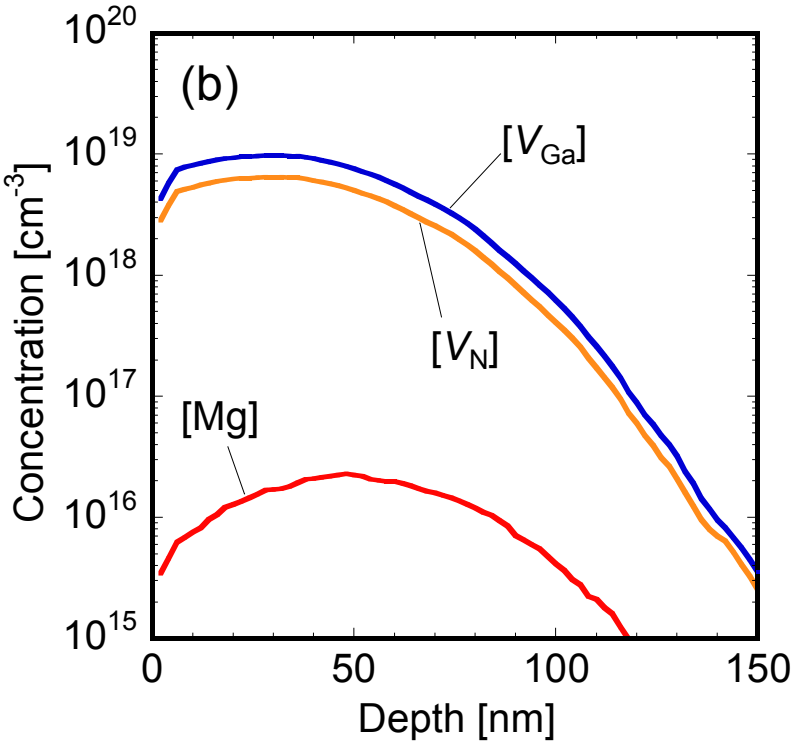
(b)
[V_{Ga}]
[V_N]
[Mg]
Concentration [cm^{-3}]
10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
0
50
100
150
Depth [nm]

Fig. 1

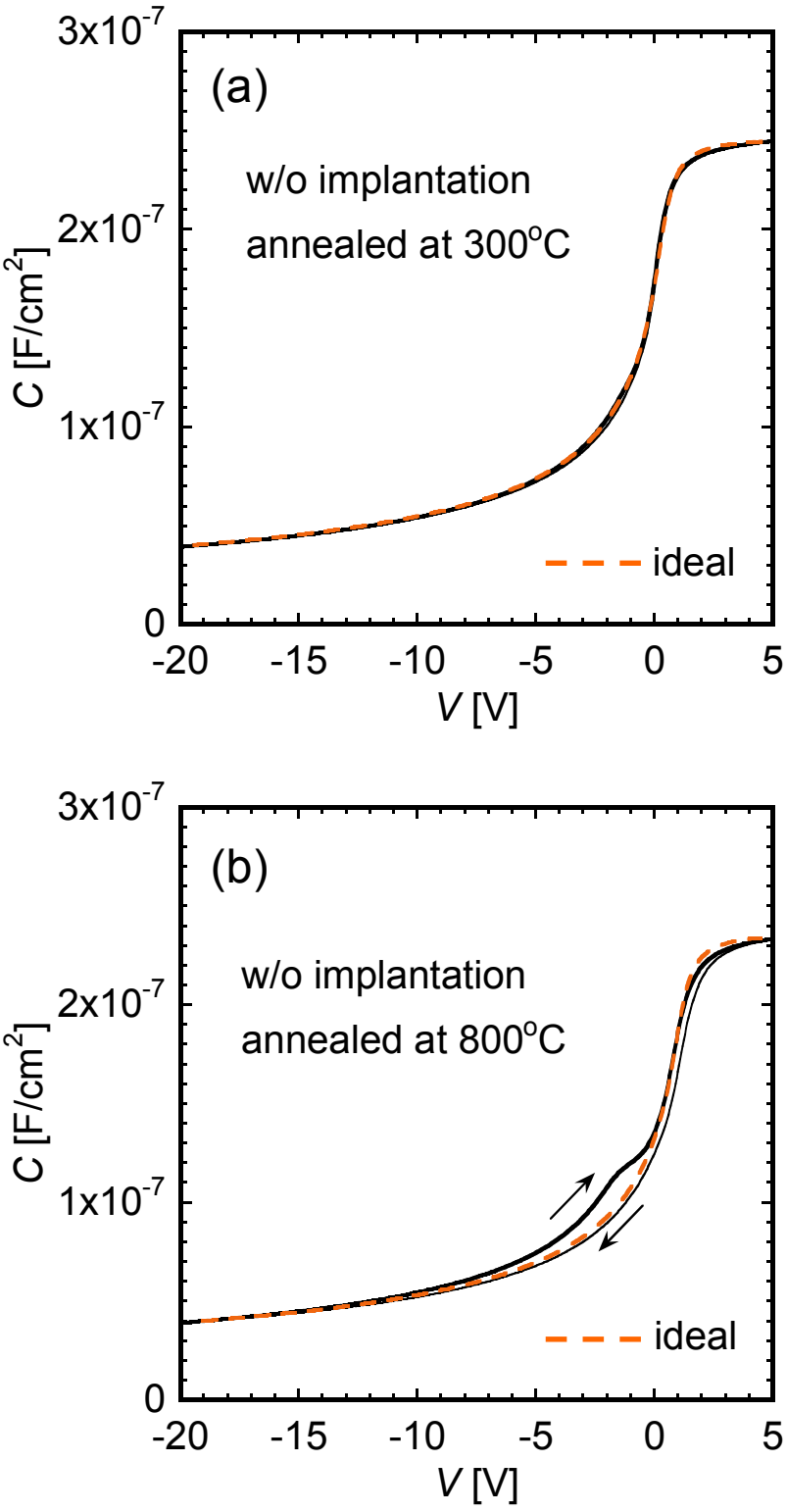
(a)
w/o implantation
annealed at 300°C
ideal
C [F/cm²]
V [V]
3x10⁻⁷
2x10⁻⁷
1x10⁻⁷
0
-20
-15
-10
-5
0
5
(b)
w/o implantation
annealed at 800°C
ideal
C [F/cm²]
V [V]

Fig. 2.

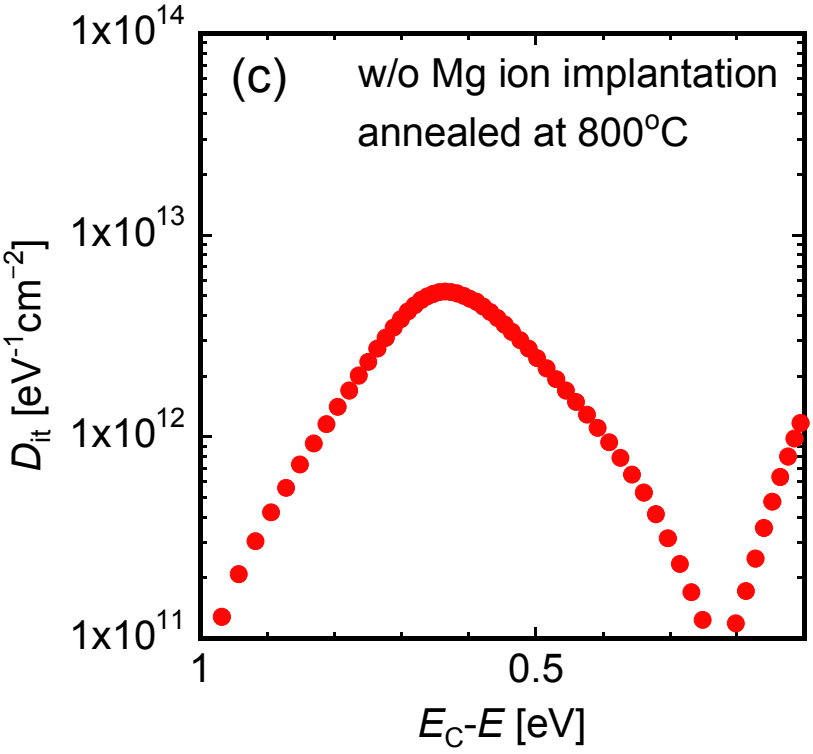
(c)
w/o Mg ion implantation
annealed at 800°C
1x10^14
1x10^13
1x10^12
1x10^11
D_it [eV^-1cm^-2]
1
0.5
E_C-E [eV]

Fig. 2.

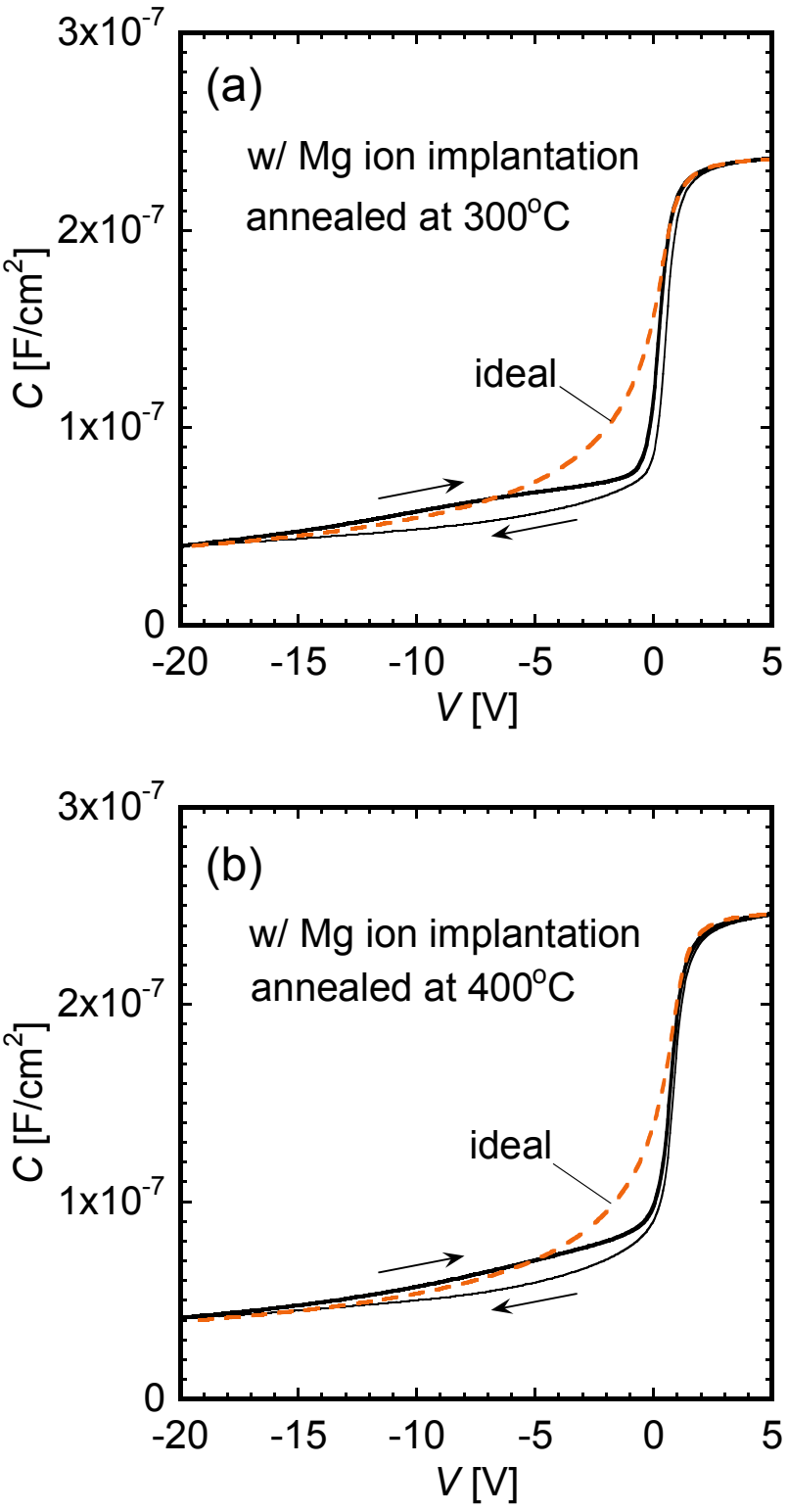
(a)
w/ Mg ion implantation
annealed at 300°C
ideal
C [F/cm²]
V [V]
3x10⁻⁷
2x10⁻⁷
1x10⁻⁷
0
-20
-15
-10
-5
0
5
(b)
w/ Mg ion implantation
annealed at 400°C
ideal
C [F/cm²]
V [V]

Fig. 3.

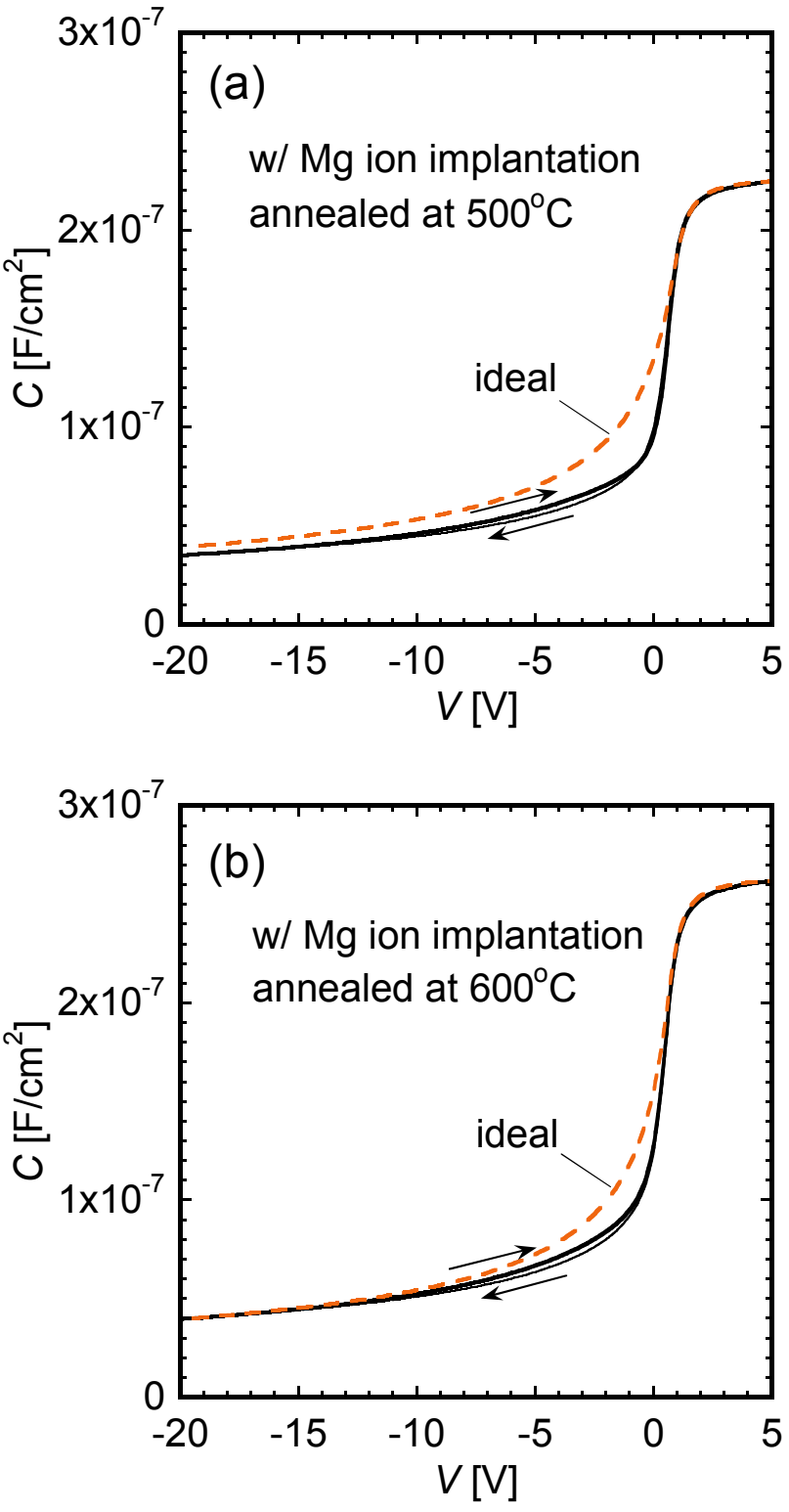
(a)
w/ Mg ion implantation
annealed at 500°C
ideal
C [F/cm²]
V [V]
3x10⁻⁷
2x10⁻⁷
1x10⁻⁷
0
-20
-15
-10
-5
0
5
(b)
w/ Mg ion implantation
annealed at 600°C
ideal
C [F/cm²]
V [V]

Fig. 4.

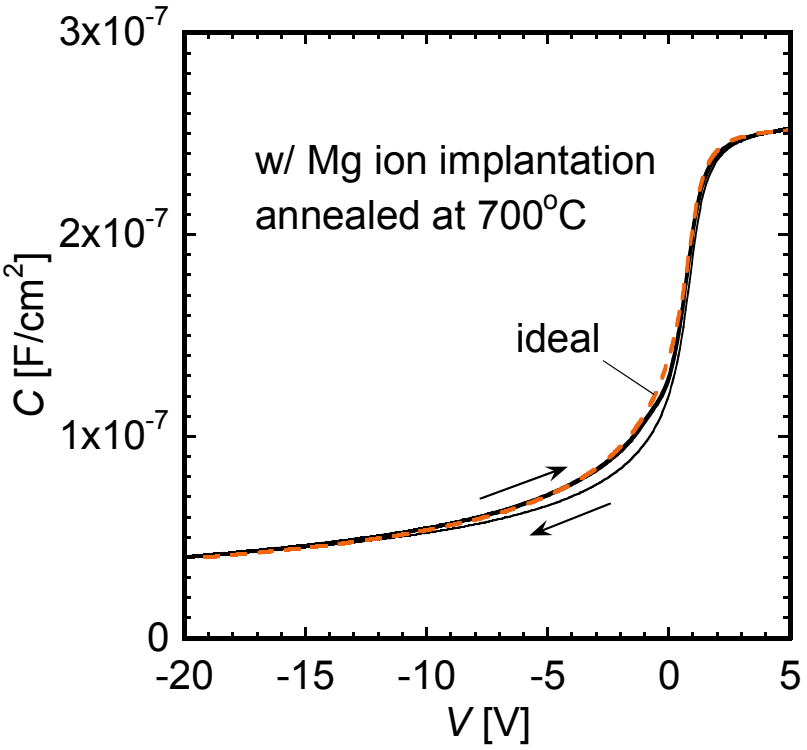
3x10-7
2x10-7
1x10-7
0
C [F/cm2]
w/ Mg ion implantation
annealed at 700°C
ideal
-20
-15
-10
-5
0
5
V [V]

Fig. 5.

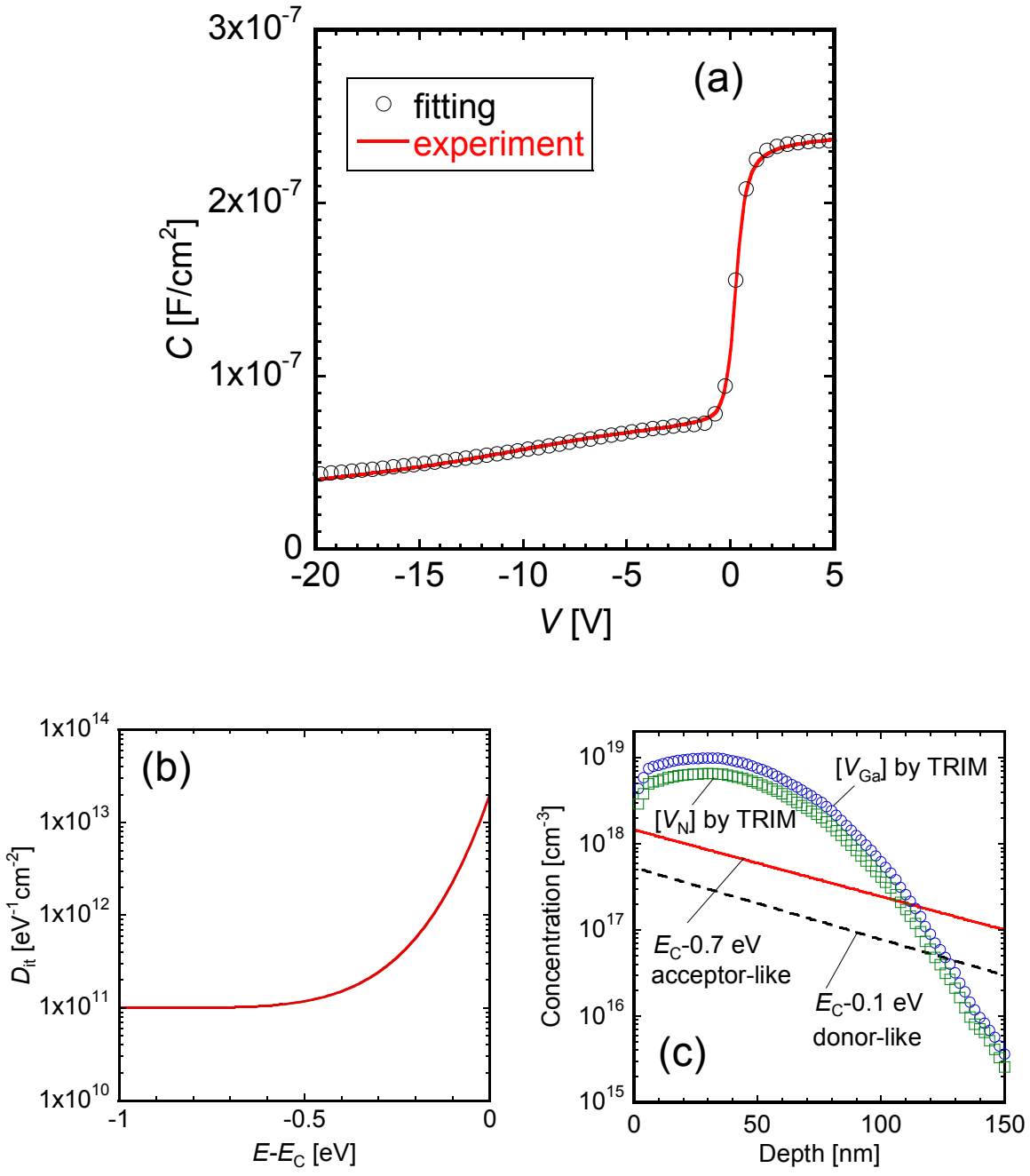
(a)
fitting
experiment
C [F/cm²]
V [V]
(b)
D_it [eV⁻¹cm⁻²]
E-E_C [eV]
(c)
[V_Ga] by TRIM
[V_N] by TRIM
E_C-0.7 eV
acceptor-like
E_C-0.1 eV
donor-like
Concentration [cm⁻³]
Depth [nm]

Fig. 6.

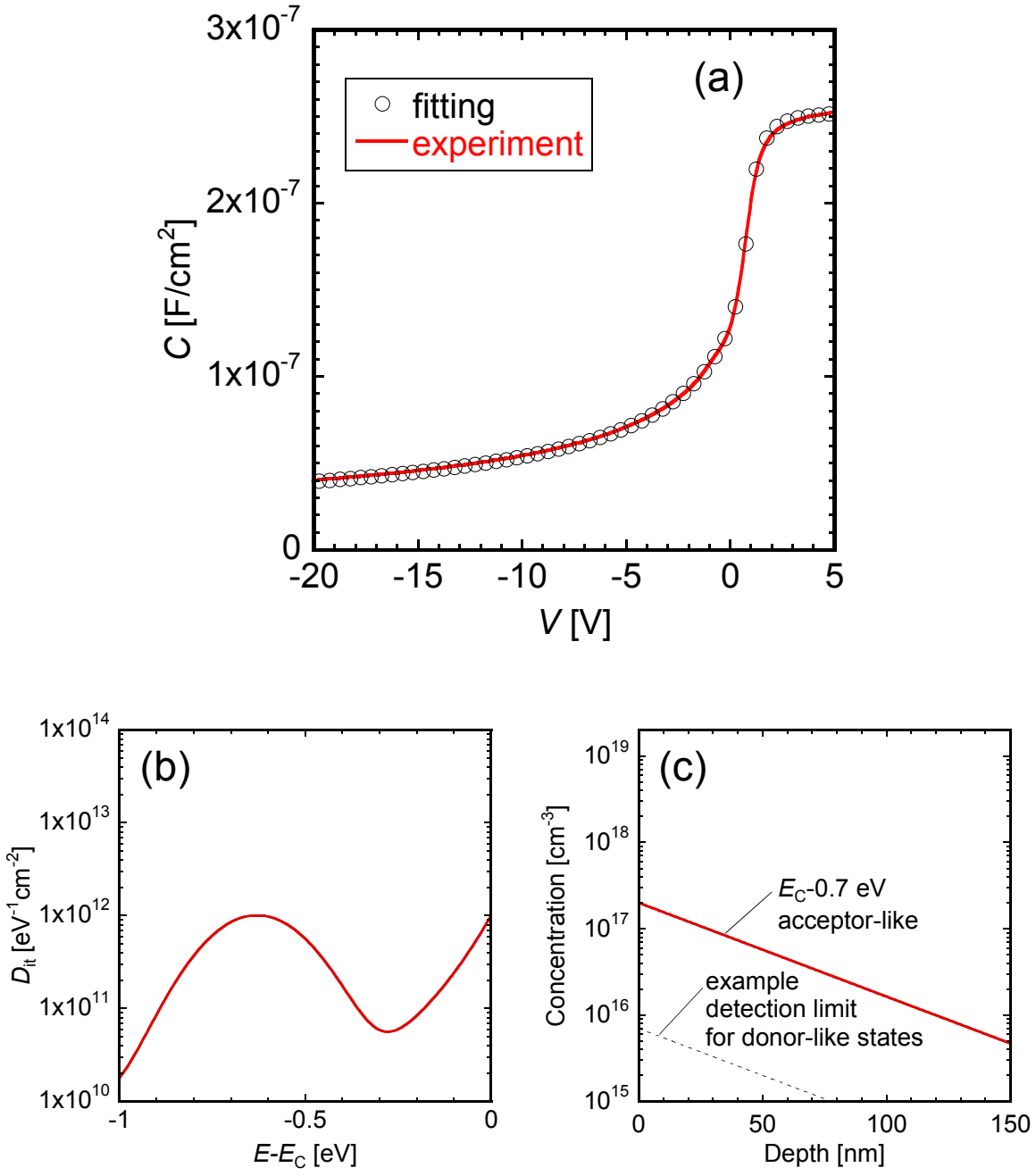
(a)
fitting
experiment
C [F/cm2]
V [V]
(b)
Dit [eV-1cm-2]
E-EC [eV]
(c)
Concentration [cm-3]
EC-0.7 eV
acceptor-like
example
detection limit
for donor-like states
Depth [nm]

Fig. 7.