Analysis of simultaneous occurrence of shallow surface Fermi level pinning and deep depletion in MOS diode with Mg-ion-implanted GaN before activation annealing

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The characteristics of a MOS diode with Mg-ion-implanted GaN before activation annealing were investigated. Mg ion implantation onto n-GaN with slightly high Si doping concentration (5×10^{17} cm^{-3}) was performed with a moderate dosage (1.5×10^{12} cm^{-2}). The completed MOS diode showed n-type features. The capacitance–voltage (*C–V*) and capacitance–frequency (*C–f*) characteristics of the MOS diode indicated that shallow surface Fermi level pinning and deep depletion occurred simultaneously. By applying the conductance method to the measured *C–f* characteristics, a discrete level at 0.2–0.3 eV below the conduction band edge was detected. On the basis of the simulation of the high-frequency-limit *C–V* curve, the detected discrete level distributed in the bulk of n-GaN rather than at the insulator/semiconductor interface, so that it caused surface Fermi level pinning at a relatively shallow energy level and deep depletion owing to its acceptorlike nature simultaneously.

1. Introduction

GaN is a promising material for constructing high-efficiency power devices[1–3] because it has a wide bandgap[3], a high breakdown field[4], a high electron saturation velocity[5], a high electron mobility[3], and good thermal conductivity[3]. Since an excellent insulator/GaN interface can be formed without difficulty[6–8], a vertical GaN MOS field-effect transistor is one of the candidate power devices for realizing efficient electric power saving. It can also provide two-dimensional electron gas with high mobility at a heterointerface with III-nitride alloys, enabling the construction of a high-electron-mobility transistor as a high-frequency high-power device.

Ion implantation technology is convenient for achieving a selective doping area in a high-power device, when applicable. However, for GaN, the formation of a p-type region by ion implantation has been difficult. Although Mg ion implantation is the most promising method for achieving p-type conduction, the activation ratio is usually low even if a large activation energy, such as larger than 200 meV[9–11], is considered. Recently, however, successful achievements of a p-type region in GaN by Mg ion implantation have been reported[12–20]. The theoretical upper limit of the activation ratio, which is as high as 10%, has been achieved by a particular rapid thermal annealing (RTA), *i.e.*, multicycle RTA, in which the temperature was increased in a fashion of sequential pulses up to 1420 ºC in 2 MPa of N_2 overpressure[12–15]. Furthermore, an ultrahigh-pressure annealing technique for Mg-ion-implanted GaN has been introduced as an effective method of forming a p-type region[19]. Even by a conventional RTA technique at a temperature of 1230–1250ºC, the successful formation of a p-type region[16–18] and a high activation ratio of 2.3% have been reported for Mg-ion-implanted GaN[20]. A common result among these reports is that a high temperature (≥1230ºC) is necessary to activate the Mg atoms as acceptors[16, 17].

To employ Mg ion implantation as a reliable technology, defects should be minimized. For this purpose, we should investigate the defects in GaN generated by Mg ion implantation. By positron annihilation spectroscopy (PAS), Uedono et al. found that a complex of a Ga vacancy, V_{Ga}, and N vacancy, V_N, is a dominant vacancy-type defect after Mg ion implantation[21, 22]. By deep-level transient spectroscopy (DLTS), Alfieri et al. reported the annealing behavior of defect levels up to 1000ºC[23]. They found deep levels located at 0.2–1.2 eV below the conduction band edge E_C. Narita et al. performed

coimplantation with Mg and H ions to enhance the substitution of Ga by Mg while suppressing carrier compensation by V_N. This approach resulted in the suppression of the forward leakage current and the current dispersion in p-n junction diodes[18].

We previously reported that a deep level located at 0.7–0.8 eV below E_C was detected using a MOS diode fabricated on lightly (1.5×10^{11} cm^{-2}) Mg-ion-implanted GaN without high-temperature (>1200ºC) annealing for activating Mg acceptors[24, 25]. More recently, we found that an increase in Mg-ion dosage led to a change in the dominant defect level that affected the electrical properties of the MOS diodes[26]. Namely, the dominant defect level in MOS diodes with moderately (1.5×10^{12} cm^{-2}) Mg-ion-implanted GaN before activation annealing was located between E_C – 0.2 eV and E_C – 0.3 eV[26]. Still, the electrical properties of the fabricated MOS diodes with moderate Mg ion dosage are not yet fully understood. In particular, the following things were not clarified.

1) Although the dominant defect level was relatively shallow, deep depletion was observed. The reason for this is unclear.
2) The type, *i.e.*, donorlike or acceptorlike, of the dominant defect level is unclear.

It is useful to deepen our understanding of these, not only for ion implantation but also for MOS physics. In this work, the MOS diode with moderately Mg-ion-implanted GaN is further investigated to clarify these unclear things.

2. Experimental procedure

Samples were prepared as shown in Fig. 1(a) and as described below. A Si-doped n-GaN layer (3 μm thick, $n = 5\times10^{17}$ cm^{-3}) was grown on a free-standing n^+-GaN (0001) substrate via an n^+-GaN buffer layer by metalorganic vapor phase epitaxy (MOVPE). Mg ion implantation was carried out at room temperature with an energy of 50 keV, an angle of 7º, and a dosage of 1.5×10^{12} cm^{-2}. The transport of ions in matter (TRIM) simulation under these conditions indicated that the maximum Mg concentration was estimated to be ~2×10^{17} cm^{-3} and that the concentrations of V_{Ga} and V_N were calculated to be much higher as shown in Fig. 1 (b). Although the distribution profiles of complex defects cannot be obtained by this simulation, the result indicates that high-concentration defects are introduced in the near-surface region by Mg ion implantation. Therefore, the detection of deep levels should be straightforward for the sample prepared here. After ion implantation,

a 30-nm-thick Al_2O_3 layer was deposited by atomic layer deposition (ALD) using trimethylaluminum and H_2O at a substrate temperature of 300ºC, followed by the metallization of a top electrode of Ni/Au to form a MOS structure and a back ohmic contact of Ti/Au. The completed MOS structure is schematically shown in Fig. 1(c). Finally, postmetallization annealing (PMA) for reducing the interface state density[23–25] was carried out at 300ºC in air. For the completed MOS diodes, capacitance–voltage (*C–V*) and capacitance–frequency (*C–f*) measurements were carried out. Then, a simulation for reproducing the *C–V* curves was performed to obtain information on the defect levels.

3. Results and discussion

3.1 *C–V* and *C–f* characteristics

The high-frequency *C–V* curves measured in a frequency range from 1 to 5 MHz are plotted in Fig. 2. It can be seen that the *C–V* curve approaches the flat feature at the high-frequency limit, which means strong pinning of the Fermi level. Overall, the capacitance is much smaller than the oxide capacitance C_{OX}, indicating a deep depletion feature. The plateau capacitance corresponds to the depletion width of approximately 150 nm. If the carrier concentration was not changed from that in the as-grown GaN, this deep depletion cannot be caused by the surface Fermi level pinning in the band gap. Therefore, a bulk defect state that compensates for the Si donors should have been generated in GaN by Mg ion implantation.

The *C–f* characteristics measured in a frequency range from 100 Hz to 5 MHz are shown in Fig. 3. The capacitance converges to the deep depletion capacitance at the high frequency even if a high positive bias voltage is applied, which is further evidence of strong Fermi level pinning that causes a deep depletion. However, the capacitance change occurs in a relatively high frequency range, which indicates that the cause of the observed frequency dispersion is a relatively shallow gap state. Consequently, the MOS diode with Mg-ion-implanted GaN exhibited electric properties with a dual nature.

The electron-emission time constant τ of an electron trap level can be estimated by[23, 27, 28]

$$\tau = \frac{1}{\sigma v_{th} N_C} exp\left(\frac{E_C - E_T}{kT}\right), \quad (1)$$

where σ is the capture cross section, v_{th} is the electron thermal velocity, N_C is the effective density of states at E_C, E_T is the energy of the electron trap level, k is the Boltzmann constant, and T is temperature. According to this equation, C–f characteristics in the frequency range from 100 Hz to 5 MHz should be affected by the trap level at 0.2–0.5 eV from the conduction band edge.

By applying the conductance method to the measured C–f characteristics, the interface state density D_{it} distribution was derived as follows. At a certain bias voltage, the frequency-dependent conductance G_p due to the interface states as a function of the measurement frequency f (or $\omega=2\pi f$) is given by[29)]

$$\frac{G_p}{\omega} = \frac{C_{OX}^2\left(G_m/\omega\right)}{\left(G_m/\omega\right)^2+(C_{OX}-C_m)^2}, \tag{2}$$

where G_m and C_m are the measured conductance and capacitance, respectively. If the time constant of the interface state is singly determined to be τ, G_p is related to the frequency-independent capacitance C_{it} by

$$\frac{G_p}{\omega} = \frac{\omega\tau}{1+\omega^2\tau^2}C_{it}. \tag{3}$$

Figure 4(a) shows plots of G_p/ω for each bias voltage as a function of f by the solid circles, where the solid lines indicate the fitting based on the calculation using Eq. (3). It can be seen that the conductance peaks at 10^3–10^5 Hz are well fitted by the single-time-constant model expressed by Eq. (3). Once C_{it} is obtained, D_{it} is obtained by

$$D_{it} = \frac{C_{it}}{q^2}.$$

By applying Eq. (1) to derive energy of interface states in the band gap, the D_{it} distribution was obtained as shown in Fig. 4(b) where $\sigma = 1\times10^{-16}$ cm^2 was assumed as a typical value measured by DLTS[30)]. An abrupt increase in D_{it} can be seen at E_C – 0.27 eV, indicating the existence of a discrete level in the band gap. Namely, a discrete level at 0.27 eV was

detected. According to the disorder-induced gap state (DIGS) model[31, 32], the D_{it} distribution should exhibit a U-shaped feature resulting from the incomplete separation of bonding and antibonding states. Even for insulator/III-nitride interfaces, U-shaped D_{it} distributions have been measured[33, 34]. However, in the case where high-density bulk defects exist in the near-surface region, a discrete level can be observed in the D_{it} distribution[35, 36]. Therefore, the discrete level in Fig. 4(b) should indicate the existence of a bulk defect level. According to previous reports[30, 37–39], this discrete level can be assigned to the divacancy V_{Ga}–V_N, even when considering the variation of σ, as is discussed later.

3.2 Simulation of *C*–*V* curve

To investigate the properties of the detected discrete level, the *C*–*V* curve was simulated using a simulator developed previously[40, 41]. First of all, the possibility that the observed electric properties of the Mg-ion-implanted sample were dominated by the interface states should be examined. Therefore, we assumed that the detected D_{it} distribution is a part of the U-shaped distribution of the interface states, and that there are no defect levels in the Mg-ion-implanted GaN. The result is shown in Fig. 5 where the solid line in the inset indicates the assumed D_{it} distribution. Even assuming an abrupt increase in the D_{it} around E_C – 0.2 eV, the plateau with the deep depletion capacitance of the measured *C*–*V* curve cannot be reproduced. This is a reasonable result considering that the Fermi level should be pinned at a relatively shallow energy point where the abrupt increase in D_{it} occurs, resulting in a saturation of the *C*–*V* curve at a high capacitance under the positive bias region. Therefore, it is unlikely that the interface states caused the observed deep depletion.

Considering the above, the possibility that the detected discrete level is a bulk defect level should also be examined. For this purpose, a simulation assuming bulk defect levels was carried out. We found that the assumption of distribution profiles as shown in Fig. 6 for an acceptorlike bulk defect level at E_C – 0.27 eV and a donorlike bulk defect level at E_C – 0.07 eV can reproduce the measured *C*–*V* curve with a deep-depletion capacitance. The simulation result for the *C*–*V* curve is shown in Fig. 7. Fermi level pinning at a deep depletion capacitance is well reproduced by assuming relatively shallow defect levels. We found that the acceptorlike bulk defect level at E_C – 0.27 eV mainly reproduced the plateau of the *C*–*V* curve. Since an additional positive charge was needed to adjust the horizontal

shift to obtain the best fit, a very shallow donorlike level at E_C – 0.07 eV with the profile shown in Fig. 6 was also assumed. The assumption of the very shallow donor level coincides with that in the previous simulation for the MOS *C–V* curve of the Mg-ion-implanted GaN with a lower dosage[25]. This very shallow donor level can be assigned to V_N[42-44].

With the same assumption of defect properties as above, band bending is also simulated. Diagrams of the simulated band bending at different bias voltages are illustrated in Fig. 8. The width of the depletion layer, formed by the acceptorlike defect level at E_C – 0.27 eV distributed in the GaN bulk, did not change at any bias voltage, although the surface potential varied. This is the origin of the wide plateau at a deep depletion capacitance in the *C–V* curve. Meanwhile, the surface Fermi level was pinned at E_C – 0.27 eV even under a high positive bias. This pinning can cause the frequency dispersion resulting in the detection of the discrete level by the conductance method. Consequently, the acceptorlike defect level at E_C – 0.27 eV can cause surface Fermi level pinning at relatively shallow energy level and deep depletion simultaneously.

Note that the acceptorlike nature of the defect level is necessary for causing deep depletion. If a donorlike defect level at E_C – 0.27 eV is assumed as the dominant defect level, the measured plateau with the deep-depletion capacitance cannot be reproduced. Figure 9 shows an example simulation result for the case where a donorlike defect level at E_C – 0.27 eV with the same distribution profile as in Fig. 6 was assumed. Even with changing the defect profile, the measured *C–V* curve was not reproduced. Therefore, the deep depletion cannot be explained by the donorlike defects. Consequently, the detected discrete level at E_C – 0.27 eV is highly likely the acceptorlike defect level distributed in the Mg-ion-implanted GaN.

3.3 Discussion on defect assignment

Since many types of defect are generated by Mg ion implantation, there must be defect levels other than the detected one. Still, it has been indicated that one dominant defect level can determine the *C–V* characteristics of the fabricated MOS diode. Although the energy E_C – 0.27 eV of the detected defect level was determined under the assumption of $\sigma = 1\times10^{-16}$ cm^2, there is the possibility that σ takes another value in the range from

1×10^{-17} to 1×10^{-15} cm^2. Considering this, we should conclude that the energy of the detected defect level is 0.2–0.3 eV below E_C on the basis of Eq. (1). From the results of the DLTS study[30, 37–39], the defect level at 0.2–0.3 eV below E_C can be assigned to V_{Ga}–V_N. On the other hand, the results of the PAS study[21, 22] on as-implanted GaN with a similar Mg concentration indicated that V_{Ga}–V_N is the dominant vacancy-type defect. Therefore, it is highly likely that the detected defect level can be assigned to V_{Ga}–V_N and that this defect level is dominant in the fabricated MOS diode.

4. Conclusions

The characteristics of the MOS diode with Mg-ion-implanted GaN before activation annealing were investigated. Mg ion implantation onto n-GaN with a slightly high Si doping concentration was performed with a moderate dosage. The completed MOS diode showed the n-type feature. The *C–V* and *C–f* characteristics of the MOS diode indicated that shallow surface Fermi level pinning and deep depletion occurred simultaneously. By applying the conductance method to the measured *C–f* characteristics, a discrete level at 0.2–0.3 eV below E_C was detected. On the basis of the simulation of the high-frequency-limit *C–V* curve, the detected discrete level was found to be acceptorlike and distributed in the bulk of n-GaN rather than at the insulator/semiconductor interface, so it simultaneously caused surface Fermi level pinning at a relatively shallow energy level and deep depletion.

Acknowledgments

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Figure Captions

Fig. 1. (a) Sequence of sample preparation. (b) TRIM simulation results for concentration of Mg, V_{Ga}, and V_N. (c) Sample structure.

Fig. 2. Measured high-frequency *C–V* and G/ω–*V* characteristics of the MOS diode with Mg-ion-implanted GaN.

Fig. 3. Measured *C–f* and G/ω–*f* characteristics of the MOS diode with Mg-ion-implanted GaN.

Fig. 4. (a) Measured G_p/ω–*V* characteristics. (b) Measured D_{it} distribution.

Fig. 5. Simulation result for *C–V* characteristics of the MOS diode with Mg-ion-implanted GaN assuming that the measured D_{it} distribution resulted from interface states (inset).

Fig. 6. Bulk defect level profiles assumed in the simulation.

Fig. 7. Simulation result for *C–V* characteristics of the MOS diode with Mg-ion-implanted GaN assuming an acceptor level at E_C – 0.27 eV and a donor level at E_C – 0.07 eV having density profiles shown in Fig. 6.

Fig. 8. Simulation result for band bending of Mg-ion-implanted GaN in a MOS structure assuming an acceptor level at E_C – 0.27 eV and a donor level at E_C – 0.07 eV having density profiles shown in Fig. 7. (a) V = -5 V, (b) V = 0 V, (c) V = 5 V, and (d) V = 10 V.

Fig. 9. Simulation result for *C–V* characteristics of the MOS diode with Mg-ion-implanted GaN assuming only a donor level at E_C – 0.27 eV having density profiles shown in Fig. 6.

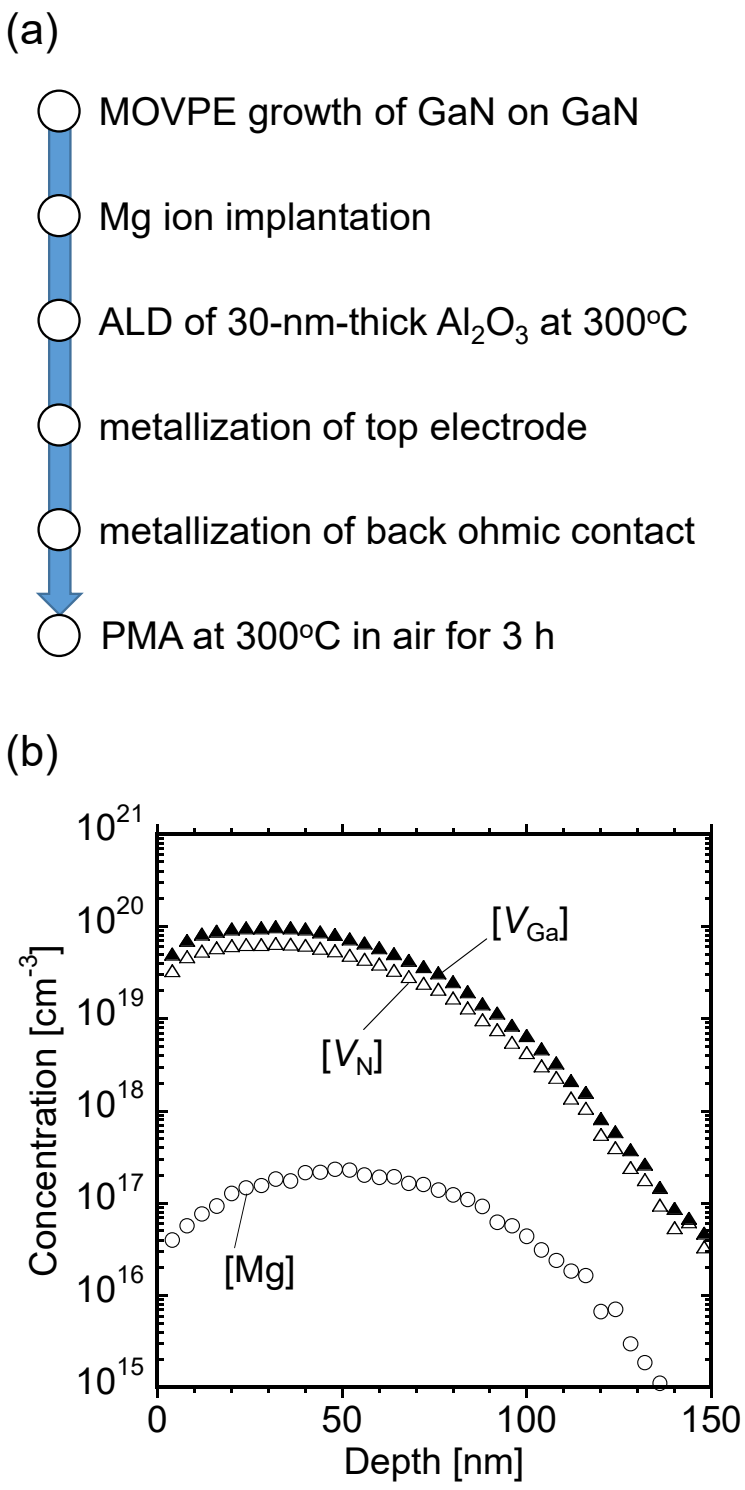

(a)
MOVPE growth of GaN on GaN
Mg ion implantation
ALD of 30-nm-thick Al_2O_3 at 300°C
metallization of top electrode
metallization of back ohmic contact
PMA at 300°C in air for 3 h
(b)
Concentration [cm^{-3}]
10^{21}
10^{20}
10^{19}
10^{18}
10^{17}
10^{16}
10^{15}
[V_{Ga}]
[V_N]
[Mg]
0
50
100
150
Depth [nm]

Fig.1.

(c)

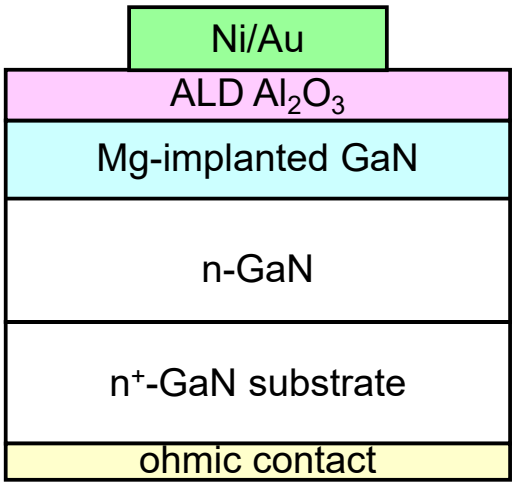
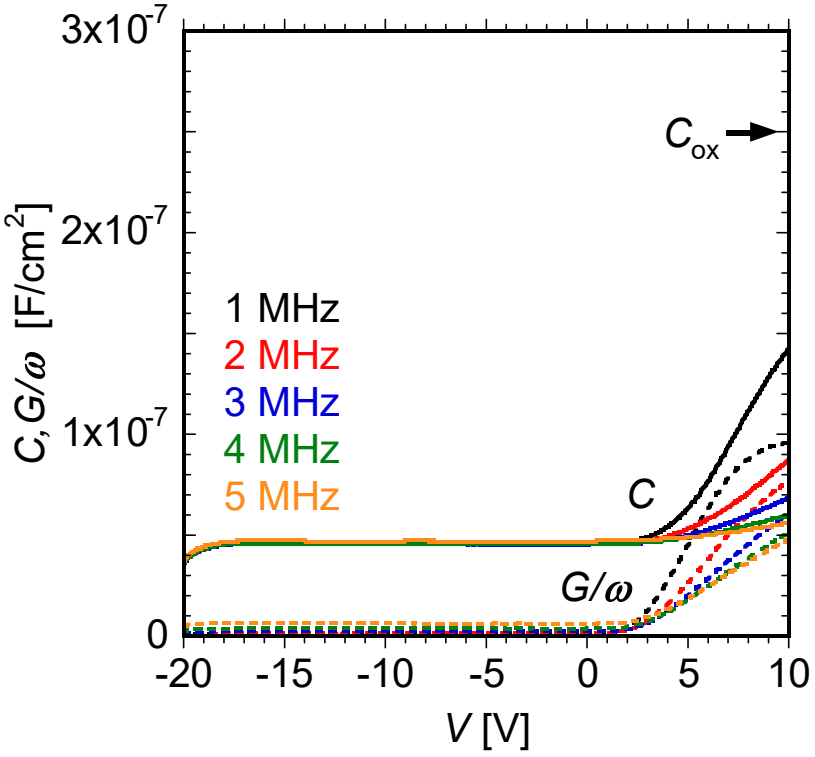

Ni/Au
ALD Al_2O_3
Mg-implanted GaN
n-GaN
n^+-GaN substrate
ohmic contact

Fig. 1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2x10-7
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Cox
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G/ω
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-5
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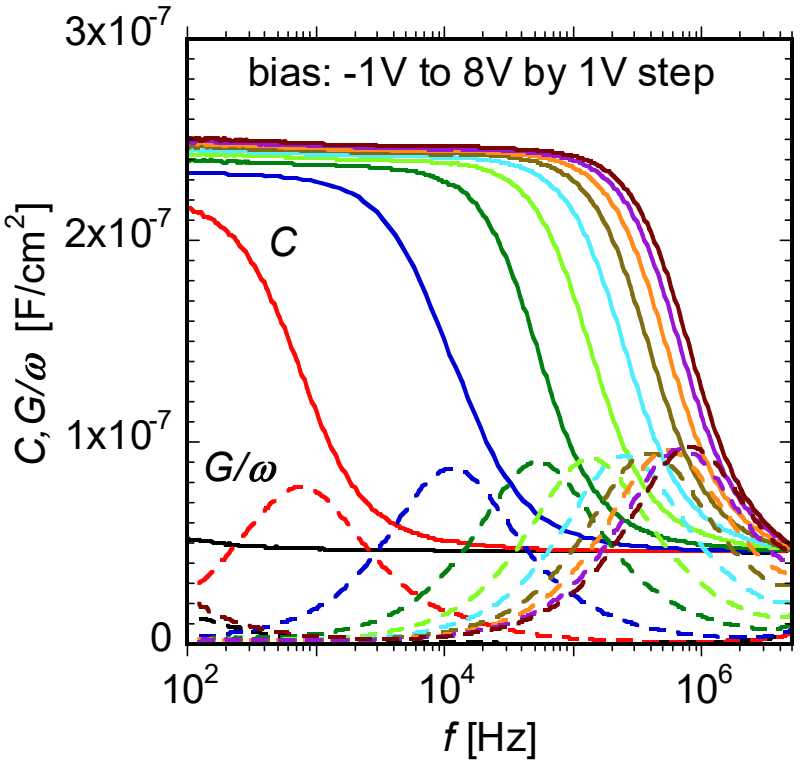
5
10
V [V]

Fig. 2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10^4
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f [Hz]

Fig. 3

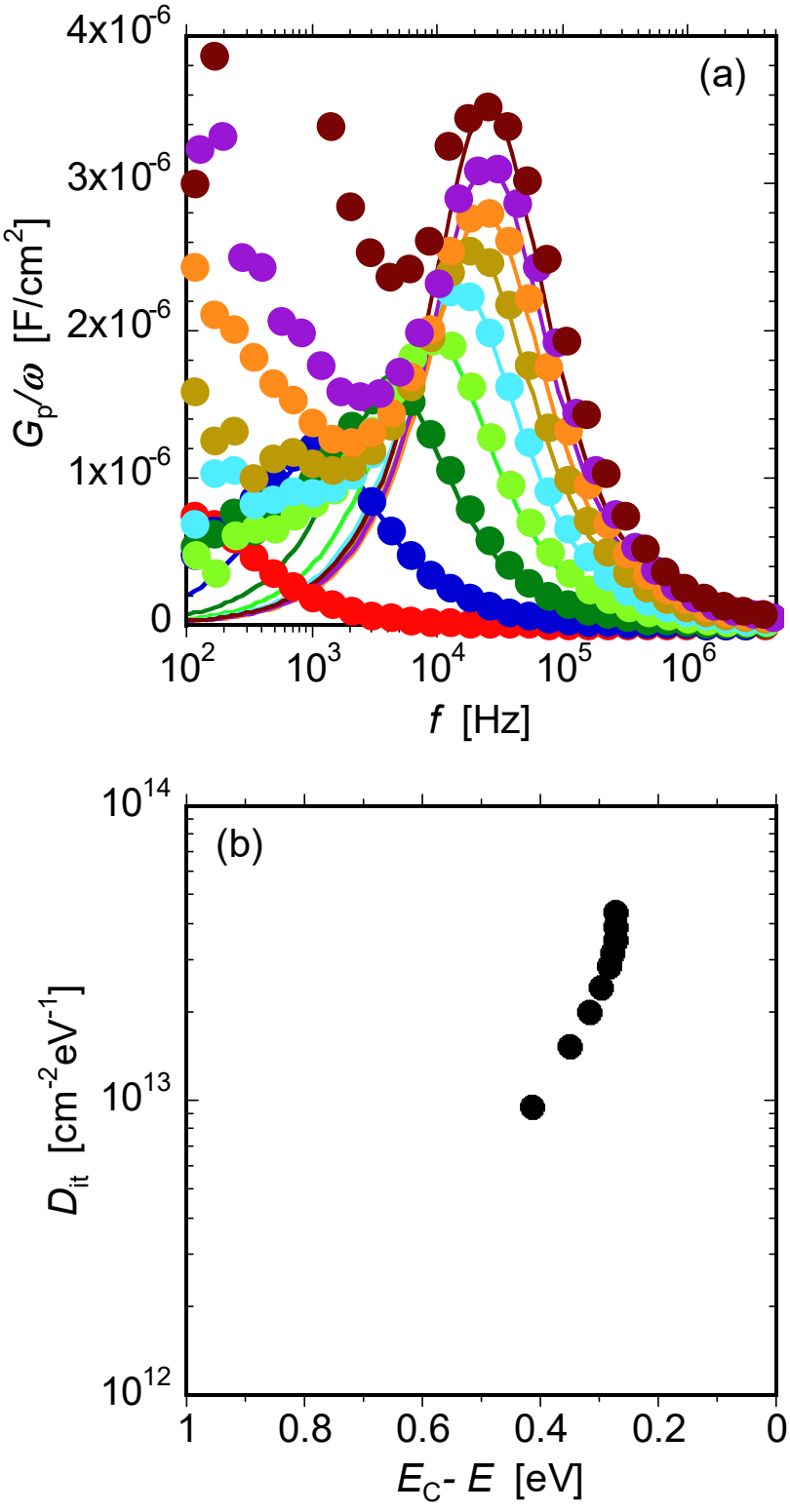
(a)
4x10-6
3x10-6
2x10-6
1x10-6
0
Gp/ω [F/cm2]
10^2
10^3
10^4
10^5
10^6
f [Hz]
(b)
10^14
10^13
10^12
Dit [cm-2eV-1]
1
0.8
0.6
0.4
0.2
0
EC- E [eV]

Fig. 4

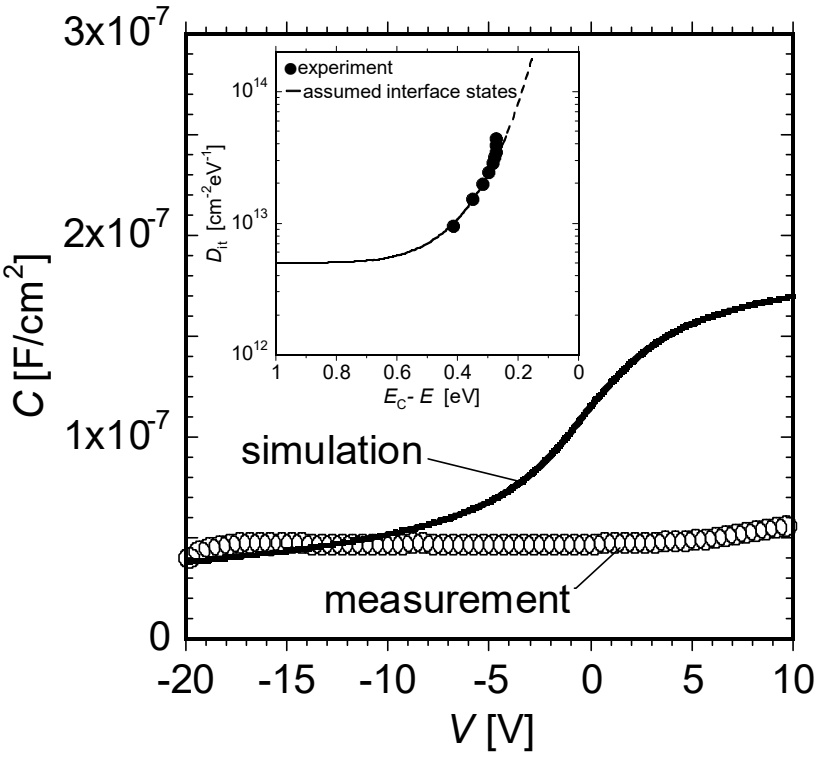
3x10-7
2x10-7
1x10-7
0
C [F/cm2]
-20
-15
-10
-5
0
5
10
V [V]
simulation
measurement
experiment
assumed interface states
10^14
10^13
10^12
Dit [cm-2eV-1]
1
0.8
0.6
0.4
0.2
0
EC- E [eV]

Fig. 5

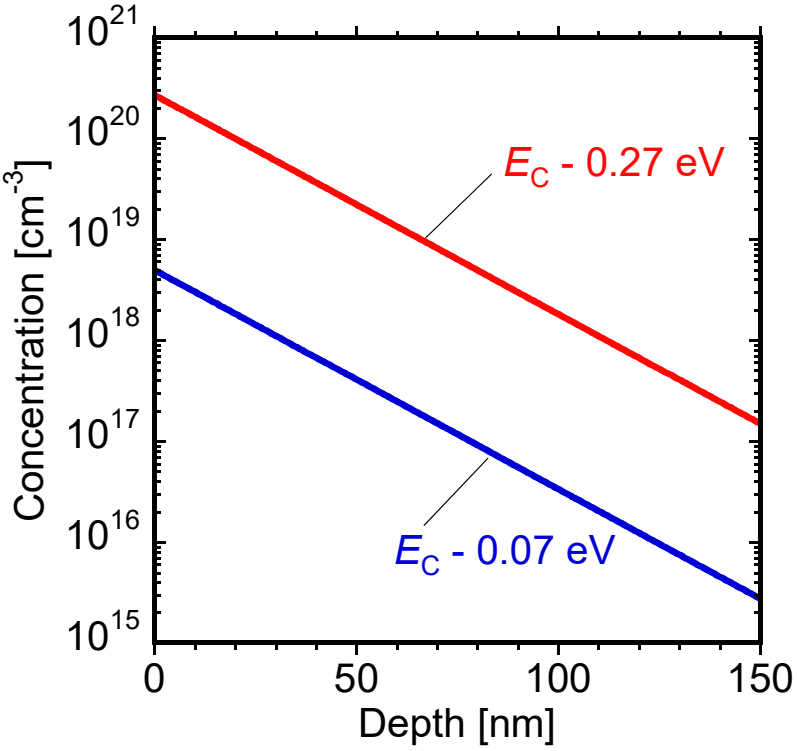
10^21
10^20
10^19
10^18
10^17
10^16
10^15
Concentration [cm-3]
0
50
100
150
Depth [nm]
EC - 0.27 eV
EC - 0.07 eV

Fig. 6

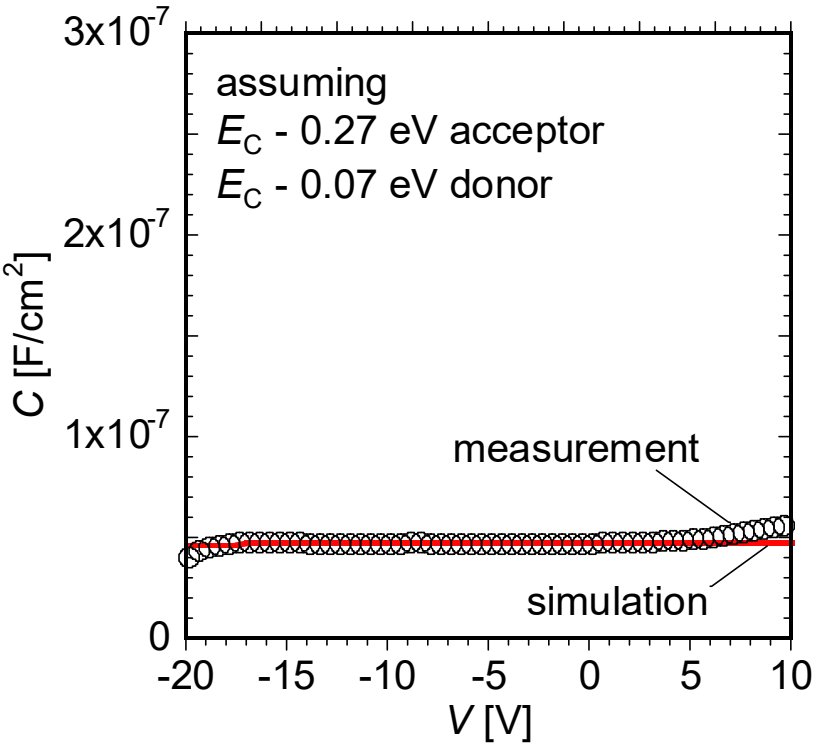
3x10-7
2x10-7
1x10-7
0
C [F/cm2]
assuming
EC - 0.27 eV acceptor
EC - 0.07 eV donor
measurement
simulation
-20
-15
-10
-5
0
5
10
V [V]

Fig. 7

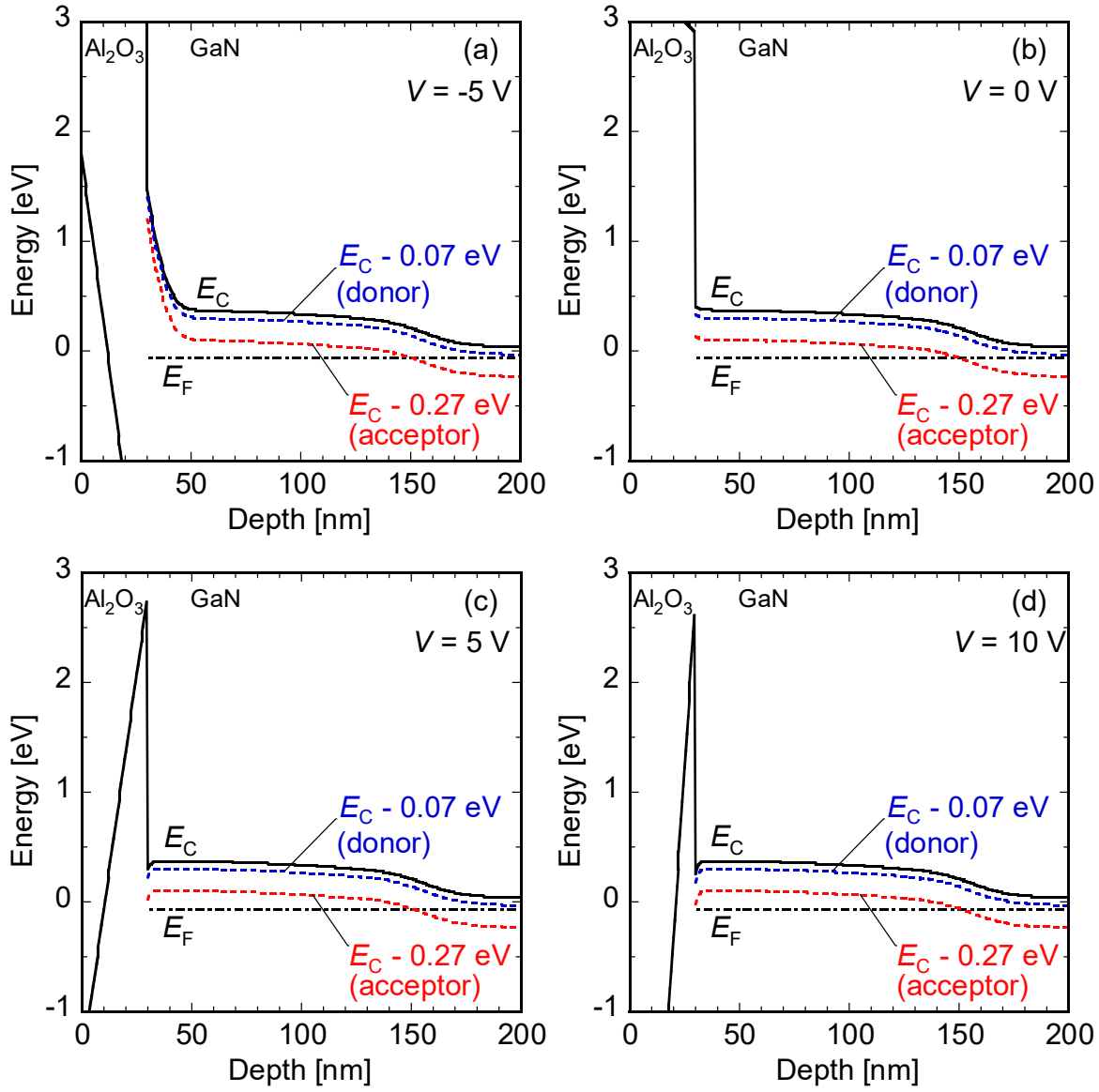
Al2O3
GaN
(a)
V = -5 V
(b)
V = 0 V
(c)
V = 5 V
(d)
V = 10 V
EC - 0.07 eV
(donor)
EC - 0.27 eV
(acceptor)
EC
EF
Energy [eV]
Depth [nm]
3
2
1
0
-1
0
50
100
150
200

Fig. 8

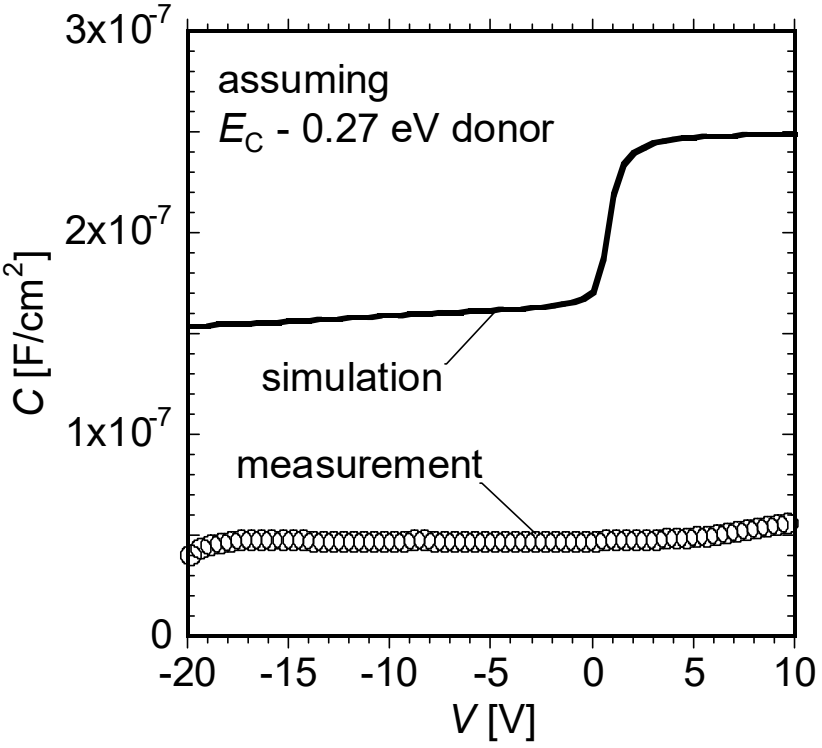
3x10-7
2x10-7
1x10-7
0
C [F/cm2]
assuming
EC - 0.27 eV donor
simulation
measurement
-20
-15
-10
-5
0
5
10
V [V]

Fig. 9