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Study on tantalum oxide resistive memory operation using different nano-material compositions

異なるナノ材料で構成したタンタル酸化物抵抗変化メモリの
動作特性に関する研究

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Abstract

Recently, the application of artificial neural networks (ANN) has shown the potential to improve the efficiency of information processing in various fields while the scaling of transistors that determine the speed of current computer performance has reached its limit, and the improvement of ANN performance is limited. To further improve the performance (universality), it is necessary to develop a new ultra-miniaturized memory element that can store analog values to create a device, which makes it possible to integrate more neurons (perceptron) and synapses (weight). One important candidate, the resistive memory, has a simple structure of metal/insulator/metal, is easy to manufacture, and is advantageous for scaling. By applying a positive (set) or negative voltage (reset) from the outside, a reversible change in conductivity occurs in the device. However, the evaluation of systematic characteristics is lacking because the mechanism of non-volatile resistive switching operation is still obscure. Therefore, in this research, we explored the operating principle of resistance change memory with the goal of realizing the characteristics of artificial synapses required by ANN.

First, the results of this research will be described from the viewpoint of electrical characteristics. Previous studies have shown complex resistive switching characteristics of binary or multi-value(analog), and it is difficult to make a unified and systematic comparison of the reported characteristics due to the usages of different material and fabrication methods. In this research, tantalum oxide, which is known as a relatively stable material, is selected as a switching material, and the goal is not only to realize multi-valued analog operation, but also to evaluate the relations between the initial state (state immediately after device fabrication) and switch characteristics of the device systematically. In the initial state, the difference in cross-sectional state was investigated by transmission electron microscopy (TEM) and element mapping experiments, and the oxidizing action of the electrodes was discovered. After that, the switching characteristics of the device differed greatly depending on the fabrication conditions, and it was found that the fabrication conditions including the electrode configuration are important for realizing stable multi-valued analog operation. Based on these results, we were able to realize spike timing-dependent plasticity (STDP) characteristics such as biological synapses.

From the result, it was found that the viewpoint of material physical properties is important. It was widely presumed that the resistance change due to voltage application is caused by the formation and breakage of the conductive filament. Depending on the electrode used, the filaments were formed by

the generation of oxygen defects in the insulating film (VCM model) or by the precipitation of the metal introduced by ionization from the electrode (ECM model). In this study, to compare the difference between the two models, a scavenging metal (Ta, Ti, Al) or an active metal (Cu) that easily ionizes was used as the top electrode. Furthermore, the concentration of initial oxygen defects contained in the tantalum oxide insulator was controlled. It is clarified that the fabrication conditions controlled in these two steps determine the initial state. The gradient of oxygen concentration and metal ion concentration near the electrode interface that affected the subsequent switching characteristics.

The outline of each chapter is presented.

In Chapter 1, reviews the history of resistive memory, including its application to ANN, and recent accomplishments are reviewed.

In Chapter 2, the purpose, significance, and the flow of this research are described.

Chapter 3 summarizes the methods used in this study. First, important processes and related equipment in device fabrication are described, and electrical characteristics and TEM evaluation methods are introduced. The results of the research are divided into three parts and described in the following three chapters.

In Chapter 4, we focused on the initial state of the device. The initial resistance and the forming characteristics were firstly investigated in detail. Then the devices were evaluated by TEM and EDX element mapping. As device fabrication conditions, the initial oxygen defect concentration of the tantalum oxide film and top electrode and were changed. Ta, Ti, Al and TiN electrodes were selected and evaluated as typical scavenging metals. The difference of initial resistance of more than 5 orders was observed. These results revealed that the oxygen vacancy distribution in the tantalum oxide film is changed significantly by the electrode and the initial oxygen vacancy concentration. This means that the scavenging effect of the electrode works greatly. In addition, it was found that the forming characteristics show unique features that depend on the chemical properties of the electrode material, and it is not uniquely determined by the ease of forming oxides that have been said so far.

In Chapter 5, devices were patterned by lithography and dry etching. The relationship between the initial characteristics, analog operation, and the manufacturing conditions was evaluated. The device materials were the same as in the previous chapter, and a Cu electrode was added as a typical ECM electrode. First, after comparing the initial states of the VCM model with the Ta as the top electrode and the ECM model with the Cu top electrode, it was found that the initial oxygen vacancy

concentration of the tantalum oxide film greatly affects not only the VCM but also the ECM. Regarding to the analog operation, the Ta top electrode became less dependent on the fabrication conditions, while the ECM device with the Cu electrode maintained the uniqueness of the fabrication conditions. This must be due to the VCM switching scenario influenced by the scavenging phenomenon during operation, whereas the EMC operation is caused by electrochemical reaction depending on the preparation condition. In addition, different analog operating characteristics were shown in devices using Ta, Cu, Ti, and Al electrodes. Based on these results, we compared the applicability to ANN, examined the strengths and weaknesses of each electrode, and concluded that Ta/Ta₂O₅ was the most appropriate.

Chapter 6 aimed to improve analog operation based on the results obtained in the previous chapter. An ultra-thin SiO₂ layer was inserted between the bottom electrode and Ta₂O₅ to optimize the current flow during forming and switching operation. As a result, we succeeded in obtaining a gradual resistance change at both sides of set and reset, and so the stable analog operation was realized. Furthermore, it was shown that the operating characteristics can be controlled by systematically changing the current limit (I_{comp}) on the set side and the voltage limit ($-V_{\text{max}}$) on the reset side. In other words, the two parameters, I_{comp} and $-V_{\text{max}}$, determine the strength of filament formation and destruction, respectively. The stable window for analog operations can be realized for set and reset by the optimized parameters. Because of these optimizations, it was found that highly reproducible analog operation can be realized and STDP characteristics simulating biological synapses were possible. Discussions about the changes in filament during operation based on the findings were presented.

Chapter 7 summarized the contents of this research.

学位論文の要旨

近年、人工ニューラルネットワーク(ANN)の応用はさまざまな分野において情報処理の効率を改善する可能性を示している。しかし、現在のコンピュータの性能を律速するトランジスタの微細化が限界に達し、ANN の性能向上が制限されている。さらに性能（汎用性）を上げるために、より多くのニューロン(perceptron)とシナプス(weight)を集積したデバイスの創出が必要になっているが、このときアナログ値を記憶できる超微細化可能な新型メモリ素子の開発が不可欠である。一つの重要な候補である抵抗変化メモリは、金属・絶縁体・金属のシンプルな構造を有し、作製が簡単で微細化に有利である。外部から正(set)、または負電圧(reset)を印加することで、素子に可逆的な導電率の変化が生じる。しかし、不揮発的な抵抗スイッチ動作のメカニズムには不明な点も多く、特性の評価に系統性が欠けている現状にある。そこで、本研究では、ANN に必要となる人工シナプスの特性の実現を目標とし、抵抗変化メモリの動作とデバイス構造との相関について詳細に検討した。

まず、電気特性の視点から本研究の成果を述べる。先行研究では、二値または多値(multi-value/analog)の複雑な抵抗スイッチング特性を示す上に、材料や作製方法が異なるため、報告された電気特性の統一的・客観的比較が困難である。本研究では、比較的安定な材料として知られる Ta 酸化物をスイッチング材料として選定し、多値・アナログ動作の実現することだけを目指とするのではなく、初期状態（デバイス作製直後の状態）の評価から始まり、続いてデバイスのスイッチ特性との関連も系統的に調べることとした。初期状態では、透過電子顕微鏡(TEM)および元素マッピング実験によって断面の状態の違いを調べ、電極の酸化作用についての知見を得た。その後のデバイスのスイッチング特性は作製条件によって大きく異なり、安定な多値・アナログ動作を実現するためには、電極構成を含めた作製条件の最適化が重要であることが分かった。これらの結果を踏まえて、生物シナプスのようなスパイクタイミング依存可塑性(STDP)特性を実現できた。

上記の検討より、材料物性の視点が重要であると言える。これに関する本研究の成果を述べる。電圧印加による抵抗変化は導電フィラメントの形成と破断によるものと推測され、使う電極によって、絶縁膜中の酸素欠陥生成によるフィラメント (VCM)、あるいは、電極がイオン化して導入される金属の析出によるフィラメント(ECM)が報告されている。本研究では、二種類のモデルの違いを比較するために、VCMを誘起する scavenging 金属(Ta, Ti, Al)、またはイオン化しやすい active 金属(Cu)を上部電極として使用した。さらに、Ta 酸化物絶縁体に含まれている初期酸素欠陥の濃度を制御した。この二段階に制御した作製条件が初期状態を決定し、電極界面付近の酸素濃度の勾配が変わる、あるいは金属イオン濃度の勾配が変化することで、その後のスイッチング特性に影響を与えることを明らかにした。

次に各章の概要を述べる。

第 1 章では抵抗変化メモリの歴史、ANN への応用の経緯および近年の研究をレビューする。

第 2 章では本研究の目的、意義および流れを述べる。

第 3 章では本研究で使用した手法をまとめている。まずは全体として、デバイスの作製において、重要なプロセスおよび関連する装置について述べ、電気特性および TEM の評価方法を紹介する。

本研究の成果を三つの部分に分け、以下の三章で述べる。

第 4 章ではデバイスの初期状態に着目し、初期抵抗の測定、最初の抵抗スイッチである forming 特性を評価すると共に、TEM 観察および元素マッピングによる評価を行った。デバイスの作製条件として、上

部電極および Ta 酸化膜の初期酸素欠陥濃度を変化させ、典型的な scavenging 金属の Ta、Ti、Al と TiN 電極を選んで評価し、5 桁以上の初期抵抗の違いを示した。これらの結果は、Ta 酸化膜中の酸素欠陥分布が、電極や初期酸素欠陥濃度で大きく変わるために生じることを明らかにした。すなわち、電極の scavenging 効果が大きく働いていることを示す。また、forming 特性に関しては、電極材料の化学的性質に依存した独特の特性を示すことが判明し、これまで言われている酸化物の形成されやすさなどで一義的に決まるわけではないことを示した。

第 5 章ではリソグラフィーとドライエッチングにより微細化したデバイスで、初期特性、アナログ動作、およびその作製条件（初期酸素欠陥濃度、膜厚及び電極の種類）との関連について評価した。デバイス材料は前章と同じとし、典型的な ECM 電極として Cu 電極を追加した。まず、Ta を上部電極とした VCM と Cu を上部電極とした ECM の初期状態を比較した結果、Ta 酸化膜の初期酸素欠陥濃度が、VCM のみならず ECM の初期特性にも大きく影響することを見出した。また、アナログ動作に関しては、Ta 上部電極の VCM デバイスでは作製条件への依存性が小さく、Cu 上部電極の ECM デバイスでは作製条件に固有性を示した。これは、Ta 電極においてはスイッチング時に主に scavenging 効果が作用することに対し、Cu 電極では作製条件に依存した電気化学的な反応が作用すると考えられる。また、Ta、Cu、Ti、Al 電極を用いたデバイスにおいてそれぞれ違った多値動作特性を示した。これらの結果を基に ANN への応用性を比較し、各電極の有利/不利な点を精査し、Ta/Ta₂O₅ が一番適切な構造であるとの結論に至った。

第 6 章では前章で得られた結果をベースにして多値・アナログ動作の改善を目標とする。そのための方策として極薄 SiO₂ 層を下部電極と Ta₂O₅ の間に挿入し、forming 時の電流制限、つまりスイッチングのパワーの最適化を試みた。結果として、set 時、reset 時の双方において緩やかな抵抗変化を得ることに成功し、安定なアナログ動作を実現できた。さらに、set 側の電流制限(I_{comp})および reset 側の電圧制限($-V_{\text{max}}$)を系統的に変化させることで、動作特性を制御できることを示した。すなわち、 I_{comp} と $-V_{\text{max}}$ の二つのパラメータがフィラメント形成と破断の強弱をそれぞれ決め、set と reset に安定なアナログ抵抗変化ウィンドウを実現できる。これらを最適化することで、再現性の高いアナログ動作を実現でき、生物シナプスを模擬した STDP 特性を実現できることが分かった。また、各章において得られた知見に基づいて、動作時の filament の変化を討論する。

第 7 章では、本研究の内容をまとめる。

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Chapter 1 A brief history of resistive memory

Resistive switching phenomenon in capacitor-like nanostructures has been discovered for over 70 years. The controllable nonvolatile switching behaviors were thought to be a good replacement for the traditional memory for the low power consumption, high speed, and good scalability for the chip integration. Because of the urgent requirements on building artificial neural network physically, the advantages have been redrawing attentions. In neuromorphic computing, algorithms like backpropagation and gradient descent require huge amount of matrix calculations. Although people have been successfully realized learning capabilities on machines, sometimes the performance even surpasses humans, the extremely high consumption is needed for the performance. Comparing to the consumption about 20 watts of human brains, a supercomputer can consume 1000 kWh to maintain the functionality. To overcome the traditional von Neumann bottleneck, in-memory computing was proposed. Artificial neurons and synapses, based on transistors, are linked directly to gain power efficiency. Promising results were acquired such as self-driving car or natural language processing using specially designed neuromorphic chips. To increase the universality to more complex tasks, people have been increasing the number of neurons and layers, which causes the number of the synapse unit to increase quadratically. As a result, more transistors are needed and so the more space on the chip. And by the thermo limitations, the area of chip cannot be increased infinitely. To solve the problem, a resistive memory can surely be a candidate because of its excellent physical properties.

Recently, resistive memories are considered essential elements for constructing neuromorphic hardware chips because of the analog behaviors and simple metal-insulator-metal structures. Still, because the underlying mechanisms are not fully understood yet, control of the resistance remains a significant challenge in terms of bringing the technology into a practical stage. Because of its simple fabrication process, various transition metal oxides have been investigated to test the capability. In addition, the proposed filamentary model as the operation model were experimentally checked by means of transmission electron microscopy and other techniques. It also has been reported that the switching behaviors can be different because of the selected nanomaterial. Both binary and analog (multiple resistance states) switching behaviors had been achieved, where analog behaviors are considered essential for neuromorphic computing.

Researchers also used pulses generators to feed biological signals to the memory and the spike-timing-dependent plasticity was successfully realized, which was a concept that being used to explain synapse plasticity in neuroscience.

In this chapter, in respect to the motivation of this work, important works relating to the resistive memory are reviewed.

1.1.Pioneering studies of the resistive memory

A permanent nonlinear resistance change that occurs on a simple two-terminal capacitor-like device by applying voltage externally was discovered in the 60s. Hickmott (1962) discovered the thin film capacitor's resistances can be controlled for SiO and Al₂O₃ oxides by current-voltage measurement or pulse applications [1]. Some novel applications of the device were also proposed such as applied as switches or in memory arrays. Simmons (1967) suggested that the negative resistance region can be differentiated by changing the threshold voltage [2]. This should be the first hint of realizing the analog switching. As shown in figure 1-1, different resistance states can be differentiated by using different threshold voltage at point A~E.

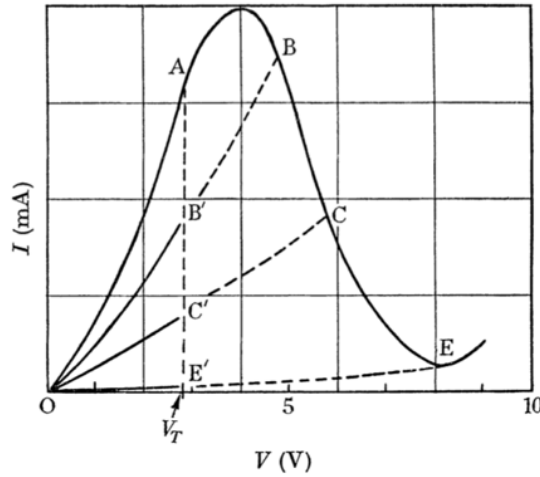


Figure 1-1. Differentiating the characteristics to obtain memory proposed by Simmons (1967).

A lot of studies about the device physics were reported about the negative resistance in the late 1900s. Detailed analyses of charge transport mechanisms, impurities, conduction band of different materials were given [3-13]. Taking advantages of high-resolution microscopes, first looks on the switching devices are also reported as shown in figure 1-2 [14-17].

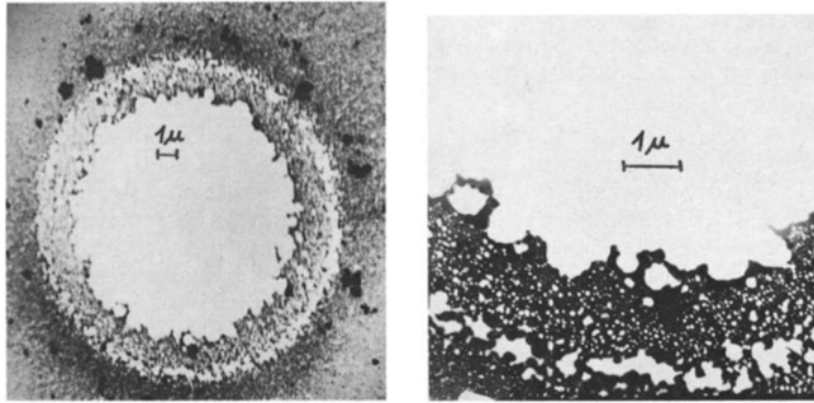


Figure 1-2. Electron micrographs of the upper Au electrode stripped off by electroforming by Emmer (1974).

Chua (1971) proposed that there should be a fourth basic circuit element base on the missing relation between charge and flux, $d\phi = Mdq$. He successfully synthesized the conceptual device using complicated analog circuits with external power supply to fulfill its functionality. He named the conceptual device a '*memristor*'. At that time, the memory device had not yet been associated to Chua's memristor circuit [18].

By entering the new millennium, the two-terminal devices had been redrawing attentions because of its capabilities of storing information like a computer memory. Unlike traditional RAM used on the personal computers, these novel memory devices did not require extra power to maintain the data existence and data fidelity (non-volatility). Besides, they also perform much faster than other nonvolatile memories such as flash memory. The metal-oxide-metal structure is also simple enough to scale down for the higher circuit integration. So, the device was considered a candidate of replacing the traditional RAM and such device was accepted as a '*memory*', and because of the possible application, '*ReRAM*' or 'RRAM' (short for resistive random-access memory) was often used [19-24]. Figure 1-3 shows an example of crossbar memories.

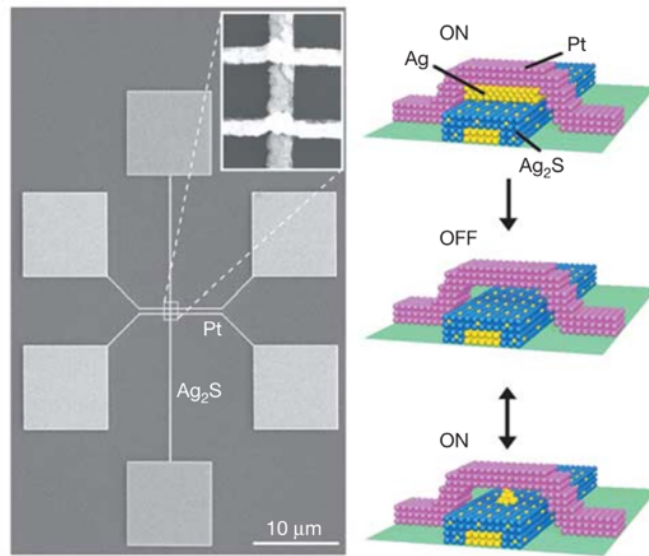


Figure 1-3. Crossbar memory devices fabricated by Terabe (2005).

Later, Strukov (2008) and his colleagues provided a model of the two-terminal device that has perfect memristive behavior. The similar behaviors had been discovered in other nano-structured two-terminal device can be considered memristive behaviors [25].

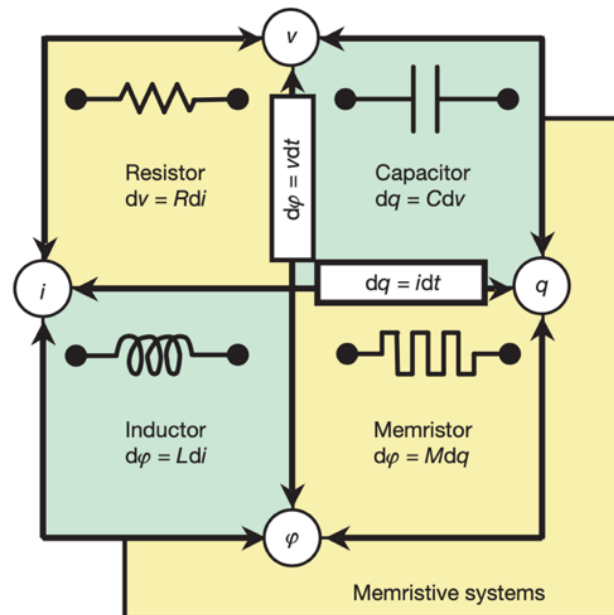


Figure 1-4. The two-terminal circuit element diagram shown in Strukov (2008).

1.2.Entering the era of neuromorphic computing

1.2.1.*Brain-inspired concepts*

The pursuit to the artificial intelligence (AI) has never been stopped by human. Starting with the automation that increases the efficiency, human-like learning capabilities are being perfected on computers recently. Like the technologies mimicking bio-systems, such as planes or cameras, researchers are also trying to draw inspirations from the living creatures [26]. Starting from the simplest neural systems of *C. elegans* (it has 302 neurons), it was fully understood that how they react to the external world [27]. Nowadays more complex mammal brains (a human can have 100 billion neurons) are being studied using modern technologies [28-32]. The synapse constantly changes, because of the information brain absorbs, to accomplish tasks such as surviving the nature.

Hebbian theory offered a possible explanation that how the synapse plasticity relates to the learning capability [33-35]. Signals transferred between two neurons by passing neurotransmitter with synapse [36]. The efficiency of the signal transmission is due to the state of synapse. Signal passes efficiently if the synapse intensity is high and vice versa. To give a definitive description of this phenomenon, spike-timing-dependent plasticity was proposed that the time delay between the two neurons firing will change the synapse intensity. Many experiments were conducted to confirm the validity [37-40]. The relation between Δt and the F is shown in figure 1-5, which is the percentage of the maximum synaptic conductance [37].

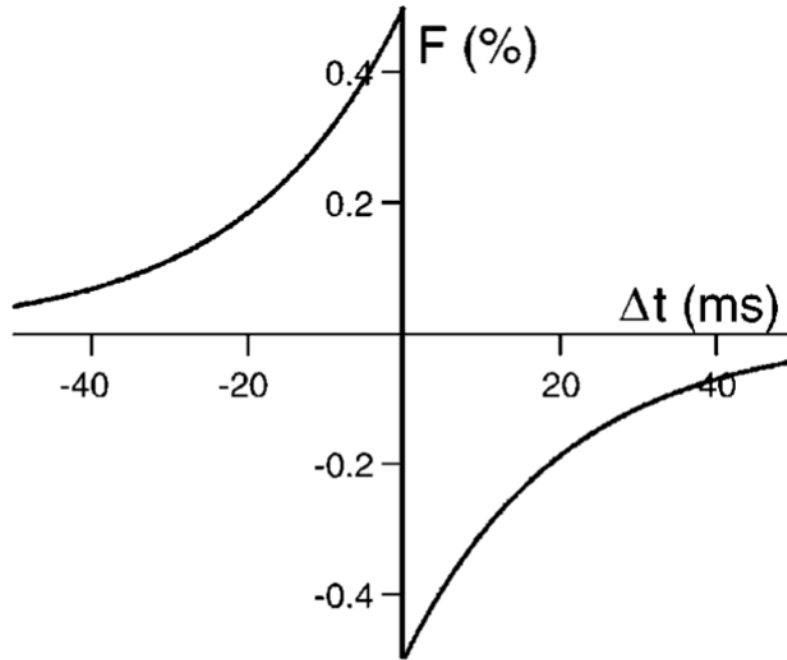


Figure 1-5. The STDP modification function, where Δt is the time delay of pre- and post-synapse neurons. Synaptic conductance is given by $g_{\max}F(\Delta t)$, where g_{\max} is the maximum synaptic conductance.

1.2.2. Neuromorphic computing

Advancing neuroscience gave researchers a new approach of realizing AI that is to construct a machine-performable artificial neural network (ANN) [41-44]. Analogous to biological neural networks, ANN also has neurons and synapses but in abstract senses. Like biological neurons, artificial neurons fire according to the activation functions and the neuron state changes because of the inputs. On the other hand, controllable weights are used to connect the neurons functioning as artificial synapses. As shown in figure 1-6, a recent network often has more layers than traditional perceptron-based signal layered network. Multi-layered networks give the system more capability to fit more complicated hidden multidimensional functions.

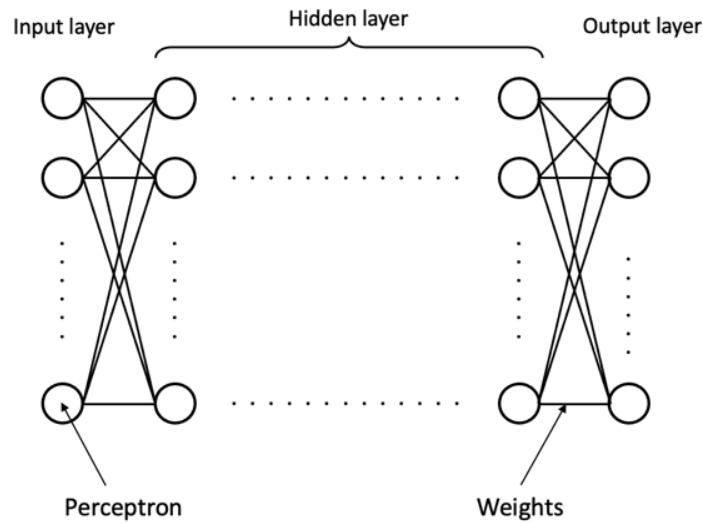


Figure 1-6. Schematic illustration of a multi-layered perceptron-based network. The number of weights is much larger than perceptron.

Algorithms like backpropagation and gradient descent used in ANN can be mathematically solved since the calculation is mainly matrix operation. The calculations were previously performed by the central processing units (CPUs) since their good universality. To increase the calculation efficiency and increase the scale of the network, graphic processing units (GPUs) are being wildly used to train models nowadays.

Well configured network can solve simple and complex problems like classification or prediction. The ANN with deep networks increased the features that the networks can handle aside from simple linear classification problems. Now, trained networks can fit any complicated functions and predictions have high confidence even capable to a commercial level. The recently reported accomplishments freed human from ground repeated works with less human error such as medical diagnosis, self-driving or financing. A well-trained network can even beat human on an intellectual game [44].

The demand of computing increases rapidly from the year of 2012, and according to *OPENAI*, the demand doubles every 3.5 months [45]. The increasing layers also increase the number of neurons proportionally and synapses quadratically. Nowadays, the fabrication of semiconductor has been reaching the limit of the Moore's law. So other approaches are needed for the further improvement of the ANN. One approach is that instead of traditional von Neumann architecture, we use a new computer architecture that overcomes the processor-memory bottleneck. Similar

to the biological brains, memories (synapses) are connected to the processors (neuron) directly. Every processor can reach respective memories directly. In fact, the mechanism of perceptron in neural networks is a linear multiplication of the weight (a scalar) and the states of perceptron (a vector). The 'in-memory' computing fits the requirement of ANN perfectly. Apart from using a cluster of DRAMs to represent a weight, every single intersection could be fully functional. The very-small area taken by each memory increases the integration of the chip, and more functionalities could be integrated on a single chip.

Despite the model of ANN is still being discussed for the future implementation, the physical properties of resistive memory indicated its profound possibility of fulfilling all the requirements. Both biological and mathematical approaches of neural network showed the natural characteristic of analog behaviors. Biological neuron fires signal to the next neuron crossing the bridge of synapse, and the efficiency of the information transmissions is strongly depended on the synapse intensity. Mathematical perceptron changes its states because of the multiplication to the weight (continuous values between -1 and 1 in deep learning). Instead of the absolute binary values of "1" and "0", the information processing in the ANN should be performed analogously. Analog signals and values are difficult to present in the digital computers because of its binary fundamental. To realize one neuron or memory cell, usually hundreds of transistors are needed. On the other hand, resistive memory has great scalability because of its simple capacitive structure. In fact, P. Yao (2020) and his colleagues successfully integrated 2048 synapse as memory arrays and the prototype had received good performance [46].

Models such as deep learning use mainly mathematics, and less bio-mimicking aspects are applied. Recent works with more biological concepts integrated also shows profound accomplishments [46-51]. Spiking neural network (SNN) is one of the pioneer models. Instead of backpropagating on each cycle, artificial neurons only fires at the moment that the inputs satisfy the internal activation function. The firing signal changes the states of synapse that influences other neurons. The concept of STDP can be integrated to the model. By the different amount of time lags from pre- and post-neuron, the intensity of the synapse changes analogously. Although the inconstant behavior of SNN is similar to the biological brain, it consumes more on

a traditional computer because of the more complex mechanism. To realize the model efficiently, artificial-neuron-based hardware is needed.

1.3.Recent resistive memory studies

Resistive memory has been widely accepted to be the strongest possibly to realize the artificial synapse in ANN. However, there still are unclear aspects that needed to be studied. In this section, the important aspects regarding to the field will be reviewed and discussed.

1.3.1.Material selections and possible models

Various transition metal oxide films were used as insulators, and the corresponding switching behaviors have been extensively explored, such as AlO_x , TiO_x , TaO_x , NiO_x , etc. [52, 53]. Although the switching capability can be easily realized, the characteristics with different material combinations are distinguishable. The control of the resistance remains a significant challenge to bring the technology to higher practical level. While many combinations have been tried on other studies, it has been accepted that the resistance changes are the consequence of the formation and rupture of conductive filaments in the insulator layer [54-56]. In the recent reports, two models have been proposed, valence change memory (VCM) and electrochemical memory (ECM), categorized by the different type of conductive filaments. VCM is based on the movements and assembly of oxygen vacancies to form the metallic conductive filament, and scavenging metals are usually used as electrodes to create different environments concerning oxygen vacancies. ECM uses active metal electrode, such as copper (Cu) or silver (Ag), and the conductive filaments were formed by the metal ion movement from the active electrode. Successful observations of conductive filaments have been reported for both models [57-63].

1.3.2. Analog switching

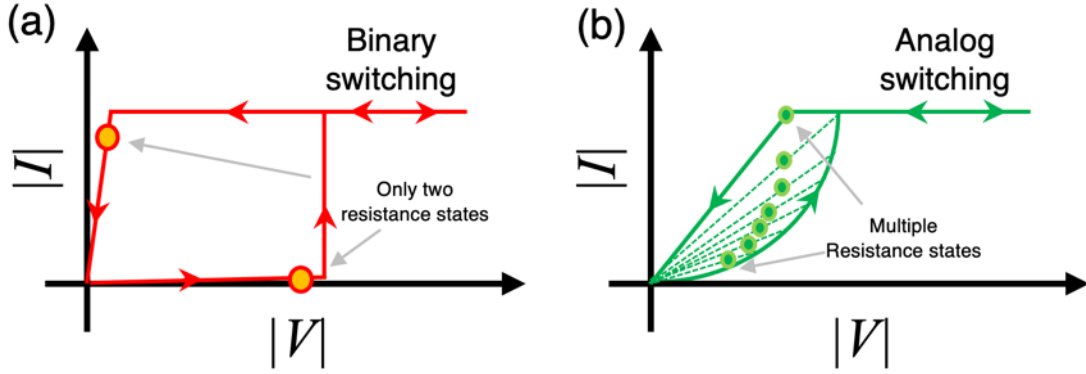


Figure 1-7. The schematic illustrations of binary switching and analog switching.

As reviewed in Sec. 1.2, synaptic analog behavior is considered essential to realize the ANN hardware. That is, with specific input forms, gradual resistance change was achieved in several different MIM-structure-based resistive memories. As shown in figure 1-7, schematic characteristics are given. Both graphs are representing the voltage sweep characteristics (semi-static measurements), which is the measurement method that will be introduced in Chapter 3. In figure 1-7(a), with the higher voltage applying to the device, the high resistive states switch rapidly, and a current limit is arrived. Then at the finish of the sweep, the low resistive states rapidly switch to the low resistive state reaching the current limit set by the current source. So, the medium states do not exist because of such the rapid avalanche-like breakdown. On the other hand, figure 1-7(b) shows an example without a rapid current jump. The switching current is gentle so that the medium resistance states can be stored by adjusting the threshold of the voltage. This multi-level resistance states are usable for analog memory operation. Recently, because of the rapidly increasing demand on the artificial neural network, the realization of the analog switching capabilities has become an important issue having a priority to be developed.

1.3.3. Oxygen-vacancy based switching

In the VCM model, oxygen vacancy is considered majority component to form a conductive filament, and the insulator layer is usually modified to an amorphous tantalum suboxide ($\text{Ta}_2\text{O}_{5-\delta}$; $\delta \geq 0$) layer by intentionally adding oxygen vacancies. The initial oxygen vacancies can be

considered as the carriers that lower the resistance than perfect Ta_2O_5 . By changing the fabrication method, which will be describe in Chapter 3, this pristine oxygen vacancy concentration can be modified. Additionally, using oxidative metals, such as titanium (Ti) or tantalum (Ta), extra oxygen vacancies can be generated by scavenging the oxygen from the tantalum oxide into the electrode [64-66]. This can be considered as the secondary aspect that influence the initial oxygen vacancy concentration. Thus, the scavenging effect by the electrode should create the switching layer having high concentration of oxygen vacancy via diffusion into the insulator layer. The scavenging effect was reported that can improve the switching performance with intentionally add a second layer to the single-layer device [67].

1.3.4. Pulse applications and STDP behaviors

Not only to acquire enough compatibility to the current computer in short-term applications, but also to develop possibilities on the applications on biomimicking SNN for the future, switch capabilities based on the binary pulses or modulated pulses were considered essential. Specifically, the modulated pulse applications were used to achieve analog resistance changes [68-70]. Recently, to realize the full compatibility to the current deep neural network algorithms, symmetric conductance changes are being studied [71-74]. Symmetric conductance changes are considered to fit the current perceptron-based ANN. However, bio-mimicking concepts such as SNN do not require such characteristics since the inputs and outputs are not continuous. Here, we only discuss the possibility of the realizations of analog behaviors using various kinds of pulse form, which can be the best method to maximum the applying possibility of the resistive memory.

1.4. References

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Chapter 2 Motivation and contents of this work

2.1.Motivation and significance

As in the literature review, resistive memories can be easily fabricated and tested. Although many combinations of metal oxide and metal electrode had been reported for their limited validities, a systematic study of the correlation between the selected materials and the switching characteristics is still lacking. Tantalum oxide was selected in this study, as the insulator layer, because of its capabilities of stable switching relating to the existences of oxygen vacancy in the insulator. Several kinds of top electrode were also selected to see the differences. An extremely important device stage, the initial states, was introduced into the view. The distinguishable initial states were successfully achieved by the controlled fabrication conditions, and they influenced the switching characteristics in many ways. The characteristics in measurements and microscope observations were revealed (Chapter 4). They could decide if the device can switch at all (Chapter 5). They could change how gentle is the switching to achieve analog behaviors (Chapter 6).

To give a complete story from the underlying electrode/insulator scavenging mechanism to the brain-like STDP, we first focused on the initial states that influence the upcoming characteristics. With the detailed investigation of six different electrodes, we continue with deeper study on the analog switching behavior with photolithography-patterned devices, where small sizes are helpful to the stability. Finally, with the groundwork done, we move our attention to the optimizations of analog switching. The series of study revealed how does the initial states affect the analog switching, and whether the switching could be optimized.

2.2.Storyline

Three major sets of investigation were performed in this study. As shown in figure 2-1, initial states are firstly studied as a preliminary base data. Then, with carefully patterned device, the relationship between the initial state and analog switching can be revealed. Finally, with detailed information presented, the analog behavior to a practical use can be optimized. Next brief summaries of each part will be presented.

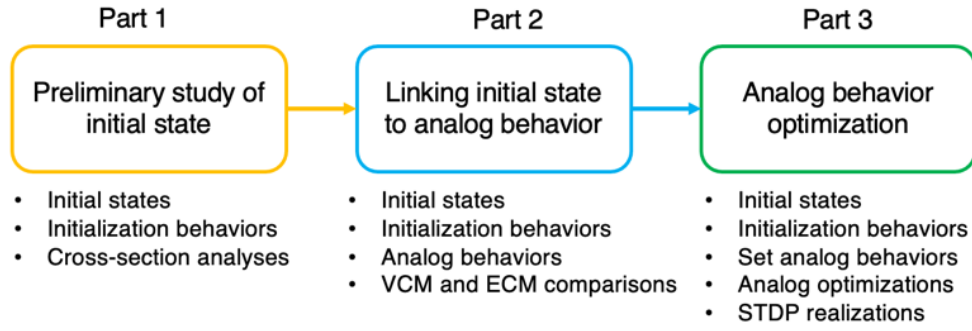


Figure 2-1. Schematic structure of the device.

Part 1 (Chapter 4): The study about the initial states of six electrodes will be presented. Here metal masks were used to pattern the devices. Specifically, TiN, Ti, Ta, Al electrodes were combined with two different pristine oxygen concentration conditions which provide different initial oxygen-vacancy concentration. The initial resistances were firstly measured. Then the initialization processes were carried to each device to obtain statistical results of the forming voltage. Finally, the samples were investigated by STEM and EDS to the cross-section to clarify the metal-oxide interface reaction and/or oxygen scavenging effects.

Part 2 (Chapter 5): The preliminary results about the initial states were carried to the next part. Four electrodes (Ta, Cu, Ti, Al) were selected, and devices were patterned using photolithography. With well patterned devices, switching behaviors were investigated by focusing on the scavenging effects of metal-Ta oxide interface and VCM and ECM mechanisms. The connections between each initial state and analog switching were investigated. Distinguishable initial states determined the initialization capabilities. And the initialized devices showed a predictive analog capability for the Ta and Cu electrodes.

Part 3 (Chapter 6): Here, the Ta-devices were selected for further test, because of its stable analog operation as studied in Part 2. To gain higher controllability with Ta/Ta₂O₅ system, we argued that the switching current (and the generated Joule heat) is argued to be a probable major issue for better performance. Thus, a thin SiO₂ film was inserted between the insulator and the bottom electrode as a current limiter. With current limitation, filament formation did not occur severely like the device in Part 2, and successful stable analog switching capability was realized on both set and reset process. We also took a step further and we found that with precisely controlled voltage threshold, the pulse can be a good way for switching. Finally, brain-like STDP was realized to demonstrate the device performance via this operation control.

Chapter 3 Experiment design and methods

3.1. Device fabrications and methods

3.1.1. Device structures and processes

The “sandwich” structure of resistive memory benefits the device implementation. There are two kinds of device structure that were being used in this study. The processes will be firstly discussed in this section. Then some important processes were described in detail because they are extremely influencing the results of the characteristic.

- **Fabricating 100 μ m devices patterned using the metal masks**

Metal masks are good for patterning the devices at a level of 100 μ m because they can be directly attached at the surface of substrates during sputtering. The production cycles were much shorter than the photolithography-based patterning. On an aim of investigation of the initial states, the metal-mask patterning was utilized because the patterning will minimize the fluctuation on the fabrication processes. Such devices that used metal-mask (MM) patterning will be refer as an MM-device in the following chapters.

In figure 3-1, the fabrication process is illustrated. While the process-3 in figure 3-1 (i.e., setting of MM) was done in air, this process was done as quick as possible (typically 2 min) to prevent further oxidation (influence by moisture) of the Ta₂O₅ operation layer.

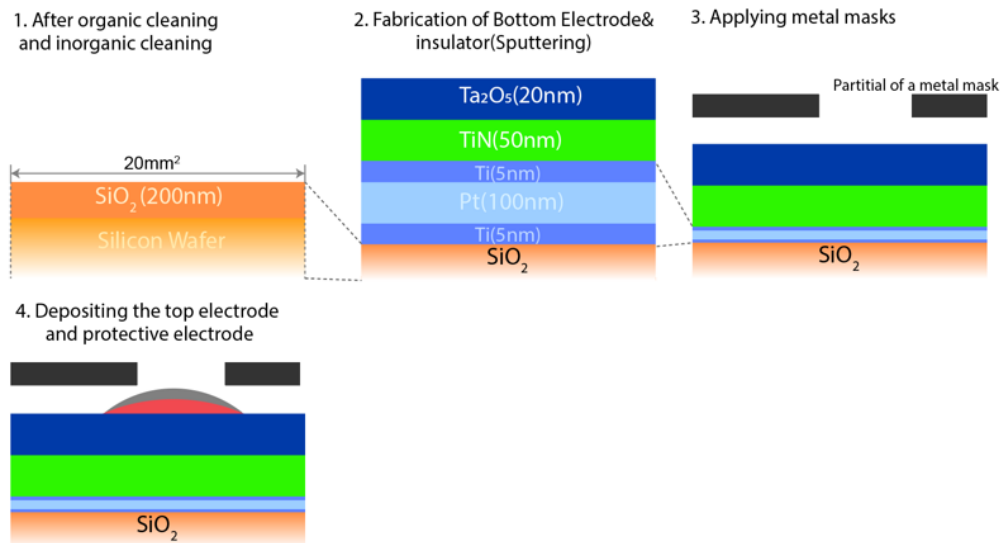


Figure 3-1. The fabrication process of the MM-devices.

- **Fabricating 4~64 μ m scaled devices by photolithography patterning**

For good scaling of the devices, photolithography was used to approach practical uses as near as possible. Only the outline of this procedure is explained here while details concerning lithography will be explained in Sec. 3.1.3 and 3.1.4. As shown in figure 3-2, the structures near the bottom electrode were fixed as the same with the MM-devices. First photolithography was carried to form patterns of the VIA holes (4~64 μ m) and contact holes of the forms of the bottom electrode. Then the reactive-ion etching was used for etching VIA and the contact holes according to the patterning. The etching duration was calculated to ensure the holes penetrated the SiO₂ insulating layer and stopped in the TiN layer. The second photolithography performed after this VIA hole opening was designed for top-electrode fabrication. Here, the photoresists were different from that of the first lithography as described later. After the final depositions of the Ta₂O₅ insulator, the top electrode and the protective platinum layer, the lift-off was carried for the finish. In figure 3-3, an optical microscope image of 8 μ m device were shown. In figure 3-4, cross-sectional scanning electron microscopy (SEM) and transmission electron microscopy (TEM) images of the fabricated device are presented. Devices with smooth taper edges were successfully fabricated.

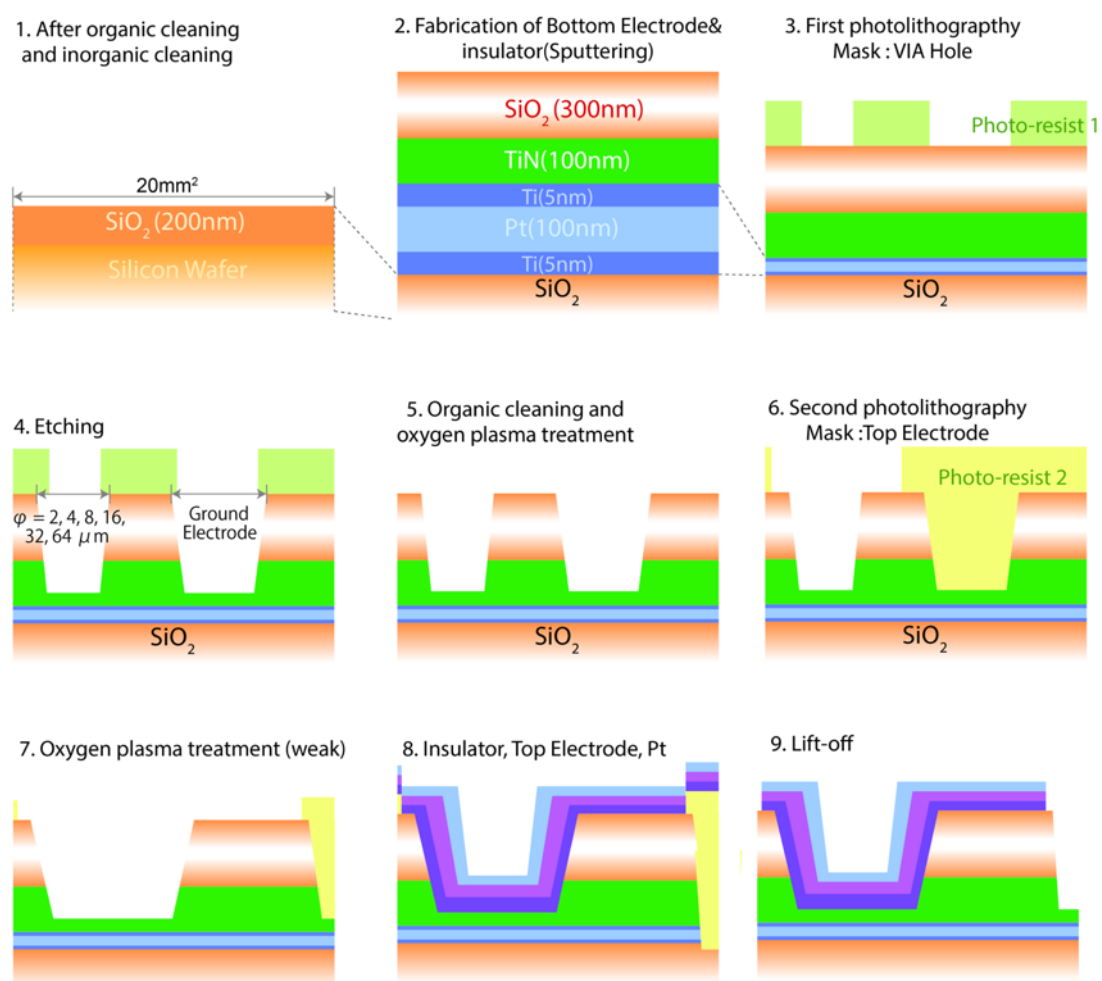


Figure 3-2. Schematic structure of the device.

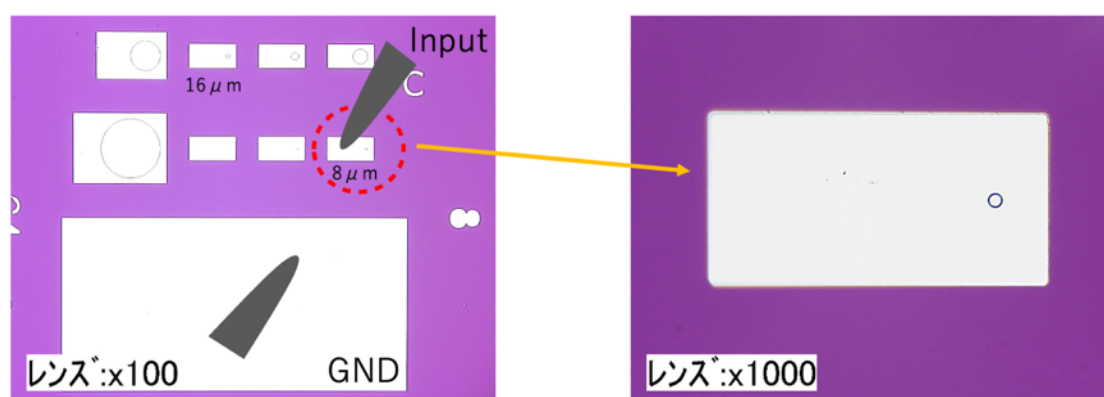


Figure 3-3. Optical-microscope pictures of one of the fabricated devices.

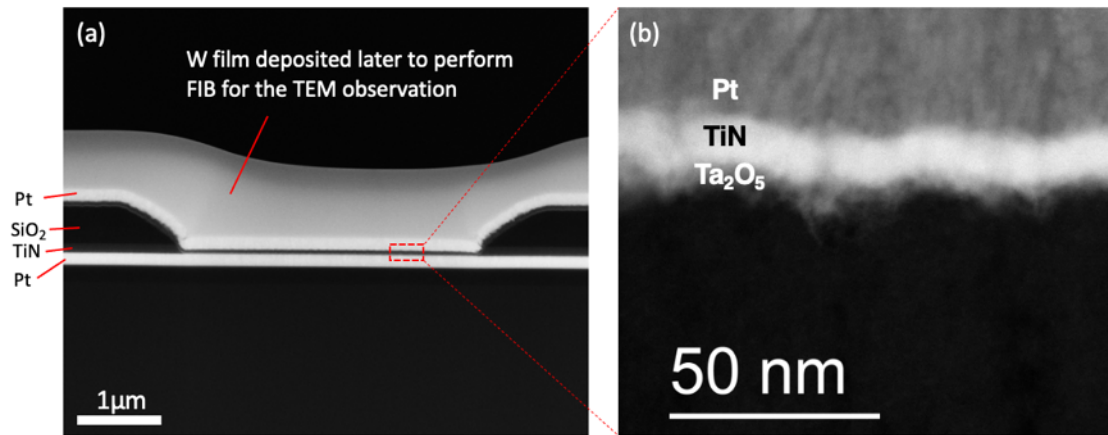


Figure 3-4. (a) SEM and (b) TEM images of one of the fabricated devices.

3.1.2. Radio frequency sputtering

All the thin films in this study were deposited by the radio frequency sputtering to ensure the data consistency. In figure 3-5, basic principles are presented. The ionized argon atoms hit the material target to release the charged atoms from the target. Under the electric field between substrate holder and the target, the sputtered atoms can be deposited onto the substrate. The method is usually used for the depositions of materials that have high melting point under a relatively low temperature environment.

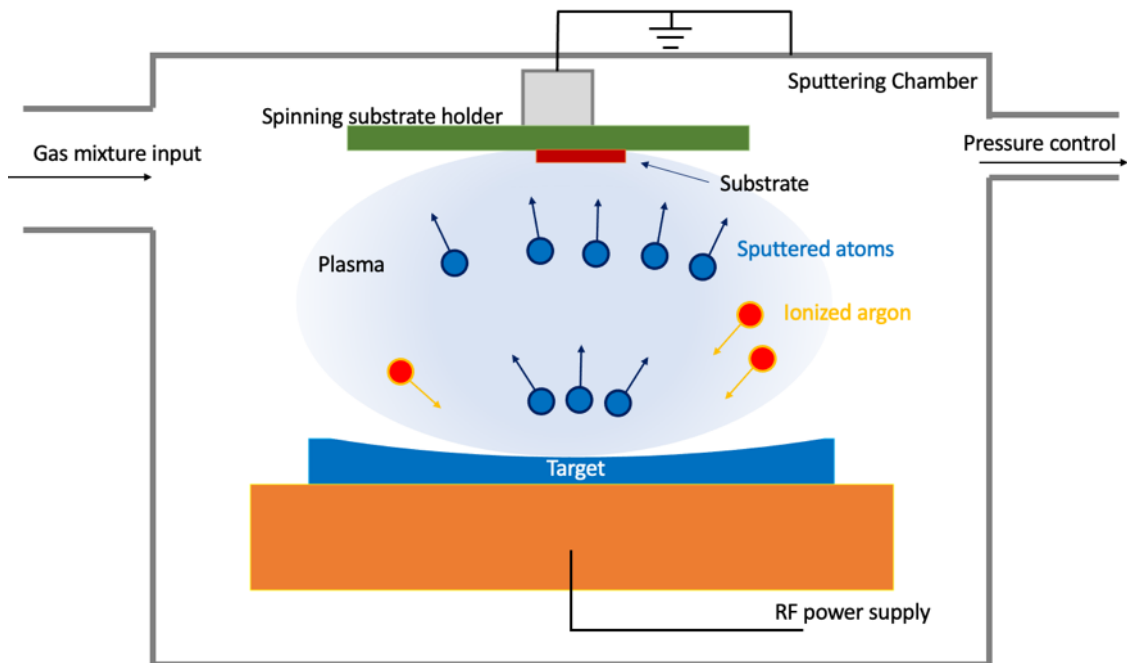


Figure 3-5. Schematic structure of the device.

Since the film depositions were the most important process in the study, the processes, detailed parameter control and initial condition control will be presented as following.

- **A general process**

Preparations: The prepared substrate(s) were firstly attached onto the sample holder so they can be put into the sputtering chamber. Then according to the material that needed to be deposited, the targets were changed. After necessary chamber cleaning, the chamber was being vacuumed to a high vacuum states that were typically under 4×10^{-4} pascal.

Gas flow initialization: The sputtering gas was feed to the chamber at a rate of 20 sccm during the pre-sputtering and formal deposition. However, the flow rate was initial set to 30 sccm to increase the possibility of the plasma generation. After the plasma environment was created under low RF power such as 20 watts, the gas flow was adjusted to 20 sccm again. In specific depositions, such as TiN or Ta₂O₅, different combinations of gases were used as reactive sputtering.

Impedance matching for plasma generation: The RF power was firstly set to 20 watts to generate plasma. A circuit was used for the for the impedance matching of the plasma, where the principle is basically adjusting two capacitors. After the successful generation of initial plasma, the reflected power was further minimized by adjusting the same capacitors. The gas flow was reverted to 20 watts and the input power was increased gradually to typically 100 watts. The distance between the target and the holder was also controlled by 80mm or 95mm. Finally, the chamber pressure was adjusted to 1 pascal by tuning the vacuum pipe volume.

Pre-sputtering: The shared targets were cleaned before the formal deposition by applying additional time with the same condition described earlier. Key material targets like Ta or Ta₂O₅ were pre-sputtered by typically 30 minutes.

Film deposition: The shutter above the active target was opened manually after the pre-sputtering and closed automatically when the object duration was reached. During the deposition, the sample holder was rotating at a rate that was about 10 seconds per cycle.

- **Parameter control**

As described earlier the sputtering processes were controlled as delicate as possible. The most important films in this study, the deposition of Ta₂O₅ was modulated by controlling the

conditions strictly. The same pure Ta₂O₅ target was applied throughout the study. The pre-sputtering duration was increased to 30 minutes to minimize the film quality fluctuations. By changing the compositions of the mixture of the gases (Ar and O₂), the oxygen vacancy concentration in the operation layer (Ta₂O₅) can be modified. The surface of the Ta₂O₅ ceramic target became dark after sputtering with pure Ar, indicating partial metallization by reduction, while its color recovered to be white after a process using Ar+O₂. By changing the duration, the thickness can be simply modified with measured deposition rate. Because the thickness of deposition is also sensitive to the position on the holder, customized holder that has circled grooves that can insert 20mm square substrates that have the same radii from the center of the holder.

3.1.3. Spin-coating and photolithography patterning

Photolithography processes were carried in the second and the third part in the study. The basic procedures including spin-coating of the photoresists and photolithography are presented in figure 3-6.

- **Spin-coating the photoresist**

The photoresists were coated onto the SiO₂/Si substrate evenly by rotate the substrate at high RPM (rotations per minute), where the substrate was held using a vacuum chuck. Then the pre-baking at relatively low temperature was performed. To fabricate device in a VIA hole, two patterning processes using different chemicals were required. In the first process directly on the SiO₂ substrate, hexamethyldisiloxane (HMDS) was used for the good adhesion. Afterwards, OFPR-800 photoresist was coated. The rotation parameters were typically 2000 RPM, and the 90-second pre-baking temperature of 110 °C was applied for HMDS and OFPR. For the second patterning, polymethylglutarimide (PMGI) resist was firstly applied that substitutes HMDS since the bottom metallic electrodes were exposed by the etching. The rotation parameters were typically 2000 RPM. The pre-baking temperature for PMGI was 190 °C with the duration of 5 minutes. The pre-baking temperature for OFPR was the same 110 °C with the duration of 90 seconds.

- **Photolithography patterning**

365nm UV light was used for the exposure. The exposure duration was typically 7 seconds, which was evaluated every time using measured illuminance to prevent errors caused by instability of the mercury light used for lighting. An empirical 20% over-exposure time was applied for the good results. As described above, the OFPR-800 single-layer was used to pattern the VIA holes, while OFPR-800/PMGI double-layer was used for formation of the VIA hole patterns. The NMD-3 developer was used in both cases. The development time for the pattern of OFPR-800 was about 90 seconds, where details were decided after eyesight confirmation. In the latter case to form the device patterns, additional time (200 seconds) was used to develop the PMGI sacrifice layer. In this case also, the development time was modified each time after eyesight confirmation using an optical microscope. Successfully developed devices were post-baked for the good plasticity.

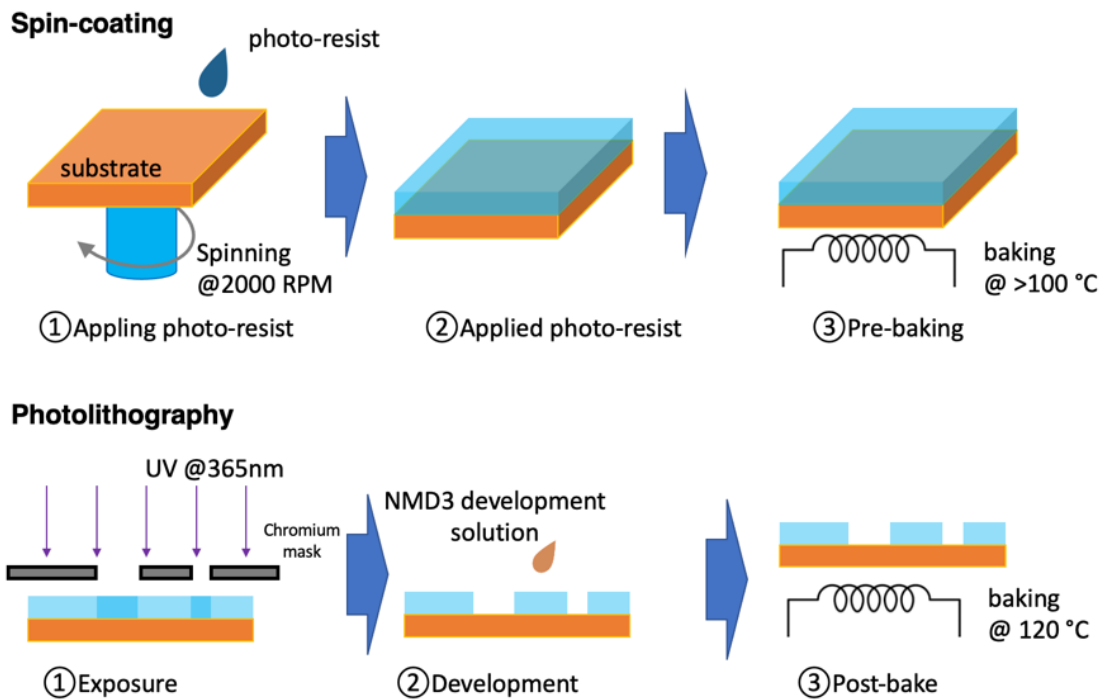


Figure 3-6. Schematic structure of the device.

3.1.4. Reactive-ion etching

The VIA holes were excavated by the reactive-ion etching (RIE) process shown in figure 3-7. The CF_4 and oxygen mixture gas was inputted to the chamber. The stage power was set to 300

watts and the antenna power was set to 10 watts. By typically etching for 7 minutes (50% over etching), the holes were excavated for about 400nm that penetrates the SiO₂ layer and stopped in the TiN layer. Because the photoresists were at micrometer level, they remained on the surface. Dimethylformamide (DMF), acetone and ethanol were used in the organic cleaning. To clean the organic substance residual completely, oxygen-plasma treatment was applied for 10 minutes. Weak oxygen-plasma treatment was performed also in the second-time photoresist process to remove the residual on the surface of the bottom electrode.

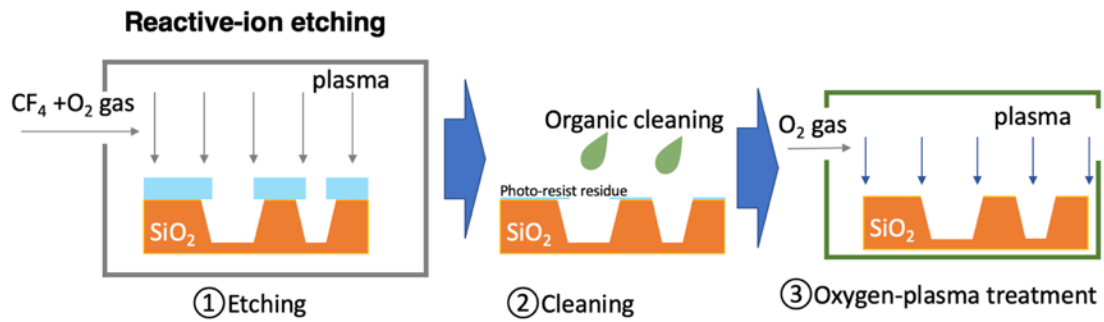


Figure 3-7. Reactive-ion etching and oxygen-plasma treatment processes.

3.1.5. Other important processes

- **Inorganic cleaning and organic cleaning of substrates**

The pristine substrates were cleaned by organic cleaning and inorganic cleaning because of the remaining protective photoresists from the dicing procedure. The organic cleaning used typically in the order of DMF × 2, acetone × 2 and ethanol × 1 in an ultrasonic cleaner for 5 minutes each. The temperature was not heated deliberately.

Inorganic cleaning was performed using the mixture of concentrated sulfuric acid and hydrogen peroxide for 5 minutes with continuous blending to gain thorough cleaning. Then the substrates and the holder were put into the deionized water to dilute the residual.

- **Oxygen-plasma treatment**

Two kinds of oxygen-plasma treatment were applied in this study. As introduced earlier, the treatment was used to the residual photoresist removal after the RIE, which was considered a high-power treatment. After the second photolithography, the photolithography patterns were needed for the final lift-off. So, only weak treatment was needed to thinner the photoresist. An

aluminum bucket was put into the chamber with the samples to weak the treatment power. Both treatments use 15 minutes pre-treatment and 10 minutes formal treatment.

- **Lift-off**

As shown in figure 3-3, a final lift-off was needed to remove the surplus resists and deposited films. DMF was used two times for 5 minutes for each with ultrasonic cleaner to resolve the substance completely. Then, with no ultrasonic cleaner applied, acetone $\times 2$ and ethanol $\times 1$ were used to finish the process. The finished devices were shown previously in figure 3-4. Although we tried to minimize the time from the final deposition to the initial state measurement about two hours.

- **Sample transfer and storage**

The samples at different fabrication stages were needed to transfer to other buildings during the experiments. Typically, the samples covered with unexposed photoresists were kept in a black box to avoid nature UV light illumination. And to avoid unwanted waste sticking to the sample, the box can be only opened in a clean room.

The moisture also could influence the characteristics of the device, so the fabricated samples were stored in dehumidified boxes. And the ongoing samples were kept in a vacuum chamber.

3.2.Device parameters and measurement methods

3.2.1.Device states and parameters

- **Initial states**

The state right after the final lift-off was called initial state (or the pristine state) because it has not been applied any external influences. The initial resistance (R_{ini}) was firstly measured at 100 mV for each device, where the linear characteristics did not show any resistance change. Then the *initialization* process was applied to the device by applying higher voltage. A typical log-log “forming” sweep curve for the VCM device is shown in figure 3-8. The dashed-line arrows indicate the voltage sweep direction. The curve was almost linear in the low-voltage region (i.e., around the region marked ‘ R_{ini} ’). The conductance increased with voltage, and the current reached the compliance current at a certain voltage (I_{comp}). These forming operations were

used for device initialization, and, thus, V_{Form} is called the forming voltage. When the current rapidly increased, the resistance became low (R_{LRS}).

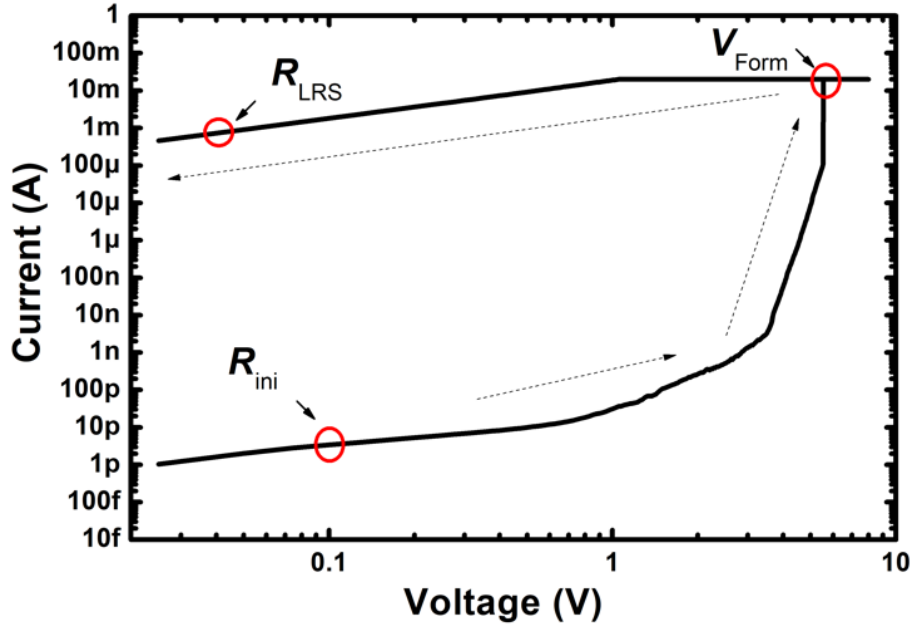


Figure 3-8. Typical I - V forming curve (log-log format of the TiN-50% MM-device). The dash-line arrows indicate the direction of the voltage sweep. The initial resistance R_{ini} decreases to R_{LRS} via forming at V_{Form} . © Copyright (2021) The Japan Society of Applied Physics

- **High resistance state (HRS) and low resistance state (LRS)**

The initialization characteristics are generally different from the functioning switching characteristics. For example, for the VCM-devices, the switching windows were much lower than the R_{ini} . In the functional switching, the resistance states can be described in a binary sense as high resistance states (HRS) and low resistance states (LRS). A set process with a voltage sweep positively biasing the top electrode induced relatively low resistance called LRS. A reset process with negative voltage sweep induced relatively high resistance called HRS.

In analog switching, the concept of HRS is weaker because there are several resistance states between the HRS and LRS. So, the word HRS in this study will refer to the highest resistance that could be achieved by reset in the respective device. LRS will refer to the lowest resistance could be achieved by set. And median analogous resistive states will be marked as middle resistive states (MRS).

- **Malfunctional states**

Natural combinations of the material could induce switching failure. Degradations by the measurement also could cause the device failure. Normally, the device becomes LRS-like states, that could not be switched in any forms.

3.2.2. Measuring the device parameters

The electrical properties were evaluated using a semiconductor parameter analyzer Agilent B1500A and Agilent 4156C that can measure the current at the pA level. The measurements were performed at room temperature in air by biasing the top electrode (TE) while the bottom electrode (BE) was grounded.

- **Current-voltage (I - V) sweep measurements**

Current-voltage sweep measurement performs gradual voltage increase to the set voltage and, by optional, the reverse directional sweep. The method was used in the R_{ini} measurements, initialization, analog measurement and endurance consecutive tests. The voltage sweep rate was typically 200 mV/s. The example of sweep measurement was shown in figure 3-8.

- **Time-current measurements**

Instead of sweeping voltage, time-current measurements were carried out using fixed voltage to investigate the time dependence on the voltage. It is a way to get hints of filament change because of the continuous change of current. This method was also used as a preliminary investigation of the pulse experiments. Because the similar form can be used to refer to the pulse parameters such as pulse number. An example is as shown in figure 3-9.

- **Pulse measurements**

Pulse generators (optional function of Agilent B1500A) are introduced to the measurement procedure if the sweep performs well or on the circumstance that sweep fails and another approach was needed. As shown in figure 3-10(a), a pulse contains two sub-pulses, switching pulses that have relatively high voltage and read pulses that were typically 20 mV. Figure 3-10(b) shows an example of the changed resistance by applying 200 cycles of the pulse where the step-like contrast in the graph is caused by moiré occurring in printing.

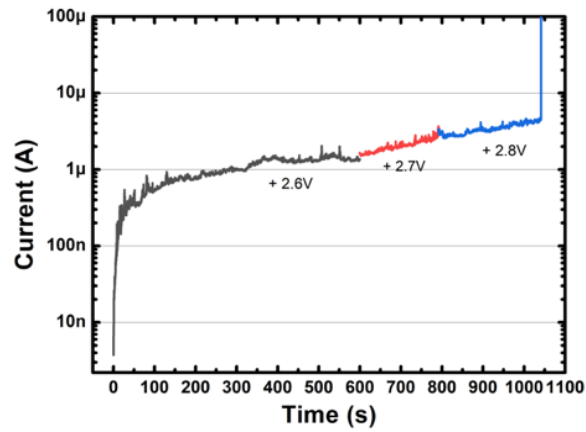


Figure 3-9. Typical current-time sampling. With three increase voltage, the device forms as the end.

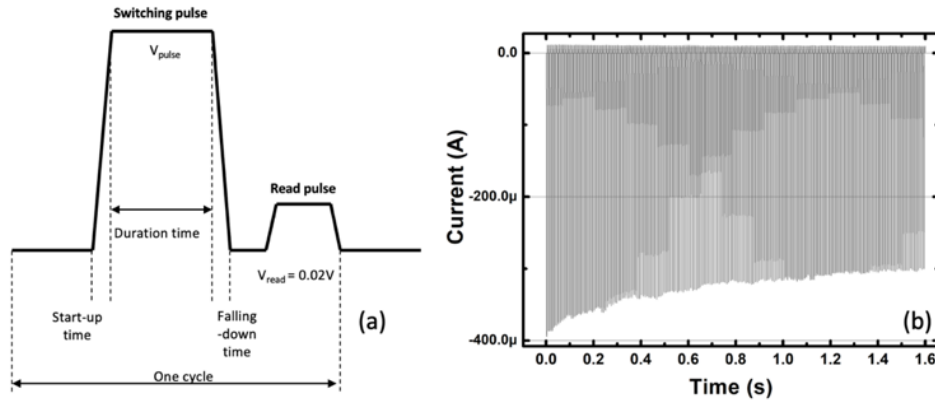


Figure 3-10. Pulse application example. (a) The compositions of a pulse. (b) With increased number of pulses, the resistance increases because of the reset pulse.

3.2.3. TEM observations

For microstructural analyses using transmission electron microscopy (TEM), the samples were processed to thin chips via focused ion beam milling (FIB, FEI Quanta 3D 200i) followed by Ar ion thinning (Gatan PIPSII M-695). They were then observed using a STEM (JEOL ARM-200CF operated at 200 kV) equipped with an analyzer for energy dispersive X-ray spectroscopy (EDS). The electron beam current used for EDS mapping was ~180 pA, which was much larger than the current for conventional STEM observations (~16 pA). The resolution was typically 2048 x 2048 pixels in the observed area.

Chapter 4 Controlled initial state by oxygen vacancy

4.1.Introduction

Although the resistive switching can be achieved by various kinds of metal electrode, such as using Ta as a valence change memory or using Cu as a conductive bridge memory, scavenging electrode based VCM has shown its profound probabilities in realizing the analog switching in a stable sense. VCM switching operation is based on the formation and rupture of conductive oxygen vacancy filament(s). Therefore, modulation of the oxygen vacancy into the Ta_2O_5 switching layer is a key factor for realizing stable switching operation. Hereafter, Ta_2O_5 containing certain amounts of oxygen vacancy will be described as $\text{Ta}_2\text{O}_{5-\delta}$ where δ should be small and its value depends on the situation [1, 2].

As we described earlier, the sputtering processes were carefully manipulated for modulating the oxygen vacancy concentration in the initial state. By applying scavenging electrodes in this work, the electrode-effect must be taken into consideration. Before the depositions of the top electrode, the deposited Ta_2O_5 insulator films were considered at the original states because the effects of scavenging electrode have not been applied. In this stage, manipulating the deposition conditions is a way to control the amount of intrinsic oxygen vacancy concentration (IOVC) included in the $\text{Ta}_2\text{O}_{5-\delta}$ layer [3-6]. For example, in the case of devices prepared via sputtering in an $\text{Ar} + \text{O}_2$ atmosphere, the R_{ini} , the V_{Form} , and subsequent switching properties can be modified by changing the oxygen ratio in the ambient gas [1]. Although the differences in the oxygen content in $\text{Ta}_2\text{O}_{5-\delta}$ is undetectably small for conventional analysis (e.g., X-ray photoelectron spectroscopy; XPS), the characteristic distinguishability was found [2]. This original insulator can be modified after the deposition by depositing an oxidative metal as the electrodes [1, 7-9]. At this stage, scavenging electrodes can be considered spontaneously absorb oxygen atoms from $\text{Ta}_2\text{O}_{5-\delta}$, generating extrinsic oxygen vacancies that serving as an oxygen vacancy source [10]. Because of this scavenging effect, the characteristics can be expected to be adjusted via selection of the electrode materials. As reviewed above, the conductive oxygen vacancy filament contributes to the VCM operation. Therefore, both intrinsic and extrinsic oxygen vacancies should influence the memory properties profoundly. Thus, the combination of the deposition

condition and selection of the electrode material should alter the electrical properties of the device. However, a systematic study of these aspects is still lacking.

In this part of study, we tested four typical scavenging electrode materials (TiN, Ti, Ta, and Al) to modify the extrinsic oxygen vacancies using two kinds of Ta₂O_{5- δ} insulator. The electrical characteristics were firstly investigated. Since the write/erase operations are also strongly influenced by the measurement parameters, such as the maximum voltage, current limit (*i.e.*, I_{comp}), measurement methods, and memory verification, we only focused on the initial resistance (R_{ini}) and the forming operation, which are key aspects for device functionality. The results demonstrated the possibility that the initial resistance and the forming properties are influenced both by the intrinsic and extrinsic oxygen vacancy concentration. To give detailed information about the metal-insulator interface, we performed extra experiment using another set of flat devices. The TEM observations and EDS analyses were performed for the eight devices.

4.2. Device fabrications and measurement

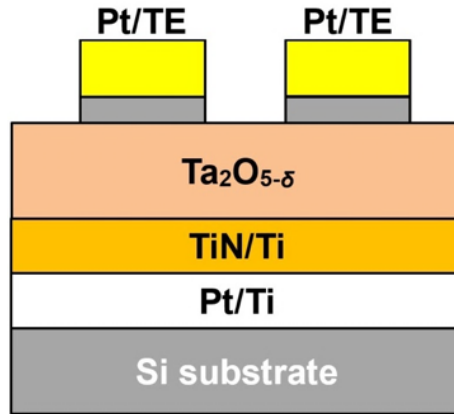


Figure 4-1. Structure of the device. © Copyright (2021) The Japan Society of Applied Physics

The device structure used in this part of study is schematically shown in figure 4-1. All thin films were deposited via RF magnetron sputtering as previously described. The silicon 20 mm square substrates were set typically 80 mm above the sputtering targets. Firstly, the Ti (5 nm)/Pt (100 nm)/Ti (5 nm) layers and TiN-BE (100 nm, bottom electrode) were deposited. Ti layers were applied for good adhesion. The TiN layer was deposited under an Ar+N₂ mixture atmosphere, while the other layers were deposited in an Ar atmosphere. Next, the tantalum oxide layer was formed using a Ta₂O₅ target in an Ar+O₂ atmosphere. In this work, two conditions with

different O_2 concentrations were used, as shown in Table I, where $f_{\text{depo}} = f_{O_2} / (f_{Ar} + f_{O_2})$ is defined to express the Ar/ O_2 ratio during deposition [1]. f_{Ar} and f_{O_2} are the flow rates of Ar and O_2 , respectively. This allows for modification of the amount of IOVC contained in the $Ta_2O_{5-\delta}$ thin film between “high” or “low”. The film thickness was fixed at ~ 20 nm. Finally, top electrodes (TE) covered by Pt protective layers ($100 \times 100 \mu m^2$) were formed using a metal mask in an Ar atmosphere. The typical thicknesses of the TE and Pt layers were 10 nm and 100 nm, respectively. The tested TE materials for the VCM were Ti, Ta, and Al. In addition, TiN was selected as a reference TE because it should have almost no reaction with the $Ta_2O_{5-\delta}$ thin film [11]. Among them, the Al device had no Pt protective layer because possible alloying of Al and Pt may generate unexpected high resistance affecting the results [12, 13]. In this case, the Al thickness was 100 nm. Examples of cross-sectional images observed via STEM are shown in figure 4-2. Nonetheless, clear layer stacking could be identified, while the layer interface was wavy due to surface roughness of the TiN bottom electrode. A list of fabricated devices is summarized in table I. Devices were fabricated under these eight combinations for the comparison. The devices with $f_{\text{depo}} = 0\%$ and $f_{\text{depo}} = 50\%$ are referred to as the 0%-device (or high IOVC) and 50%-device (or low IOVC), respectively.

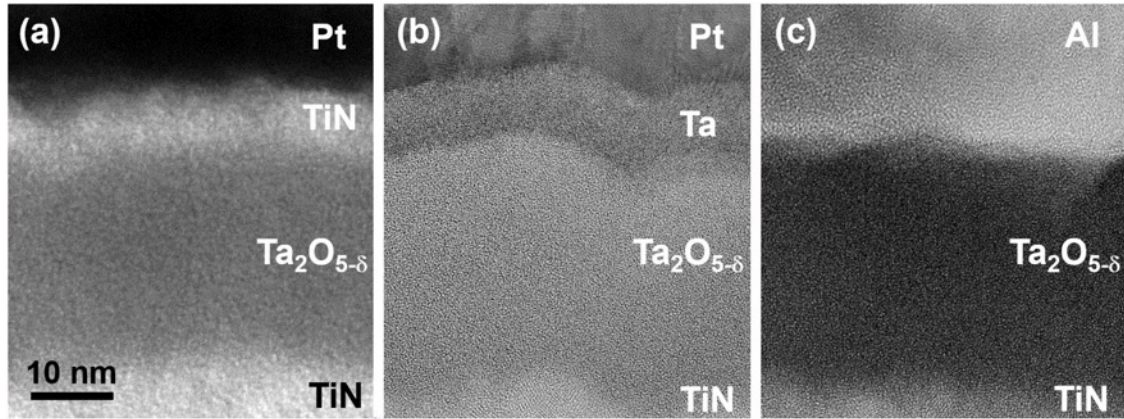


Figure 4-2. Cross-sectional bright-field STEM images for (a) TiN-0%, (b) Ta-0% and (c) Al-0% devices. © Copyright (2021) The Japan Society of Applied Physics

Table I. List of the fabricated samples.

		f_{depo}	
		0%	50%
Electrode	TiN	TiN-0%	TiN-50%
	Ti	Ti-0%	Ti-50%
	Ta	Ta-0%	Ta-50%
	Al	Al-0%	Al-50%

Because the purpose of this part of research is not the investigation of the functional write/erase operations, only current-voltage (I - V) initialization sweeps were performed to the pristine devices where positive voltage was applied to the TE. The current limit (I_{comp}) was set to 20 mA throughout this work to reveal the full forming processes for all devices even though hard breakdown may occur. While many of this process induced malfunctional states, the resulting state will be called the low resistive state (LRS) in this report. More than 20 devices were measured for each of the 8 fabrication conditions to ensure data fidelity.

For the clearer TEM observation, simple flat TE/insulator devices were also fabricated, which will be discussed later.

4.3. The initial states

4.3.1. Initial resistance

R_{ini} results for the device in the pristine states prepared under 8 conditions are summarized as a cumulative graph in figure 4-3(a). All the conditions displayed a narrow distribution, and thus, the devices were well fabricated and characterized. The R_{ini} values of the 0%-devices were much lower than those of the 50%-devices. The results suggested that oxygen in $\text{Ta}_2\text{O}_{5-\delta}$ was deficient on reducing the oxygen fraction in the sputtering gas. In figure 4-3(b), the median values are plotted to compare the fabrication conditions. The 50%-device with the TiN-TE showed an extremely high resistance $R_{\text{ini}} \sim 100 \text{ G}\Omega$. This should be an intrinsic property of $\text{Ta}_2\text{O}_{5-\delta}$ with low IOVC because the oxygen scavenging effect by TiN would be very weak. The other TE materials (Ti, Ta, and Al) showed lower R_{ini} , which could be attributed to the expected oxygen scavenging. However, the reduction in resistance was small. This suggests that oxygen vacancies introduced

by the electrode were localized mainly in the top part of $\text{Ta}_2\text{O}_{5-\delta}$ and did not affect the overall R_{ini} significantly. In contrast, the 0%-devices revealed a clear difference between the electrodes. Here, the TiN devices again had the highest R_{ini} in this group, where the resistance reduction from the TiN-50% device was about two orders of magnitude. This reduction must be caused by increase of the IOVC in the 0%-device, because the scavenging effect of TiN should be weak. Resistance drops for the other TE devices occurred with various degrees. From figure 4-3(b), it can be clearly seen that the 0%-devices with Ti, Ta, and Al electrodes showed resistance drops of at least four orders of magnitude compared with those of 50% devices (two orders more than TiN). The clear difference between the 0%- and 50%-devices for these electrodes indicates that the extrinsic oxygen vacancies generated near the metal-insulator interfaces diffused into the deeper regions of the 20-nm-thick high IOVC, which resulted in the reductions of the overall resistance.

Here, metal-insulator interface is illustrated as shown in figure 4-3(c). The tantalum oxide layer contains intrinsic oxygen vacancies (intrinsic O_V , open circles in figure 4-3(c)) that was intentionally added by modulating f_{depo} parameter. After deposition of the top electrode, a certain amount of oxygen was scavenged to generate extrinsic O_V (dotted circles). As a result, an O_V -rich area is formed at the top of $\text{Ta}_2\text{O}_{5-\delta}$. The bottom of the electrode was also modified by taking oxygen atoms (full circles). On top of the electrode, there is an intrinsic area that remained conductive because it did not participate in scavenging. The R_{ini} decreases of the Ti, Ta, and Al devices were caused by the scavenging layer (the oxygen-exchanging region), or effectively by the reduced insulator on the top of the original $\text{Ta}_2\text{O}_{5-\delta}$ layer. Perevalov et al. reported that the resistance of $\text{Ta}_2\text{O}_{5-\delta}$ decreased exponentially and tended to saturate with increasing IOVC [2], and thus even small oxygen deficiency may contribute to R_{ini} reduction. As a result, it was thought that the thickness of the oxygen deficient region in the high-IOVC devices with the Ti, Ta, and Al electrodes was thicker than that of the low-IOVC devices.

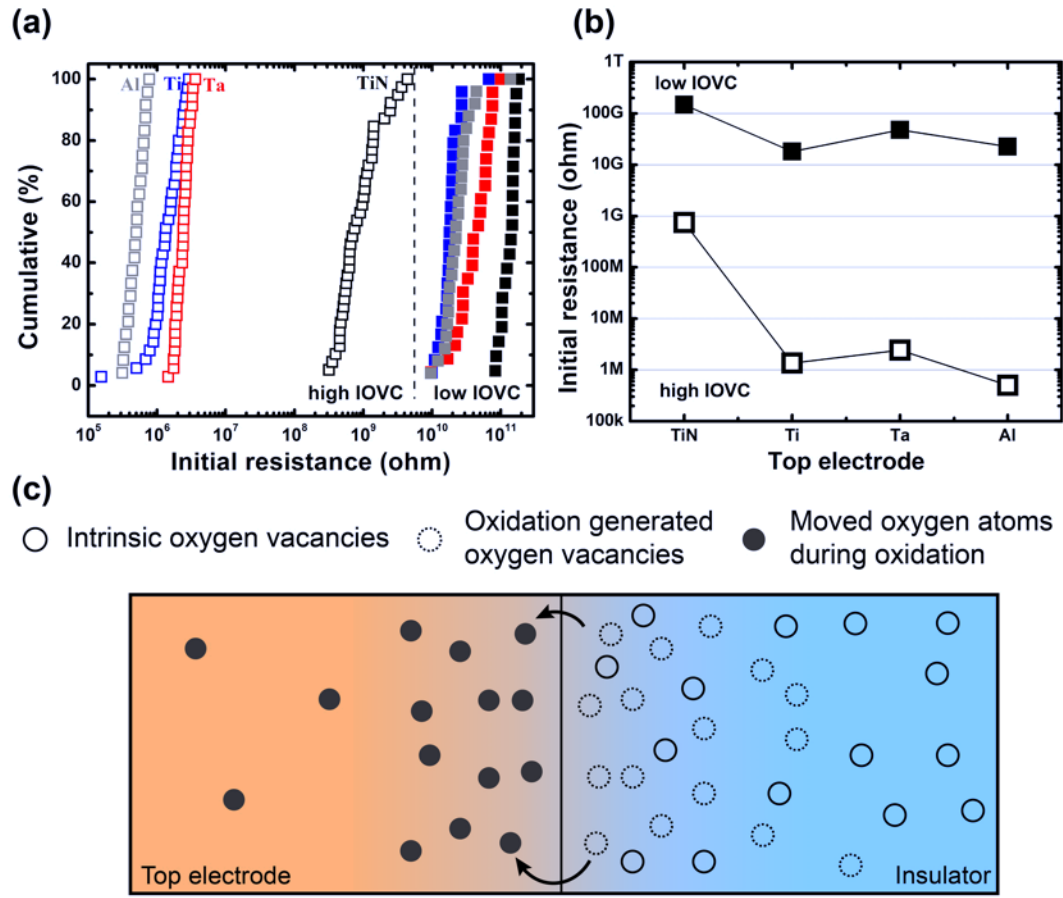


Figure 4-3. (a) Cumulative graph of R_{ini} of more than 20 devices on the same chip. (b) The median results of the R_{ini} are plotted: solid blocks for low IOVC and squares for high IOVC. (c) A possible initial resistance model for the fabricated devices. Because of the electrode scavenging, oxygen atoms move to the top electrode. © Copyright (2021) The Japan Society of Applied Physics

The results suggested that the diffusion constant of oxygen atoms increased as the oxygen vacancy concentration increased. The diffusion constant of oxygen may depend on the density of the oxide, as previously proposed [14]. The scavenging effect of the electrode was discussed using the oxide formation energy [5, 6]. The R_{ini} for the three metal electrodes were $Ta > Ti > Al$ and basically followed to this discussion. It was pointed out that the scavenging effect should be influenced also by oxygen movement in the TE (e.g., along the grain boundaries) and its oxidized region at the interface [15]. In this work, however, this was not clearly identified behind the effect of the oxide formation energy.

4.3.2. Forming voltage

The initialization process, referred to as forming, is an important treatment that can influence practical switching behaviors in both good and bad ways. Usually, the compliance current for forming is set as low as possible to avoid device destruction. However, when the current before forming is not sufficiently small, the forming process cannot be realized. Therefore, in this work, a compliance current of 20 mA was used even if it would cause malfunctional states. Detailed information on the properties related to oxygen vacancies will be provided for all pristine devices. Typical forming curves are summarized in figure 4-4, where only the forward sweeps from 0 to 6 V are presented. These graphs are characteristic to memory initialization where abrupt current jump occurs at the certain voltage. This abrupt change is called *forming* where the conductive filament used in the memory operation is formed. The curve characteristics differed from each other for (a) high and (b) low IOVC. In the following discussion, we will focus on the forming voltage (V_{Form}) and the resistance after forming (R_{LRS}).

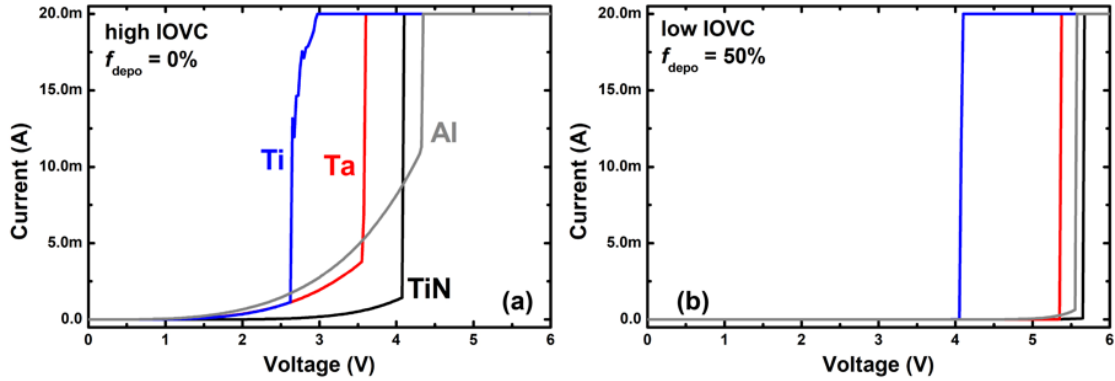


Figure 4-4. Typical forming curves of (a) high and (b) low IOVC devices. The meaning of the color in (a) and (b) is the same each other. © Copyright (2021) The Japan Society of Applied Physics

As identified in the two graphs of figure 4-4, the V_{Form} values for these two IOVC conditions clearly differ from each other. Looking at figure 4-4(a) for 0%-devices (high IOVC), the current gradually increased with voltage. The current values before forming well corresponded to the sequence of R_{ini} . In figure 4-4(b) for 50%-devices (low IOVC), it was much smaller as expected from high R_{ini} value. Comparing these graphs, V_{Form} was higher in low IOVC devices. In figure 4-5(a), the resulting V_{Form} values are summarized using all measured devices as cumulative

graphs. While V_{Form} showed large variability, difference between the high and low IOVC devices were clearly seen. From figure 4-5(b) summarizing the median results, it is recognized that V_{Form} of the low IOVC was about 1.5 V higher than the value of the high IOVC.

While the conductive path was formed by gathering oxygen vacancies [16], its formation energy seems high under the low IOVC condition as expected from fig. 4-5. Devices with Ti and Ta had relatively low V_{Form} , and specifically, Ti needed the least amount of energy in the formation. Notably, despite the unclear differences in R_{ini} , all the devices had clear differences for V_{Form} , which suggests that the scavenging layer was more related to the respective forming processes. The results indicated that the scavenging layers formed differently because oxygen was scavenged by the electrode over different ranges. The oxide formation energy of TE element has been discussed to explain different V_{Form} results, and the low formation energy providing many oxygen vacancies in Ta_2O_5 has been reported to show low V_{Form} [6]. The present results for TiN, Ti and Ta followed this tendency. The net oxygen vacancy concentration increased via the scavenging effect depending on the TE material. The generated extrinsic oxygen vacancies near the TE/ $\text{Ta}_2\text{O}_{5-\delta}$ interface drifted towards the BE during the forming process and made filament formation easy. However, the Al was an exception. The device with Al showed a high V_{Form} similarly to the TiN devices for both IOVCs, while its R_{ini} was much lower than those of TiN devices. Because Al is thought to generally form a stoichiometric Al_2O_3 insulator, we speculate that the bottom of the top electrode consisted of a thin Al_2O_3 -like insulator film, and it should contribute to high V_{Form} . This issue will be discussed later using STEM and EDS results.

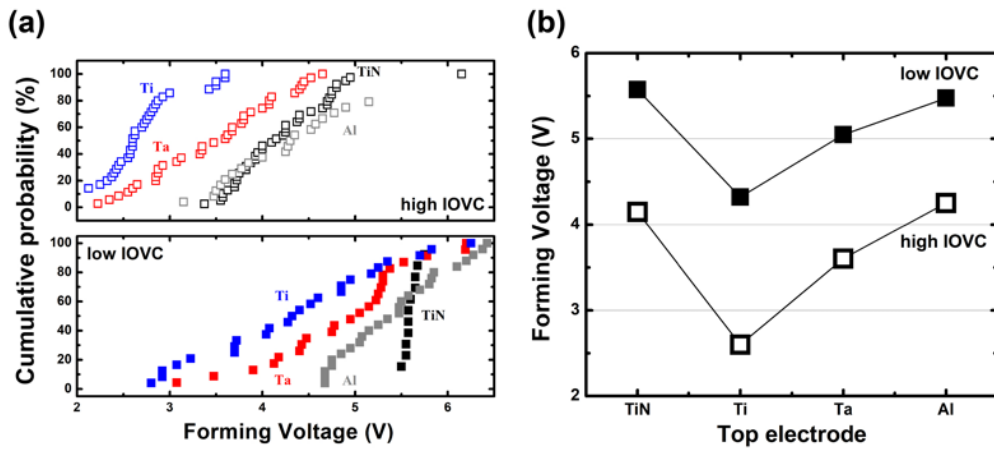


Figure 4-5. (a) Cumulative graph of measured V_{Form} of more than 20 devices on the same chip and (b) the median values. © Copyright (2021) The Japan Society of Applied Physics

4.3.3. Low resistive state

The condition of the forming process affects R_{LRS} as well. The cumulative graphs of R_{LRS} are shown in figure 4-6(a) and the respective median results are shown in figure 4-6(b). Here, the compliance current of 20 mA was set by a semiconductor parameter analyzer, and thus, current overshoot during abrupt resistance drop at forming cannot not be eliminated effectively. Under this measurement condition, strong filaments (or hard breakdown) are expected for high V_{Form} . Because of the high V_{Form} of the TiN and Al devices, the R_{LRS} of these devices was $\sim 100 \Omega$, which is typical of metallic filaments [17-18]. However, the Ti and Ta devices had higher R_{LRS} . There are many reports on analog (multi-level) switching using the TEs [9, 19]. Because of the extra oxygen vacancies in the absence of the strong oxide of the electrode metal, less power would be needed to form the oxygen-vacancy filament. This mild forming of the conductive filament is expected to provide a higher R_{LRS} and is attributed as the reason for such observations in other reports. Ta showed the highest R_{LRS} among the four electrode materials, and it was the most adequate among the four TE materials for the realization of the soft switching used in analog switching operation.

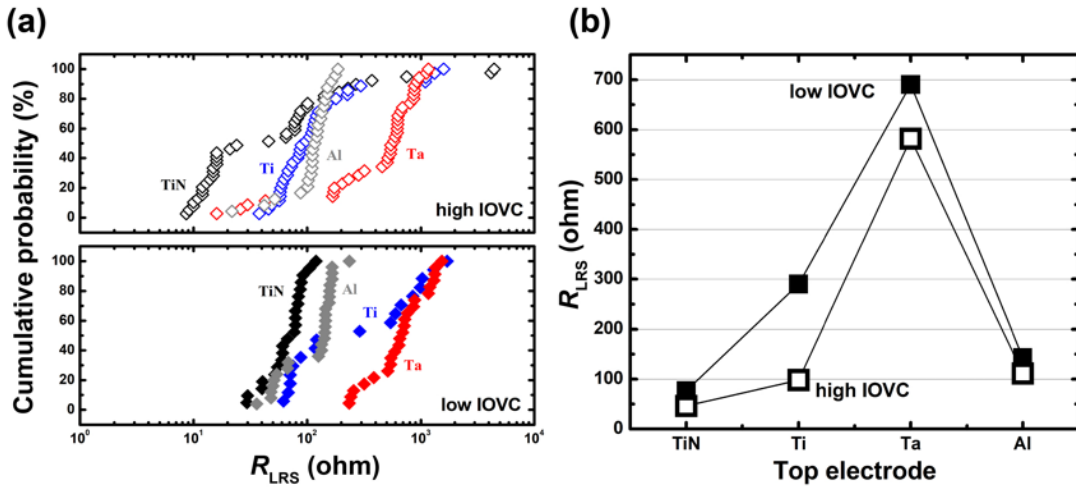


Figure 4-6. (a) Cumulative graph of measured R_{LRS} of more than 15 devices on the same chip and (b) the median values in (a). © Copyright (2021) The Japan Society of Applied Physics

4.4. The TEM and EDX analyses

In addition to the introduction of oxygen vacancies in the $\text{Ta}_2\text{O}_{5-\delta}$ switching layer, the oxidation of the TE metals is also an important factor for device performance. In this regard, STEM-EDS analyses were performed to investigate the metal-insulator pristine states. Clear intermixing between TE metals and $\text{Ta}_2\text{O}_{5-\delta}$ was not seen, which may also influence R_{ini} and V_{Form} . Examples of the element maps are shown in figure 4-7 for the TiN, Ta, and Al-0% devices. In the maps, only tantalum (red) and oxygen (green) are superposed to reduce complexity. In the TiN device, there was no clear interlayer, as expected. In the Ta device, clear modulation at the interface could not be observed as well, which does not indicate a lack of scavenging effect. Because the metal elements of the electrode and the oxide are the same in this case, making a distinction between the oxidized Ta TE and the reduced Ta oxide is quite difficult. While a clear indication could not be observed in this EDS map, the scavenging effect must occur, as expected from the electrical measurements. However, in the Al device, a green layer of oxygen without Ta could be observed, and the layer was ~ 3 nm thick. In this region, the Al signals were clearly identified and the formation of aluminum oxide at the interface was confirmed, which supports the earlier expect. Modulation of the oxygen content in $\text{Ta}_2\text{O}_{5-\delta}$ was not clearly detected in all cases. This means that the reduction of oxygen from $\text{Ta}_2\text{O}_{5-\delta}$ was small.

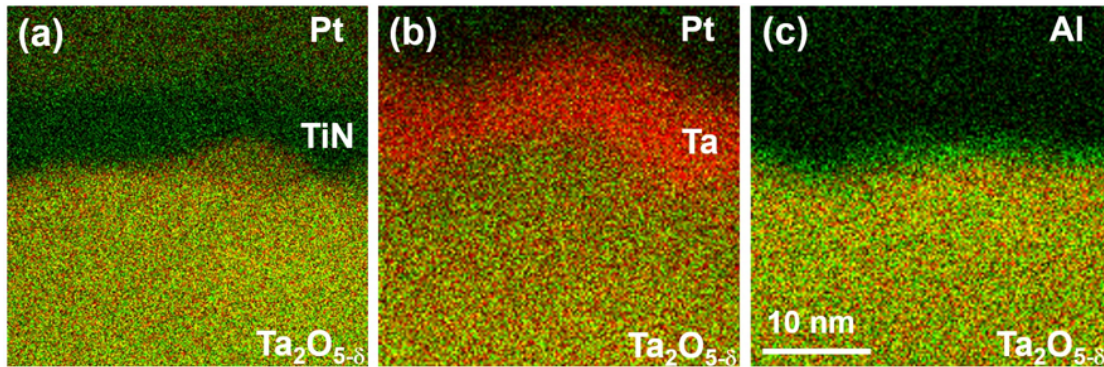


Figure 4-7. EDS mapping results for (a) TiN-0%, (b) Ta-0% and (c) Al-0% devices. Oxygen is colored green, tantalum is colored red. An oxygen-rich area existed at the interface in (c) for Al-TE while there is such an area in (a) for TiN-TE. © Copyright (2021) The Japan Society of Applied Physics

Here, I briefly discuss about the high V_{Form} of the Al devices. The bright-field STEM images of the Al/Ta₂O_{5- δ} interface before or after EDS mapping are compared in figure 4-8. The sample was Pt/Al/Ta₂O_{5- δ} deposited directly on SiO₂/Si without the TiN BE to form a flat interface. As discussed above, there was a thin Al₂O₃ layer at the interface in the pristine sample in figure 4-8(a). Figure 4-8(b) is the STEM image after EDS mapping ($100 \times 100 \text{ nm}^2$) for about 15 minutes. The Al₂O₃ layer became thick. Afterwards, additional EDS mapping for about 15 minutes was performed in the region of figure 4-8(b) ($20 \times 20 \text{ nm}^2$), and the interfacial region was observed under a low magnification as shown in figure 4-8(c). The corresponding part of the Al₂O₃ layer (center) swelled while it was kept thin in the other region. During this process, the sample was continuously irradiated by the electron beam, and the microstructure of the interfacial region changed. While the influence by the electron beam should contain many factors like ejection of oxygen from Ta₂O_{5- δ} , temperature increase is one of the major factors which must enhance the scavenging effect by Al as well as oxygen vacancy diffusion in Al₂O₃. The Al TE could get further oxygen from Ta₂O_{5- δ} , and the Al₂O₃ layer became thick. Based on this phenomenon, another possible reason of high V_{Form} for Al-device can be discussed. By the gradual increase of current before forming, the Joule heat is generated in the local region of the device, and the temperature are locally increased. This enhances the scavenging effect of Al, and thus the Al₂O₃ swells. This is a possible scenario giving the high V_{Form} for Al devices. The forming power was so strong that a huge pit was even be created by the forming as shown in figure 4-9. This phenomenon caused by local Joule heat may make it complicate to compose the first stage of memory structure, which plays an important role in following switching characteristics.

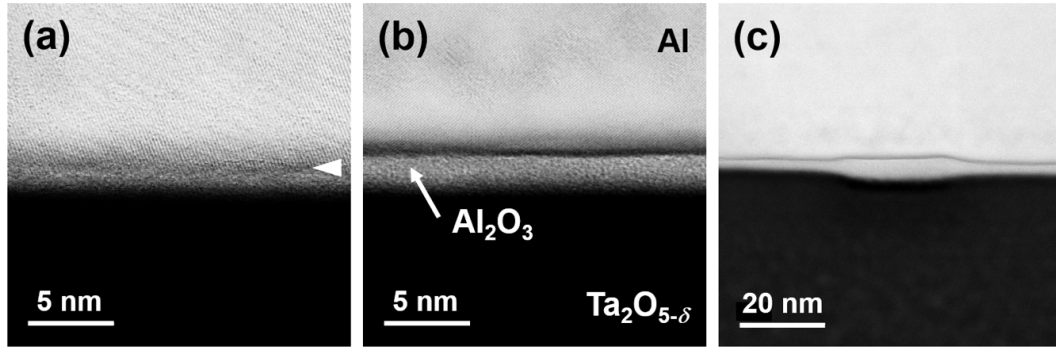


Figure 4-8. The Al_2O_3 layer formed at the interface. The sample was $\text{Pt}/\text{Al}/\text{Ta}_2\text{O}_{5-\delta}$ deposited directly on a SiO_2/Si to form a flat interface, where the number in parentheses are thickness in nm. The $\text{Ta}_2\text{O}_{5-\delta}$ was prepared in 50% f_{depo} . Bright-field STEM images of (a) the as-deposited sample, and after (b) the 1st and (c) after the 2nd EDS mapping. The dark line (arrow) in (a) were Ga segregation at the $\text{Al}/\text{Al}_2\text{O}_3$ interface injected by Ga-ion beam for the FIB processing, which could be used as the marker to identify the $\text{Al}/\text{Al}_2\text{O}_3$ interface. By electron beam irradiation for EDS mapping, the Al_2O_3 layer swelled. © Copyright (2021) The Japan Society of Applied Physics

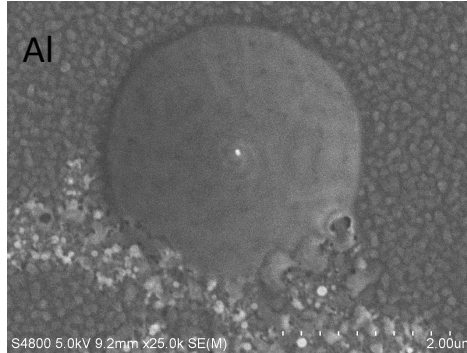


Figure 4-9. An example of the pit randomly appearing on the surface of the Al devices. The bright dot in the middle of the pit can be considered as the main filament. The substances on the bottom-left are aluminum burst during the high-power forming. Every measured Al device had similar pit at the surface.

For more careful STEM observations, the flat interfaces were prepared by deposition of $\text{TE}/\text{Ta}_2\text{O}_{5-\delta}$ directly on SiO_2/Si substrates. Thickness of these layers were 80 – 120 nm. Figure 4-10 shows an example of such device. Without insertion of the TiN bottom electrode having a rough surface, a flat interface between Al and $\text{Ta}_2\text{O}_{5-\delta}$ is clearly identified.

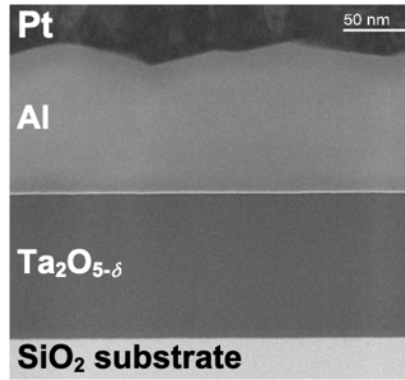


Figure 4-10. Cross-sectional bright-field STEM image of Al-0% sample.

The EDS line profiles from TEs to the SiO_2 substrate are summarized in figure 4-11 for 0%-devices with (a) TiN, (b) Ti, (c) Ta and (d) Al layers. The intensity is normalized in each component where the maximum value is set to be 100. Ta and O signals are drawn with black and red curves, respectively. Other metal elements (Ti and Al) are drawn with grey curves while N is green. Here, we should be careful that the spike-like Al signal in figure 4-11(d) is an artifact by Ga ion irradiation in the FIB process for STEM sample preparation [20], where Ga was injected in the metal Al layer (but not in the Al oxide layer) and the Al signal was reduced. Comparing these graphs, two characteristic features can be identified.

The first one is the formation of oxide layer at the interface. Focusing on figure 4-11(d) for Al, oxygen signal intruded into the Al layer from $\text{Ta}_2\text{O}_{5-\delta}$ while there was no such indication in figures 4-11(a) and (b) for TiN and Ti. This result using very flat interface support well the discussion using figure 4-7. The second point is the gradient of oxygen content in the $\text{Ta}_2\text{O}_{5-\delta}$ seen in figure 4-11(c) for Ta. In other cases, this phenomenon is not clear. In the case of Al, the Al electrode cannot be oxidized further when the Al_2O_3 thin layer is formed at the interface. In the case of Ta, on the other hand, the oxide layer formed at the interface is $\text{Ta}_2\text{O}_{5-\delta}$, and oxygen can penetrate through this layer without diminishing the scavenging effect by Ta. This must be the origin of this oxygen gradient inducing gradual change in resistivity of $\text{Ta}_2\text{O}_{5-\delta}$ and realizing the soft forming.

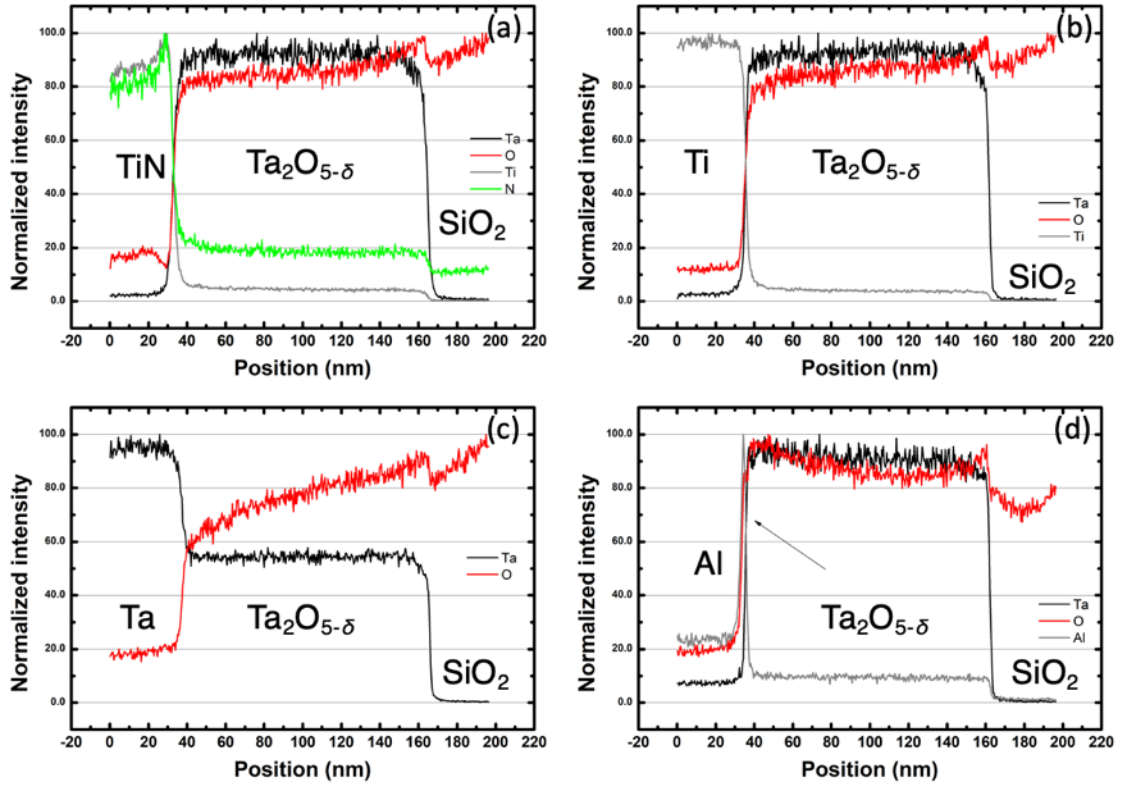


Figure 4-11. Line profiles of the EDS results of four 0% flat devices.

4.5. Conclusions

In this part, the electrical characteristics of the pristine $\text{Ta}_2\text{O}_{5-\delta}$ resistive memory was investigated comparing four electrode metals deposited on two types $\text{Ta}_2\text{O}_{5-\delta}$ layers having different IOVC. The R_{ini} of low IOVC samples was larger than that of high IOVCs as expected. For both types $\text{Ta}_2\text{O}_{5-\delta}$ layers, its sequence was $\text{TiN} > \text{Ta} > \text{Ti} > \text{Al}$. This result via the scavenging effect of metal electrodes can be explained based on their oxidation energies as previously proposed. However, R_{ini} reduction was much larger in high IOVC samples than the low IOVCs. This may indicate that the diffusion rate of oxygen vacancies in the $\text{Ta}_2\text{O}_{5-\delta}$ layer having high IOVC is large and that the scavenged region spread widely. Combinations of the intrinsic and extrinsic oxygen vacancies is an important factor influencing the pristine state (and thus the memory operation). The high IOVC sample had larger V_{Form} than the low IOVCs as expected from R_{ini} difference. However, the electrode dependence of V_{Form} showed different tendency from R_{ini} ; $\text{TiN} \sim \text{Al} > \text{Ta} > \text{Ti}$. While the sequence of $\text{TiN} > \text{Ta} > \text{Ti}$ can be explained based on the strength of the scavenging effect expected from the oxidation energy, the high V_{Form} value of Al

cannot be explained only by the quality of $\text{Ta}_2\text{O}_{5-\delta}$. Clear formation of an Al oxide layer (probably Al_2O_3) at the electrode/ $\text{Ta}_2\text{O}_{5-\delta}$ interface was detected in STEM-EDS analyses, and this can be a reason of high V_{Form} . In addition, possible growth of this insulating layer with the help of Joule heat in the forming process can be another origin of high V_{Form} despite of its low R_{ini} . High V_{Form} induces high power forming which generates thick filaments giving low R_{LRS} . However, the sequence of R_{LRS} was $\text{Ta} > \text{Ti} > \text{Al} > \text{TiN}$. Among them, Ta-device had exceptionally large R_{LRS} . The structure around the electrode/ $\text{Ta}_2\text{O}_{5-\delta}$ interface may contribute also to this phenomenon. Ta electrode near the interface is oxidized by getting oxygen from $\text{Ta}_2\text{O}_{5-\delta}$ and generate a region with gradual change in resistivity. This expectation induces inhomogeneous electric field, and thus forming occurs gradually place by place without abrupt power injection. This gives a soft forming resulting in large R_{LRS} .

4.6. Relating to the next part...

As described above, selection of electrode metals combined with intrinsic quality of $\text{Ta}_2\text{O}_{5-\delta}$ is a key factor to control the pristine characteristics. Among the 4 metals tested in this work, Ta-devices showed a gradual scavenging behavior that formed a gradient of oxygen vacancy. This unique property of Ta- Ta_2O_5 system should give the devices distinguishable switching behavior than other systems. In the next part of study (Chapter 5), using miniaturized devices by lithography and reactive ion etching (RIE) processes, the memory operation (especially analog operation) of the Ta-device (VCM) will be discussed, comparing with the Cu-device (ECM). For further discussion, the VCM devices with Ti and Al electrodes will be briefly discussed.

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Chapter 5 Initial states and switching capabilities

5.1.Introduction

In Chapter 4, the pristine state and device initialization (i.e. forming) were investigated using relatively thick $\text{Ta}_2\text{O}_{5-\delta}$. In the experiments there, a high current compliance of 20 mA was used to achieve forming for all devices, and the forming process frequently induced eternal hard breakdown without further switching operation. In this chapter, subsequent memory operation after forming with adequate current compliance will be discussed using miniaturized devices fabricated by photolithography and RIE (reactive ion etching) processes. The Ta-devices (VCM) with different insulator thicknesses and ambient conditions are compared with other electrode metals combined with the $\text{Ta}_2\text{O}_{5-\delta}$ insulator.

As described in section 1.3, the resistance changes are the consequence of the formation and rupture of conductive filaments in the insulator layer [1-4]. In two major resistive switching modes called VCM and ECM, the conductive filaments are formed with oxygen vacancies and (electrochemically active) electrode metal like Cu, respectively. Because of this difference, VCM and ECM may have different switching characteristics which are important information for further development of the memory applications. In this chapter, Ta-devices (VCM) and Cu-devices (ECM) are firstly compared with the aspect of the pristine state as discussed in chapter 4. Afterwards, their memory operations, especially the analog switching characteristics, will be discussed in detail. At the end of this chapter, switching characteristics of other VCM devices with Ti or Al electrodes will be briefly discussed.

5.2.Device fabrications and measurement

5.2.1.Fabrications

As shown in figure 5-1(a), Ta/ $\text{Ta}_2\text{O}_{5-\delta}$ /TiN and Cu/ $\text{Ta}_2\text{O}_{5-\delta}$ /TiN samples were formed vertically in VIA holes ($\varphi = 8 \mu\text{m}$) on SiO_2/Si substrates, which were patterned by photolithography and RIE. One example of the device is shown in figure 5-1(b), and the cross-sectional shapes can be identified with figure 3-4(a). Deposition conditions of the thin films were kept the same as in chapter 4.

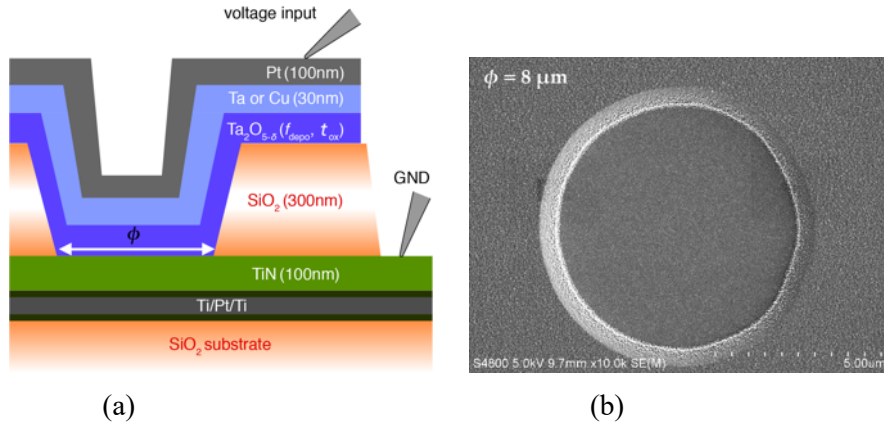


Figure 5-1. (a) Schematic cross-sectional image of fabricated devices. (b) SEM image of one of the samples observed from the upside. The cross-sectional image can be seen in figure 3-4. © Copyright (2020) The Japan Society of Applied Physics

The formation conditions of the Ta₂O_{5-δ} insulator were modified as shown in Table I. Here, three sets of devices with different insulator thicknesses (t_{ox}) of 7, 10, and 20 nm by modulating the duration of deposition. Thinner film conditions were added apart from chapter 4 for the detailed comparison. Each set were prepared under three different oxygen gas flow ratio, $f_{\text{depo}} = f_{\text{O}_2}/(f_{\text{Ar}} + f_{\text{O}_2})$, of $f_{\text{depo}} = 0, 0.2$, and 0.5 to modulate the intrinsic oxygen vacancy concentration (IOVC) in the insulator to high, medium and low levels, respectively. Here, f_{Ar} and f_{O_2} are the flow rates of Ar and O₂ gasses during the sputter deposition. In this part of experiments, the medium level of IOVC was added because the condition can provide extra information on the OV influences and device qualities as well. The duration of deposition was changed to modulate the insulator thickness (t_{ox}) to 7, 10, and 20 nm. Thinner film conditions were added apart from chapter 4 for the detailed comparison. The combination of outcoming condition modifications of f_{depo} and t_{ox} can be considered as insulator formation matrix containing ‘Comb. I’ to ‘Comb. IX’. Both kinds of top electrode were combined with the same insulator matrix, and therefore, 18 conditioned devices were fabricated for the VCM and ECM comparison. Ti and Al electrodes were combined only to 10-nm insulators and yield 6 different conditions ($t_{\text{ox}} = 10\text{nm}$). To reveal credible initial state, the insulator and top electrode were consecutively deposited.

Table I. Insulator fabrication matrix

Initial oxygen-vacancy concentration (IOVC)				
		$f_{\text{depo}} = 0$ High	$f_{\text{depo}} = 0.2$ Medium	$f_{\text{depo}} = 0.5$ Low
Thickness (nm)	7	Comb. I	Comb. II	Comb. III
	10	Comb. IV	Comb. V	Comb. VI
	20	Comb. VII	Comb. VIII	Comb. IX

Additionally, the pristine insulator environments were judged by using symmetrical double inert electrodes: TiN (50 nm)/Ta₂O_{5- δ} (10 nm)/TiN (50 nm) structures in the same 8- μ m VIA holes, where two conditions of $f_{\text{depo}} = 0$ and 0.2 conditions were used to fabricate the insulators.

5.2.2. Measurements

- **Basic characteristics**

All measurements were performed by I - V sweeps and more than 10 devices were measured for each fabrication condition. Here, the top electrode was biased while the TiN bottom electrode was grounded. The initial resistance (R_{ini}) was evaluated at ± 20 mV just after the fabrication, which was considered the pristine state. Afterwards, initializations were performed following the flowchart shown in figure 5-2(a). According to Rini, two branches of processes were performed to initialize the devices. The forming-reset operation process was applied to the devices with $R_{\text{ini}} > 1$ k Ω , which was considered as HRS-start, and the result can be categorized as “Switching” or “Reset failure” according to the capability of reset.

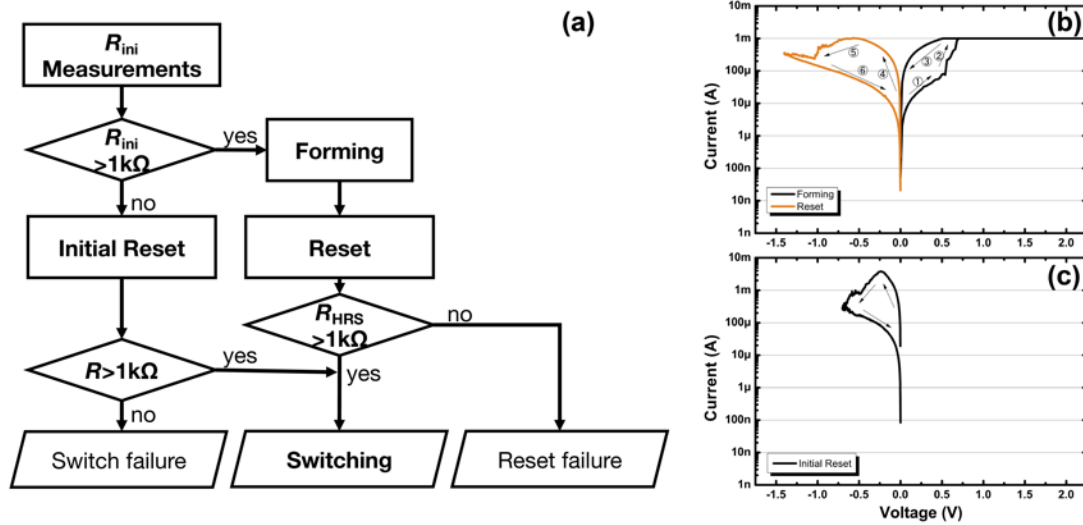


Figure 5-2. (a) Flow chart of initialization: initial-Forming or initial-reset were performed according to the initial resistance. The switching capabilities were categorized as “Switch failure”, “Reset failure”, or “Switching”. (b) Successful initialization on an HRS-start device with a Forming-Reset operation. (c) Successful initialization on an LRS-start device with an initial-Reset operation. © Copyright (2020) The Japan Society of Applied Physics

For example, figure 5-2(b) shows an example of a successful forming-reset initialization of an HRS-start device that can be categorized as “Switching”. Here, forming operations for all devices in this category were performed using the same compliance current of 1 mA to unify the condition before reset operations. On the other hand, initial-reset was performed on an LRS-start device if R_{ini} was less than 1 k Ω , which was also categorized as “Switching” or “Switch failure” according to the capability of reset. Figure 5-2(c) presents a successful reset initialization categorized as “Switching”. In both forming-reset and initial-reset cases, the HRS resistance after reset (R_{HRS}) should be higher than 1 k Ω to be categorized as “Switching” in this work. The devices satisfying this condition was classified as functional devices surviving in the initialization. The analog switching behaviors were evaluated only with these devices that were categorized to “Switching”. The analog operations were performed on the negative side of switching (reset) after switching the device to LRS (set), using multiple reset sweeps that had gradually increased maximum values (analog-reset).

- **The analog switching operations**

As reviewed in chapter 1, analog switching operations broke up the switching behaviors and several resistance states revealed. The measurement used in this chapter mainly was I - V sweep. The analog behaviors were realized on the Reset side. Further analog switching on the Set side will be discussed in chapter 6. The measurement method is schematically illustrated in figure 5-3. Set process was applied on the device to switch from the HRS to the LRS with steep resistance change. On the other hand, because of the gradual current change, the resistance change in Reset can be divided into several steps. The resistance states between the LRS and HRS are referred as the MRS in this work. The measurement was thought similar to the method proposed by Ref. 1-2 [Simmons (1967)], as shown in figure 1-1. Specifically, the MRS can be achieved by the I - V sweeps with gradually increased maximum negative voltage ($-V_{\max}$). As shown in figure 5-3, firstly sweep with $-V_{\max} = -V_{\text{reset1}}$ applied to the device gives the R_{MRS1} . Through subsequent I - V sweeps with the $-V_{\max}$ from $-V_{\text{reset2}}$ to $-V_{\text{reset5}}$, multiple resistance states can be achieved. This functional switching capabilities had been tested after the aforementioned basic characterization.

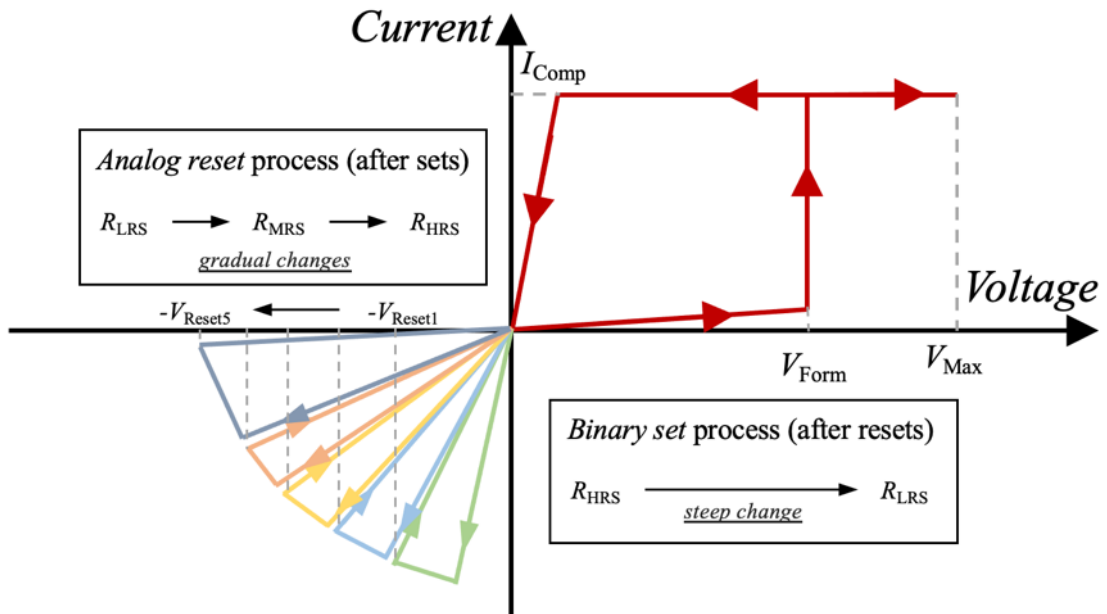


Figure 5-3. Schematic process of the analog manipulation used in this part of study.

5.3. Brief confirmation of analog operation

Prior to detailed discussion of device properties, the analog operation observed in Ta and Cu devices are briefly demonstrated. Typical operations are summarized in figure 5-4. The results of a Ta-device prepared with $f_{\text{depo}} = 0.5$ and $t_{\text{ox}} = 10$ nm are shown in figures 5-4 (a)-(c) while those of a Cu-device with $f_{\text{depo}} = 0$ and $t_{\text{ox}} = 7$ nm are in figures 5-4 (d)-(f). As clearly observed in the I - V sweeps of the devices, figures 5-4 (a) and (d), both devices showed steep set behaviors and gentle reset behaviors. Therefore, the reset process could be separated by the stepwise analog-reset described above as shown in figures 5-4 (b) and (e), and gradual increase of R_{MRS} could be achieved as identified in figures 5-4 (c) and (f). While the analog operation could be achieved in both cases, their controllability seems different from each other. In the following sections, systematically fabricated devices will be discussed with the aspect of the initial state and switching capability. Afterwards, analog capability and evolution between stepwise R_{MRS} stages will be discussed.

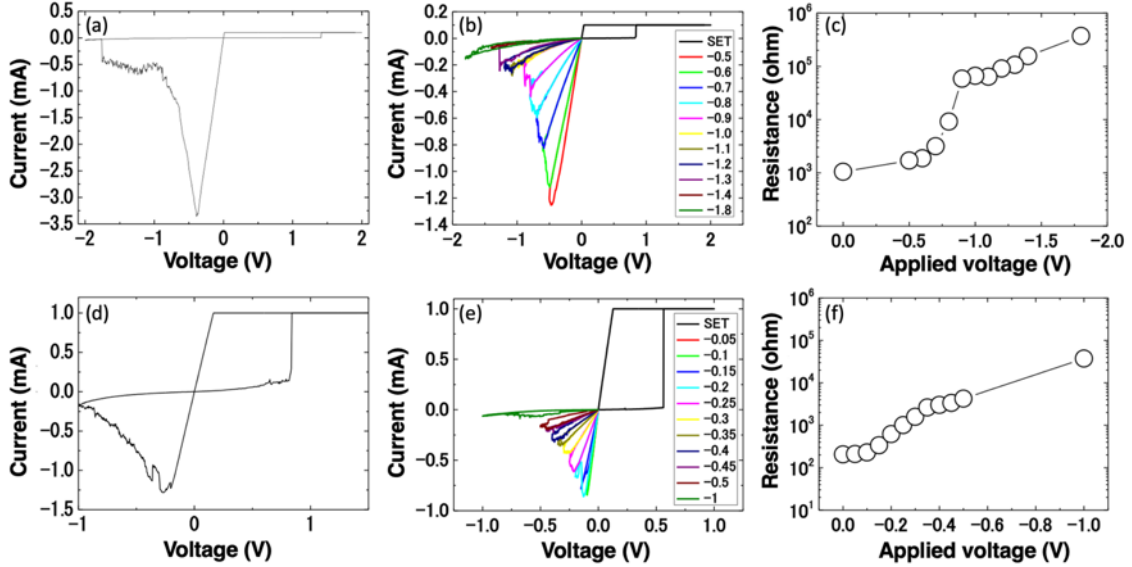


Figure 5-4. (a)-(c) Basic switching behaviors and analog switching behaviors of one Ta device. (d)-(f) Basic switching behaviors and analog switching behaviors of one Cu device.

5.4. Initial states of Ta and Cu devices

5.4.1. Initial resistance

The initial resistances (R_{ini}) before any switching operations are important indicators according to the nanomaterials including the scavenging and diffusing behaviors as discussed in chapter 4. At first step of the research using miniaturized devices, the initial resistance R_{ini} are discussed to compare characteristics of VCM and ECM. The R_{ini} results measured for Ta and Cu devices are shown in figure 5-5(a) and figure 5-5(b). t_{ox} and f_{depo} clearly affected the R_{ini} of the two types of devices in different ways. The Ta devices showed rapid increases of R_{ini} with higher t_{ox} and f_{depo} . It was predictable that the increase of the partial pressure of oxygen in the sputtering ambient during the insulator formation reduced the oxygen-vacancy concentration and increased the initial resistance of the insulators that like chapter 4. Additionally, thicker insulator yielded the full scavenging phenomena. Extra oxygen vacancies possibly formed at the top of the insulator because LRS-start did not appear in the thick insulator devices. By comparing the three groups of devices with $f_{depo} = 0, 0.2, 0.5$, the R_{ini} increased for different orders by t_{ox} that suggested the scavenging was greater with higher IOVC. In the other words, comparing the devices with high IOVC and low IOVC, R_{ini} increased from about 100Ω to about $500M\Omega$ for high IOVC. For the devices with $f_{depo} = 0.5$, R_{ini} only increased for 2.5 orders by increasing the same amount of thickness. The results in figure 5-5(a) also suggested that the scavenging range and should be approximately 10 nm because two 7-nm devices had extremely low R_{ini} results (LRS-start), and by just increasing the t_{ox} for 3 nm, ‘Comb. IV’ increased for more than 3 orders (HRS-start). On the other hand, more complicated tendencies appeared in the ECM devices, as summarized in figure 5-5(b). The IOVC affected the diffusion coefficient non-monotonously. The lowest R_{ini} existed at the medium IOVC, suggesting that the Cu-ion diffusion at that condition was enhanced. The fact that R_{ini} increased at both sides of the low and high IOVC region indicates that the appropriate IOVC also enhanced the diffusion but that too much IOVC clearly suppressed it. The overall lower R_{ini} of ECM devices than that of VCM devices implies that the diffusion constants and/or concentration of diffused Cu ions were higher than those of oxygen vacancies.

As TiN inert electrode had highest R_{ini} as discussed in chapter 4. Symmetric TiN structure is like to be a good reference to Ta and Cu. The TiN samples showed similar increment with higher f_{depo} like VCM devices, shown in figure 5-5(c), which again confirmed that f_{depo} modulations altered the local oxygen-vacancy concentration. Both Ta and Cu devices showed much lower R_{ini} than TiN samples probably because of the scavenging and diffusing behaviors. It is interesting that both models are likely to have notable interactions at the metal/insulator interfaces that may cause dissimilarities from the intended fabrication, which is an unneglectable aspect to the individual switching behavior.

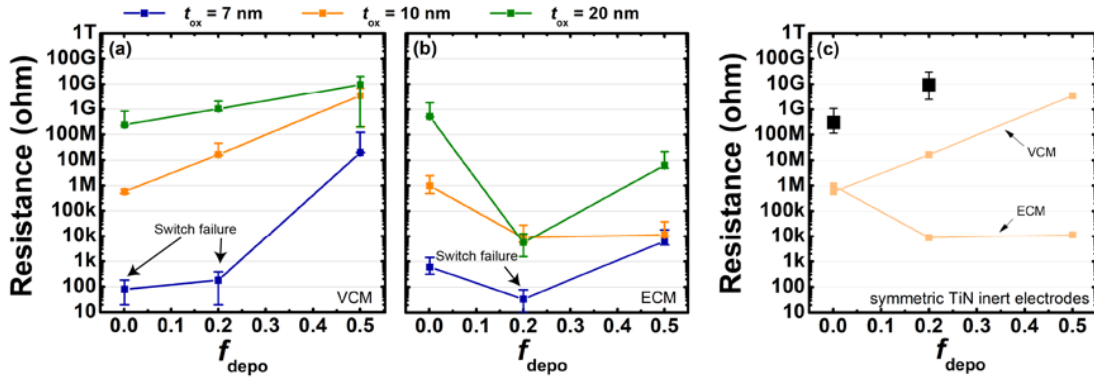


Figure 5-5. R_{ini} dependence on f_{depo} for (a) VCM (Ta top electrode) and (b) ECM (Cu top electrode). (c) Two 10-nm devices of double TiN-electrode with $f_{\text{depo}} = 0$ and 0.2, the same R_{ini} at the same t_{ox} conditions of VCM and ECM were drawn as light orange for direct comparisons. The solid blocks are the average values, and the error bars represent the distributions of the results of multiple devices. Additionally, $>100\text{G}\Omega$ results were shown with symmetric TiN-top-electrode device fabricated with the conditions of 10nm-50%. Although the results are not shown because of the limitations of the measurement equipment, the increase of R_{ini} can be considered an agreement to the discussion. © Copyright (2020) The Japan Society of Applied Physics

5.4.2. Switching capabilities and conduction mechanism

Initializations were performed to categorize the switching capability, and the results are summarized in Table II and Table III, respectively. It was clarified that “Switching”, “Switch failure”, and “Reset failure” were distributed differently for VCM and ECM devices.

Two types of failure were confirmed in the Ta devices. ‘Comb. I’ and ‘Comb. II’ in the thin insulator regions did not show any switching behaviors (“Switch failure” in Table II), and the devices remained in the LRS possibly because of the filament-like substance formed by the high

degree scavenging of oxygen that could not be retracted. Reset operations on ‘Comb. VIII’ and ‘Comb. IX’ devices failed after Forming sweeps (“Reset failure” in Table II). These results are considered hard breakdowns. Figure 5-6(a) presents the representative initialization results of 10-nm Ta devices, and the forming voltages increased with higher R_{ini} and lower IOVC. These results confirm that the higher R_{ini} induced by the combinations of IOVC or t_{ox} involves higher formation voltage [3,4]. Appropriate R_{ini} conditions are needed for formations and ruptures of conductive filaments. Well-modified t_{ox} and f_{depo} can avoid unrecoverable initial scavenging of the oxygen and hard breakdowns. Additionally, 1 M Ω –1 G Ω is likely the appropriate range for the appearance of VCM switching capability. On the other hand, initializations were successfully performed on most of the ECM devices. ‘Comb. II’ could not be switched to HRS possibly because of the extremely low R_{ini} induced by over-enhanced initial Cu-ion diffusion. However, an initial-Reset was successfully applied to ‘Comb. I’ device, and it recovered to HRS. Despite the thicker insulator layers used in ‘Comb. VIII’ and ‘Comb. IX’, they both exhibited successful switching capabilities apart from VCM devices, which suggests that weakened insulation or low R_{ini} induced by the initial Cu-ion diffusion prevent hard breakdowns.

Table II. Resistive switching categories for VCM devices

		Initial oxygen-vacancy concentration (IOVC)		
		High	Medium	Low
Thickness (nm)	7	<u>Switch failure</u> ^{1,2}	<u>Switch failure</u> ^{1,2}	Switching
	10	Switching	Switching	Switching
	20	Switching	Reset failure ²	Reset failure ²

Table III. Resistive switching categories for ECM devices

		Initial oxygen-vacancy concentration (IOVC)		
		High	Medium	Low
Thickness (nm)	7	<u>Switching</u> ¹	<u>Switch failure</u> ¹	Switching
	10	Switching	Switching	Switching
	20	Switching	Switching	Switching

¹ The underlining in tables 2 and 3 indicates devices with LRS-start.

² See the two types of failures in supplementary materials figure A-4.

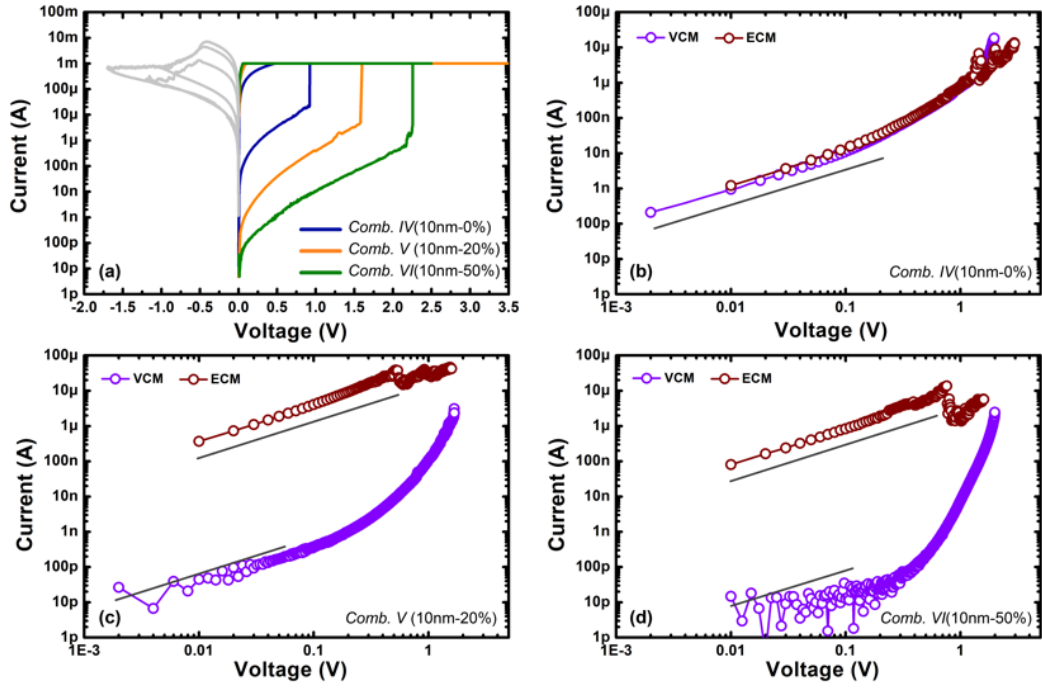


Figure 5-6. (a) Forming-Reset results for ‘Comb. IV’ to ‘Comb. VI’ of Ta devices. (b)–(d) I–V curves of initial-forming of Ta and Cu devices shown in log–log plot for (b) ‘Comb. VII’, (c) ‘Comb. VIII’, and (d) ‘Comb. IX’. The black lines are the references of slope 1 of the ohmic conduction. © Copyright (2020) The Japan Society of Applied Physics

To investigate the initial states even further, the initial conductions in the low-voltage regions of the initial-Forming curves (the I - V curve partition before the abrupt current jumps) were compared using the partition by log–log graphs [5,6]. Because of the greater diffusions of the Cu device, 20-nm Ta and Cu devices were selected for reliable discussion. The forming processes of ‘Comb. VII’, ‘Comb. VIII’, and ‘Comb. IX’ are shown in figures 5-6(b), 5-6(c) and 5-6(d), respectively, where the initial conductions of the Ta and Cu are compared. As observed in figure 5-6(b), the initial conductions of the ‘Comb. VII’ devices were almost the same, which may imply that the initial scavenging of oxygen of the Ta electrode and the Cu-ion diffusion are similar for high IOVC conditions, because they both had huge R_{ini} drops from the TiN results. R_{ini} and the initial conductions being almost the same may be a coincidence; however, it was still an unexpected result that the scavenging depth and diffusion depth were similar under this condition. The decrease of IOVC also induced different I - V characteristics between the Ta and Cu devices. The ohmic conduction regions shrunk in the Ta device possibly because of the gradual formation

of oxygen vacancy filament, whereas ohmic conduction dominated most of the forming processes in the Cu devices. The ohmic conduction of the Cu devices for lower IOVC can be considered as the result of initial spontaneous Cu-ion diffusion during and after the top-electrode depositions.

The general higher V_{Form} shown in the Ta devices was much lower than the V_{Form} statistics obtained in chapter 4. The possible edge of the via holes may cause the thickness of the insulator to shrink locally as shown in figure 3-4(b).

5.4.3. Models of initial states

Here, schematic illustrations of the scavenging behaviors are shown in figure 5-7, specifically for the Ta and Cu devices. The initial scavenging of oxygen at Ta/ $\text{Ta}_2\text{O}_{5-\delta}$ interfaces and diffusion of Cu ions at Cu/ $\text{Ta}_2\text{O}_{5-\delta}$ interfaces played important roles in determining the initial resistances and switching capabilities. As described above, R_{ini} of the Ta device clearly indicated that the extra oxygen vacancies were formed at the top side of $\text{Ta}_2\text{O}_{5-\delta}$ layers and that they accelerated the resistance reduction. As another important phenomenon, it was clarified that the faster generation of oxygen vacancies at the interface and greater scavenging occurs as IOVC increased.

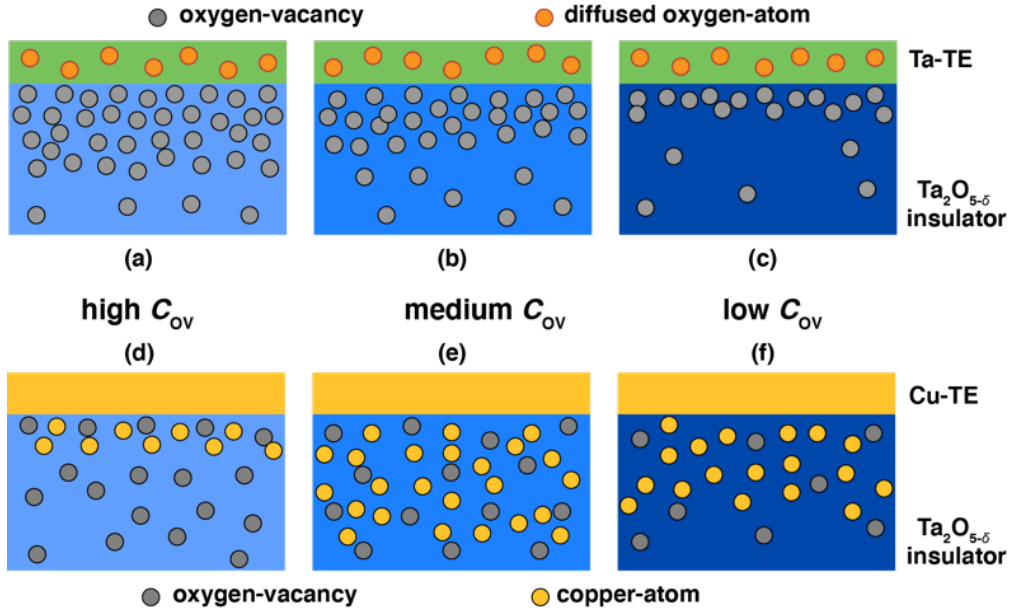


Figure 5-7. Schematic initial models of Ta and Cu devices. From left to right: $f_{\text{depo}} = 0, 0.2, 0.5$. (a)–(c) Redox reactions near the metal-insulator interface with different degrees. (d)–(f) Diffusion behaviors of Cu ions with different IOVC. Oxygen atoms are excluded for simplification of the ECM diffusion models because no evidence of scavenging behaviors was detected in the previous discussion. © Copyright (2020) The Japan Society of Applied Physics

Figures 5-7(a)–(c) present schematic illustrations of the initial distribution of oxygen vacancies at stable states for the VCM device. The regions containing much oxygen vacancies became thicker for higher IOVC. It should be noted that the scavenging depth is not that large (approximately 10 nm), which may explain why the thin oxide layers are generally applicable for VCM-type resistive switching memories [7-9]. The Cu-ion diffusion depth is greater than those of oxygen vacancies for the Ta devices, which resulted in the relatively lower R_{ini} . The most interesting result was that the Cu-ion diffusion constants seemly depended on IOVC because of the non-monotonic dependency on f_{depo} . Schematic illustrations of the initial distribution of Cu ions and oxygen vacancies of the Cu devices are presented in figures 5-7(d)–(f). Cu ions were deeply introduced in $Ta_2O_{5-\delta}$ layers for medium IOVC, resulting from the enhancement of diffusion. However, too much IOVC suppresses Cu diffusion as well.

5.5. Analog behaviors of four sets of devices

5.5.1. Ta top electrode

The analog capabilities were confirmed by using successfully initialized Ta devices and were measured by sweeping the voltage from 0 V to the positive direction (Set sweeps) and then to the negative voltage direction (stepwise reset sweep cycles; "analog-reset" operation called in this report). Figure 5-8(a) is a typical example of analog switching using a Ta-device in ‘Comb. I’. While a sharp resistance change was observed from HRS to LRS in the set sweep, gradual resistance manipulation was achieved by increasing negative stop voltages with the analog-reset operation. Notably, the Ta devices showed similar characteristics regardless of the fabrication conditions. This can be identified in figure 5-8(b) where set curves are superposed for five devices prepared under ‘Comb. III’ to ‘Comb. VII’ (the complete matrix of analog switching results is summarized in appendix). The set voltages were all approximately + 0.5 V, which were much lower than the forming voltage shown in figure 5-6(a). Despite some variations of the analog-reset curves, the switching shapes almost overlapped with each other. Moreover, the resistances after each reset operation as a function of the absolute negative stop voltage from – 0.2 to – 1.0 V are presented in figure 5-8(c), where the resistance changes are distributed over a small range. The gradual resistance changes at stop voltage sweeps lower than – 0.4 V clearly

indicates successful analog behaviors, where a resistance change of more than one order of magnitude can be achieved. The maximum analog resistance after reset was approximately 10 k Ω , which is a substantial drop from R_{ini} of at least two orders. Good reproducibility was also achieved in repetitive set-reset operations (see appendix).

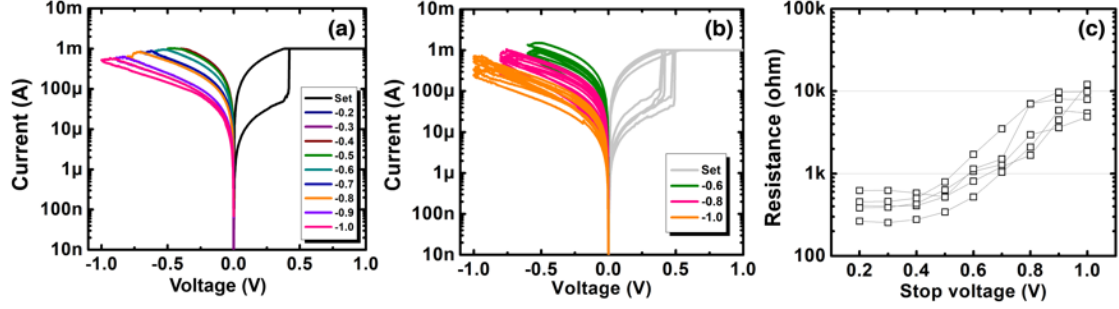


Figure 5-8. (a) An example of complete analog-reset switching behavior achieved by increasing the negative stop voltages from -0.2 to -1.0 V using ‘Comb. V’. (b) Analog switching behaviors of VCM using five successfully initialized devices of ‘Comb. III-VI’. For simplicity, only the curves for Sets and Reset curves with negative stop voltages of -0.6 , -0.8 , and -1.0 V are shown. (c) Analog resistance changes of the five devices. The absolute values were used for the x-axis in (c). © Copyright (2020) The Japan Society of Applied Physics

The similarities of the analog switching behaviors can be explained because of the initialization processes. Similar conduction paths with a current bottleneck ($I_{\text{comp}} = 1$ mA) were formed by the forming process regardless of the initial condition shown in the previous section. The current limits were lowered from 20 mA in the last chapter to 1 mA, where the lower value is considered good for the filament formation. Because the oxygen-vacancy filaments formed during the forming operations were too robust to be retracted completely, restrictions on increasing R_{HRS} are thought to exist for the following reset operations. As a result, similar analog resistance can be achieved because of the almost same current limiting path shape even though the total filament shapes might have variations. This phenomenon may simplify both fabrication processes and analog operations for future Ta devices.

5.5.2. Cu top electrode

Analog switching capabilities were also confirmed for all the successfully initialized Cu devices, as shown in figure. 5-9. Apart from the Ta devices, switching behavior variations were observed, which can be considered to result from the different t_{ox} and f_{depo} condition. Consecutive

cycling tests were also performed for 20-nm devices (see appendix), with the same finding that greater variations may have resulted from the $\text{Ta}_2\text{O}_{5-\delta}$ formation conditions. Specifically, thicker insulator layers (20 nm) induced distinguishable switching patterns apart from the 7-nm and 10-nm devices. Rapid and wide range resistance changes appeared in the 20-nm devices, and the final resistances were approximately three orders of magnitude higher than those of the 10-nm devices. The 7-nm and 10-nm devices tend to show VCM-like switching behaviors, which suggested that oxygen-vacancy may take effects at such thin insulator. In general, Cu devices had a wider range of analog switching than Ta devices. These individualities again confirm that oxygen vacancies in the ECM model not only affected the initial Cu-ion diffusion but also, as no newly formed oxygen vacancies were confirmed, the initial insulator conditions were able to maintain the original deliberate modulations for the formations and ruptures of Cu-ion filaments, which may be a significant feature to realize predictable stable switching.

With notably different characteristics of the Cu devices, gradual analog resistance changes of the three 20-nm devices are plotted as a function of negative stop voltage in figure 5-10. The devices with medium IOVC exhibited the lowest final resistance, whereas those with high and low IOVC provided comparably high final resistance. This dissimilarity might also be caused by the initial Cu-ion diffusion. For the medium IOVC devices, Cu ions diffused deeply into the insulator layer, which made it difficult to completely retract the diffused ions to achieve higher HRS. Nevertheless, the resistances obtained at the negative stop voltage of -1 V were still higher than R_{ini} , which may be realized by the retractions of Cu ions by the negative electric field because of the high diffusivity of Cu ions. Although the devices with low and high IOVC achieved higher HRS larger than $1 \text{ M}\Omega$, the resistances were much lower than R_{ini} , most likely because of the lower Cu-ion diffusivity in the insulators compared with that for the medium IOVC.

Despite the much higher R_{ini} of VCM devices, the overall maximum HRS was approximately $10 \text{ k}\Omega$ as discussed previously; the two Cu devices still exhibited much higher HRS than the Cu devices with the same voltage applied, which suggests intensive Forming processes of Ta device did not likely occur in Cu devices, so that Cu filament rupture relatively easily and completely than the Ta device in analog switching. Though maximum t_{ox} was set to 20 nm to compare the VCM and ECM models in this study, much thicker $\text{Ta}_2\text{O}_{5-\delta}$ films can achieve wider and higher

HRS resistances for ECM. The variabilities of the Cu devices analog switching behaviors suggest that the model involves a more complicated mechanism, and that production may be stricter to obtain desired performance, as higher resistance operations have profound possibilities to realize low chip power consumption by reducing the operating current. More accurate current controls, such as the integration with a transistor, and/or introduction of multi-insulator-layer structures may be needed to minimize the uncertainty of Cu devices.

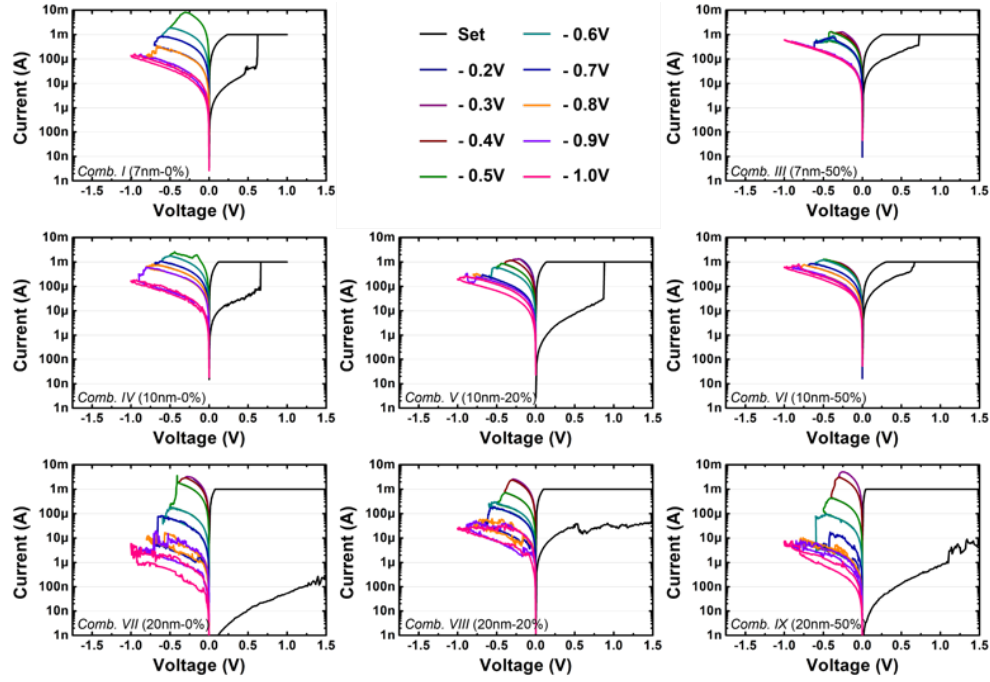


Figure 5-9. Analog switching results of successfully initialized Cu devices. Analog-Reset was applied by increasing the negative stop voltage to -1 V with an interval of -0.1 V. © Copyright (2020) The Japan Society of Applied Physics

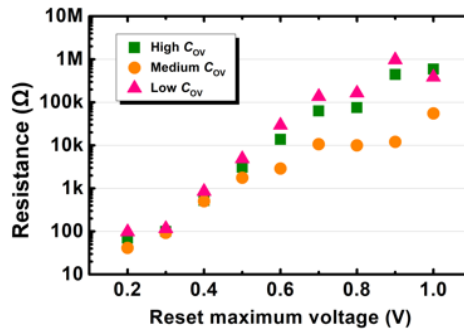


Figure 5-10. Analog switching resistance of three Cu devices as a function of negative stop voltages (shown as absolute values) for high, medium, and low levels of oxygen vacancy at $t_{\text{ox}} = 20$ nm. © Copyright (2020) The Japan Society of Applied Physics

5.5.3. Ti top electrode

In the following subsections, other sets of VCM devices with Ti (section 5.5.3) or Al (section 5.5.4) electrodes are briefly demonstrated comparing with the Ta-device. The devices having 10-nm- thick $\text{Ta}_2\text{O}_{5-\delta}$ were prepared also via photolithography patterning. Analog switching capabilities were confirmed on the three devices while notable long-term characteristic changes were found.

- **The analog capabilities**

As a scavenging electrode, Ti devices also showed successful analog switching behaviors as shown in figures 5-11(a), (b), and (c) for f_{depo} of 0%, 20% and 50%, respectively. The measurements were done after 2 hours from the deposition of the Ti electrode, clear multi-level resistance states can be observed. Figures 5-11 (b), (c) shows distinguishable analog behaviors that were different from the Ta and Cu devices. Only lower voltage was needed to achieve relatively high HRS for the conditions. And the V_{Form} was also higher than Ta. This may suggest the oxygen vacancy reactions were easier than Ta/ Ta_2O_5 systems. On the other hand, 0% device only showed a switching behavior that had a small window. Although the Ti is a scavenging electrode like Ta, the distinguishable characteristics were thought to due to the different movements of oxygen vacancies.

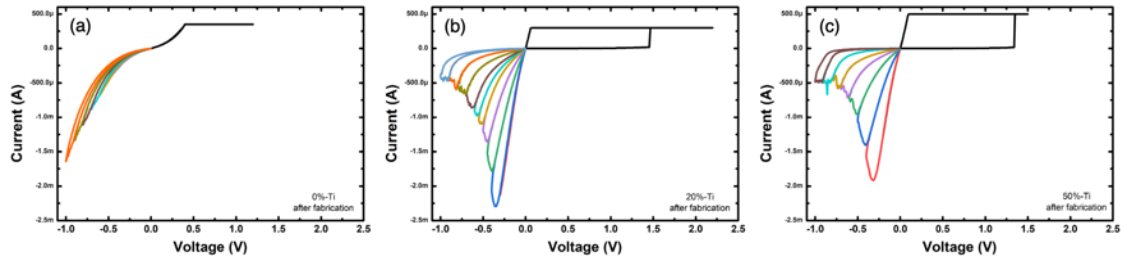


Figure 5-11. The analog behavior of the three Ti devices fabricated with the same conditions to the Ta and Cu devices. The t_{ox} was fixed to 10nm and f_{depo} was changed from 0% (a), 20% (b) and 50% (c). Clear analog behaviors were observed in the three devices with significant differences to the Ta and Cu devices.

- **The long-term characteristics**

Unlike the Ta scavenging electrode, Ti showed a clear time dependency on the characteristics. As shown in figure 5-12, the initial resistance was measured for a certain time of duration. In the intervals, the devices were kept in a dehumidified case at RT. The R_{ini} was slightly changed for

the 0% and 20% devices. Clear trend of decreasing R_{ini} was found in 50% device. This may suggest the electrode oxidation was much stronger in such oxygen-rich environment.

Although the R_{ini} of the 0% and 20% did not change significantly, the switching behaviors clearly degraded with time. As shown in figure 5-13, although the devices were able to show high R_{ini} after weeks of fabrication, the switching behaviors were much different. In figure 5-13(a)-(c), after weeks of fabrication, the analog switching windows were smaller despite they still show the switching capabilities. In figure 5-13(d)-(f), after 3 months of fabrication, all devices were not able to switch at all. We speculate the scavenging effect behaving strongly in the Ti/Ta₂O₅ system.

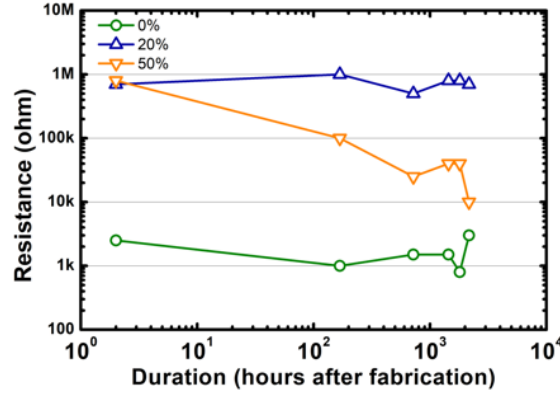


Figure 5-12. The long-term influence on the R_{ini} of fabricated device. Specific devices were excluded from analog behavior measurements and only used for the R_{ini} measurements.

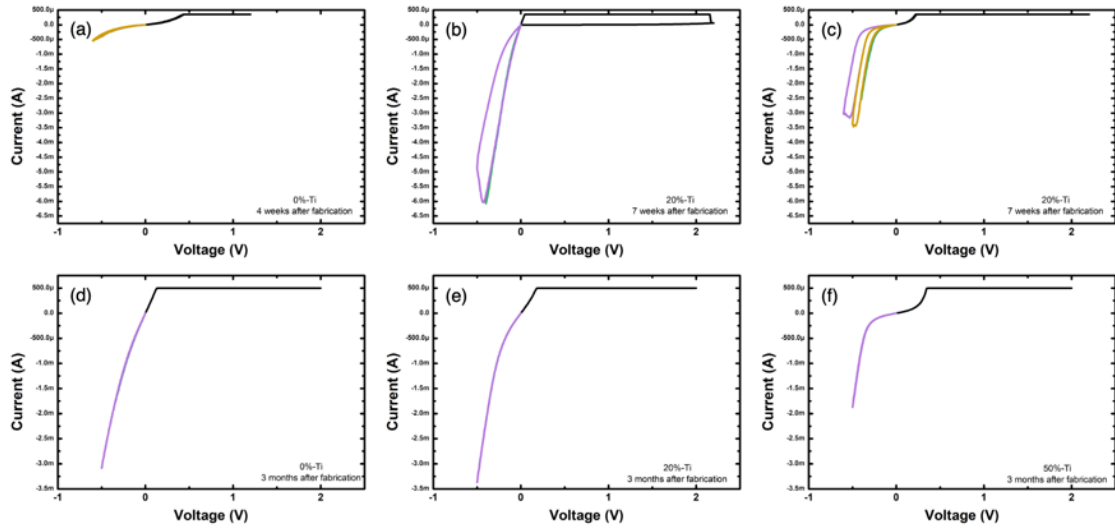


Figure 5-13. The long-term influence on the analog behaviors of fabricated Ti device. (a)-(c) shows the characteristics weeks after the fabrication. (d)-(f) show the characteristics 3 months after the fabrication.

5.5.4. Al top electrode

Al top electrode was also tested for the analog capabilities. As shown in figure 5-14 (a)-(c), three conditioned f_{depo} devices showed analog-like behaviors on the reset side. However, the switching windows were small, and the current changes were unstable. Although analog-like reset behavior occurred in the 20% device, the steep curve could not be applied for the functional analog behavior. As we discussed in the last part of chapter 4, the thickness of the Al_2O_3 interlayer might be altered by the Joule heat caused by the switching current. The characteristics shown here can be considered due to the reason. The unstable thickness change caused the current changes were in unstable states. On the other hand, long-term characteristics did not change much for the Al device as shown in figure 5-14(d)-(f).

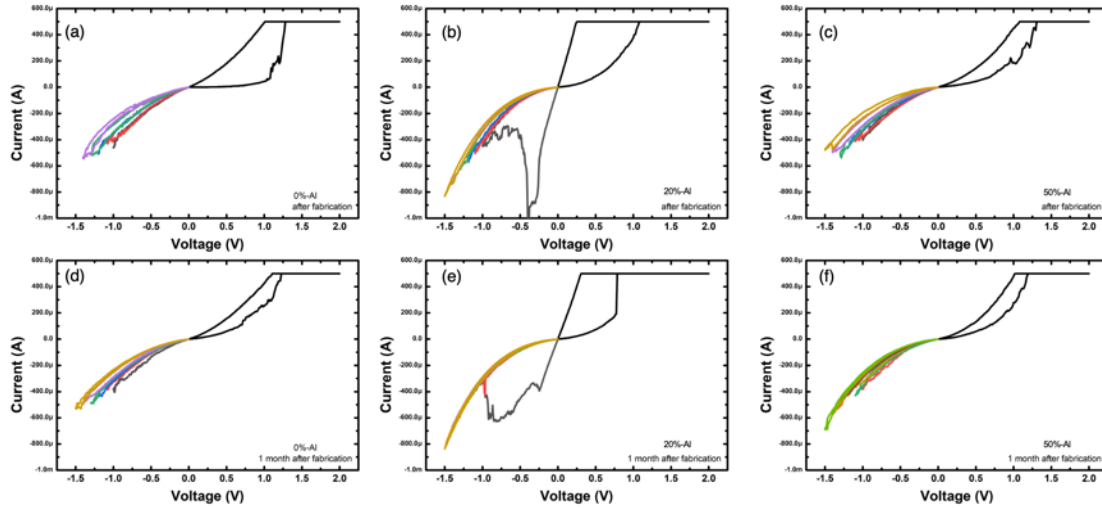


Figure 5-14. The long-term influence on the analog behaviors of fabricated Al device. (a)-(c) shows the characteristics right after the fabrication. (d)-(f) shows the characteristics 1 month after the fabrication.

5.6. Discussion

5.6.1. Intrinsic oxygen vacancy concentration (IOVC)

By using sophisticatedly fabricated device at nanometer scales, we can first discuss the IOVC that had been modified in chapter 4 and chapter 5 quantitatively. $\text{Ta}_2\text{O}_{5-\delta}$ layers (50 nm) were fabricated separately on silicon wafers with the three different IOVC used in this work and evaluated by X-ray photoelectron spectroscopy (XPS). The results were not distinguishable

among the different conditions. As shown in figure 5-5(b), symmetric $\text{TiN}/\text{Ta}_2\text{O}_{5-\delta}/\text{TiN}$ structures showed rapid resistance increment as the decrease of IOVC. In fact, literatures have reported that the tantalum suboxide resistivity has non-linear correlation with oxygen proportion [10, 11]. Results in ref. 11 can suggest converting the initial resistances shown in figure 5-5(c). The pristine IOVC in the symmetric structure can be roughly estimated to be on the orders of 10^{20} cm^{-3} ; $< 3.0 \times 10^{20} \text{ cm}^{-3}$ for high IOVC and $< 1.2 \times 10^{20} \text{ cm}^{-3}$ for medium IOVC, respectively. These estimations imply that the stoichiometric number realized in this work should in a range of $0 < \delta < 0.04$ in $\text{Ta}_2\text{O}_{5-\delta}$. The results indicate that the IOVC modulations during sputtering had only done delicate changes to the insulators, which may not to be identified by our XPS analysis, however, notably altered R_{ini} results were able to display the delicate film modulations.

5.6.2. The artificial synapse realizability

Here, the artificial synapse realizabilities of the fabricated device were briefly discussed. Bullet layout will be used for a clearer view.

◆ Cu top electrode

Advantages:

- No degradations during initialization.
- High realizability on the analog behavior.
- Relatively high HRS.

Disadvantages:

- The characteristics were unstable.
- Sensitive to the fabrication conditions.

◆ Ti top electrode

Advantages:

- Realizing the analog behavior with relatively high HRS.

Disadvantages:

- Long-term degradation.

◆ Al top electrode

Advantages:

- Realizing the analog behavior in limited condition.

Disadvantages:

- The current change was not stable.

◆ Ta top electrode

Advantages:

- Relatively high realizability on the analog behavior.
- Behavior similarities by the initializations.
- High controllability.

Disadvantages:

- Relatively low HRS.

As listed above, every electrode has distinguishable characteristics and has its own different advantages and disadvantages. Analog behavior was realized in all selected materials and for the practical applications, one should select the material combination carefully. In the next part of study, we selected Ta because its high controllability. The relatively low HRS was also expected to be solved by different film composition.

5.7. Conclusions

In this chapter, the analog behaviors using the same scavenging electrode materials in the last chapter were investigated. To give a comparison to typical VCM model, Cu as an ECM model was also tested. The respective initial states influenced the subsequent analog behaviors. For Ta-based VCM, analog characteristics can be only realized only with certain combinations of t_{ox} and f_{depo} . The initialization unified the functional devices into a similar switching window. For Cu-based ECM, analog characteristics were almost realized with entire matrix of device. The initialization was not modifying the following switching behaviors and devices showed unstable switching current despite of the higher HRS. For Ti-based VCM, analog behaviors were successfully fulfilled like we predicted. However, the long-term characterization showed spontaneous degradations to the devices. For Al-based VCM, analog-like behaviors were presented. The unstable current change was not considered to fulfill the requirement of an artificial synapse.

5.8. Relating to the next part...

In chapter 4 and chapter 5, a groundwork for predicting the switching capabilities was established. Three VCM scavenging electrodes and one ECM active electrode with two kinds of patterning methods were studied. Every electrode had unique advantages and disadvantages in the switching behaviors. Either unstable current or obvious degradation were found Ti, Al and Cu electrodes, which thought to be hard to overcome with the current device platform. Precise

current control by the transistors may be needed for the good characteristics. On the other hand, Ta showed fabrication independency on the analog behavior. In other words, being not too sensitive to the fabrication conditions, as long as the fabrication conditions were set in the right ranges, the analog behaviors could be realized. This particular property is perfectly adequate to the current ANN system. It could be very hard for one to unify the qualities of millions of memory device on one chip. Ta/Ta₂O₅ memories can modify themselves to a similar state even the fabrication quality had small fluctuations. In the next chapter, operation optimization using the Ta/Ta₂O₅ system will be discussed to achieve higher switching performance to realize the brain-like STDP characteristics.

5.9. References

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Chapter 6 Analog switching behavior optimizations

6.1.Introduction

Functional analog behaviors do not need hard forming and the set process with high-power [1-3]. As discussed in Chapter 5, mild and adequate power injection will cause the functional and stable devices operation. In this chapter, the Ta-device (VCM) showing soft forming is used as an example, and methods to optimize the power injection is discussed to realize the stable analog operation. One of them is insertion of the current limiter layer in the device. Here, a thin SiO₂ was investigated, and the analog behavior was realized on both the set and reset side in the I - V switching cycles. In addition, importance of the set current and the reset voltage was investigated. Systematical adjustment of these two switching parameters achieved better device durability. By referencing the optimized I - V characteristics, analog behaviors using voltage pulses could be managed, and the STDP characteristics could be successfully demonstrated using pre- and post-synapse pulse signals to the device.

6.2.Device fabrications and measurement

The device fabrication procedures were basically the same as the method showed in chapter 5. After the RIE and before the deposition of the Ta₂O₅ film, a SiO₂ thin film (~1.2nm) was deposited on the TiN bottom electrode. Here, the deposition of the SiO₂ film was performed using well controlled deposition rate (0.1 nm/s) evaluated via α -step measurements of separately prepared thick SiO₂ films (deposition time: 30 minutes). For uniformity of the film, the substrates were rotated (typically 5 rpm) during deposition.

As described earlier, the Ta/Ta₂O₅ structure was chosen because of the potential realizability of the artificial synapse. The condition of the Ta₂O₅ deposition was $t_{ox} = 10$ nm and $f_{depo} = 50\%$ because it showed relatively stable switching characteristics and high HRS in chapter 5.

6.3.Basic characteristics

In this section, some basic characteristics are compared between the devices with or without the thin SiO₂ layer (marked as w/ or w/o SiO₂ in the following discussion) to study the effect of the current limiter layer.

6.3.1. The initial states

In figure 6-1(a), the initial resistance R_{ini} of the 8 μm devices of w/ and w/o SiO_2 were compared. Although both showed unevenness on the value, the median resistance of w/ SiO_2 device is about 4 times higher than that of w/o SiO_2 device. This suggested the insertion of SiO_2 film successfully functioned as a serial resistor in the circuit. The switching current should be limited by the film. The forming I - V curves are compared in figure 6-1(b). While these two kinds of device (w/ and w/o) did not show distinguishable differences, the V_{form} of w/ SiO_2 devices were slightly higher than that of the w/o device. After the forming operation, the R_{LRS} results were summarized in figure 6-1(c). Similar to the R_{ini} results in figure 6-1(a), the probability to achieve larger R_{LRS} was higher in w/ SiO_2 devices though the unevenness was increased. The high-power forming must be further avoided by current limitation due to thin SiO_2 . As demonstrated here, insertion of thin SiO_2 layer is effective to achieve soft-forming showing subsequent analog operation.

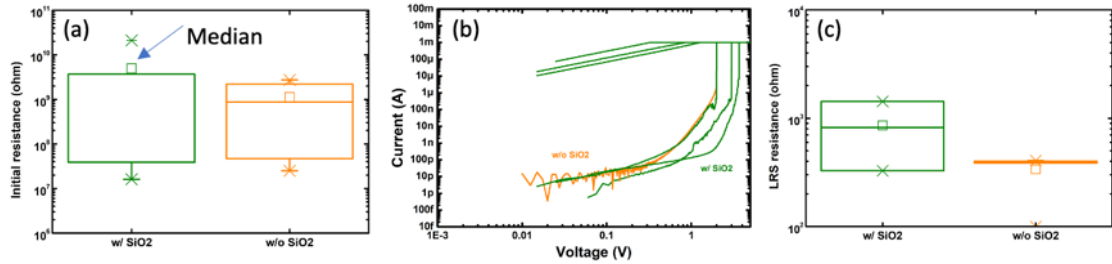


Figure 6-1. The electrical properties compared between the w/ and w/o SiO_2 devices (f 8 nm) of which the data are drawn with green and orange colors, respectively. (a) R_{ini} became slightly higher by insertion of the SiO_2 layer. (b) The forming curves of three w/ SiO_2 devices and one w/o SiO_2 device, where the former devices showed slightly higher forming voltage V_{form} . (c) R_{LRS} after initialization. The w/ SiO_2 devices gave larger R_{LRS} instead of higher V_{form} .

6.3.2. The analog switching behaviors

After the forming operation, cyclic I - V set-reset operations were performed to investigate the switching behaviors. As already shown in chapter 5, the w/o SiO_2 devices showed abrupt set and gradual reset. On the other hand, the w/ SiO_2 devices tended to show the gradual current change starting after a small abrupt set (an arrow in figure 6-2(a)). Though many of the 1st reset showed

abrupt jumps, subsequent operations tended to be gradual as in the w/o SiO_2 device. By insertion of the SiO_2 layer, gradual resistance switching could be achieved in both set and reset operations. Because of this phenomenon, the analog set and the analog reset was possible as shown in figure 6-2(b). In this graph, 6 different resistance states are demonstrated in the set operation. In figure 6-3, the resistance states were plotted as a function of the stop voltage in each cycle, where error bars denote the standard deviation of about 10 individual devices. As expected from figure 6-2(b), gradual resistance states are clearly seen in both set and reset processes of the w/ SiO_2 devices. The appearance of the gradual set states must be caused by the soft-set occurred in the w/ SiO_2 devices, which could not be achieved in the w/o SiO_2 devices. Further optimization of the switching voltage and current should be performed to more precise control of the multi-level resistance state (or analog operation).

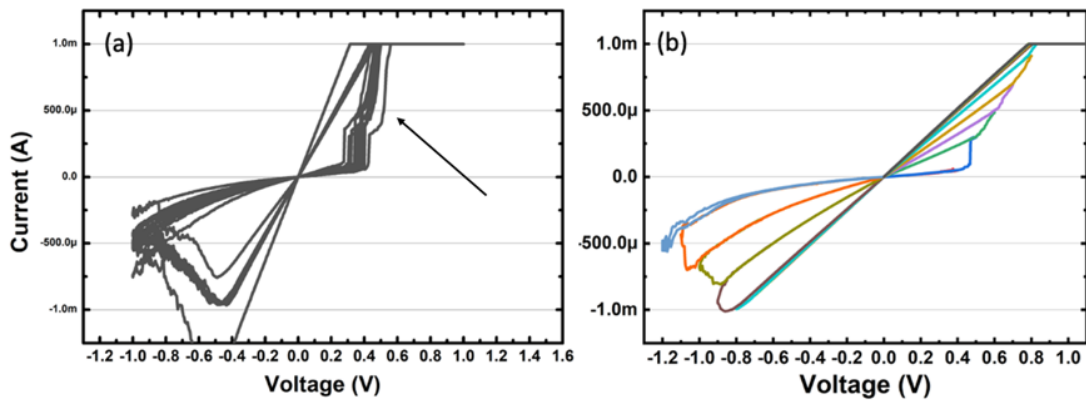


Figure 6-2. (a) 20 times consecutive I - V sweep cycles and (b) the analog behaviors on the set of the devices with SiO_2 inserted.

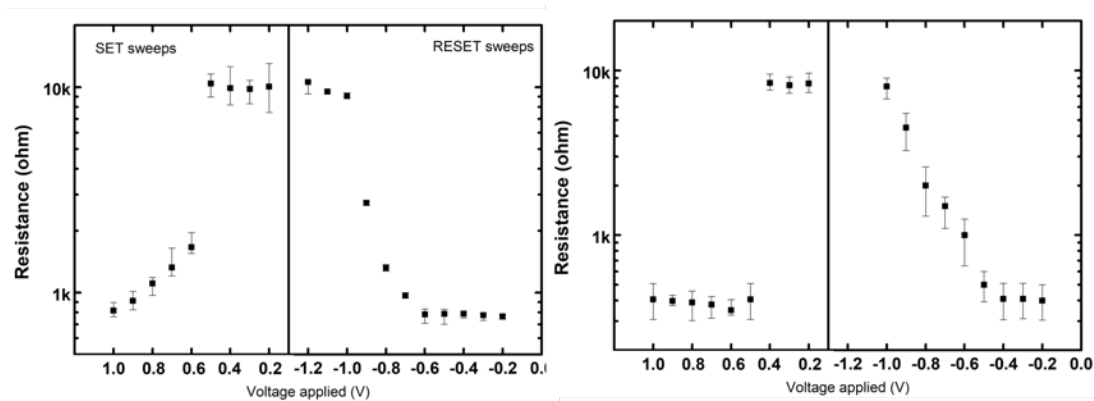


Figure 6-3. The analog resistance states comparing the devices with SiO_2 and without SiO_2 .

The features of the two devices are compared in table 6-1. Inserted SiO₂ weakened the filament formation giving more configurable filament with gradual current change. Without this current limiter SiO₂, the configurable resistance states are become fewer because the characteristics always contain rapid current jumps during set sweeps.

Here, the initial states and the following reset characteristics are briefly discussed using model illustrations in figure 6-4. Firstly, the filament alterations of HRS and LRS are compared in figures 6-4 (a, b) and (c, d). Because the HRS resistances were much lower than R_{ini} , it can be certainly supposed that the succeeding resistive switching behaviors occurred on the platform of the initial filament strongly formed through the insulator during the forming process. The difference between w/ and w/o SiO₂ devices must be caused by the strength of the filament as shown in figures 6-4 (a) and (c). The initially grown filament is thought to be thinner in the w/ SiO₂ device than that in the w/o SiO₂ device because of current limitation by the SiO₂ layer. In figure 6-4 (b)-(d), the filament states of HRS are illustrated to show the possible destruction conditions after reset processes. The detailed filament states during the analog switching will be discussed later in this chapter.

Table 6-1 The comparisons of the filament formation for two kinds of device.

	Initial filament formation	Changeable states
w/o SiO₂	Very strong	Fewer states
w/ SiO₂	Strong	More states

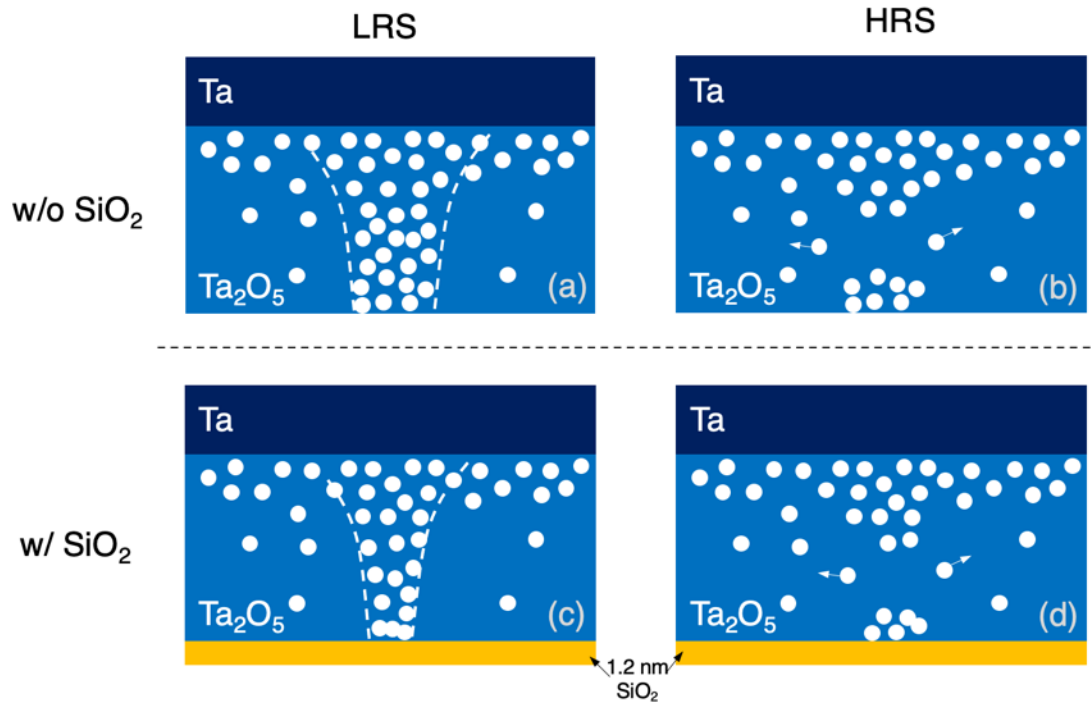


Figure 6-4. Illustrated models for the two kinds of device considering the forming power. The movements of oxygen atoms were omitted, which were considered as the same shown in figure 4-3.

6.3.3. *I-t* sampling experiment

As the third basic characteristic, *I-t* sampling experiments (time-dependent resistance evolution under constant voltage application) were performed to obtain some information about the condition for the pulse operations. Both the forming (initialization) and the set processes were investigated.

Figure 6-5(a) is an example of the forming process. It required the voltage higher than +2.6 V to cause the resistance change. Gradual conductance change was identified by applying constant voltage of +2.6 V, where resistance change was from 1 GΩ to 2 MΩ. The resistance was saturated, and no rapid current jump indicating filament formation through the insulator layer could not appeared within a reasonable duration. By increasing the voltage to +2.7 V, the resistance became 1 MΩ. After increasing the voltage to +2.8 V, the device showed rapid increase in resistance when 1050 s has passed. On the other hand, devices initialized with *I-V* sweeps can be easily switched by the *I-t* sampling as shown in figure 6-5(b). By applying constant +0.8V

bias to the device, the device switched at 9 seconds, that was much quicker than that of forming. The gradual current change was also revealed in the measurement.

The results shown here, +2.8 V (V_{Form}) and +0.8 V (V_{set}), were typically agree with the I - V sweep parameters. While resistance decrease due to filament growth occurred with lower voltages than these values, it occasionally showed saturation. There must be a threshold voltage to realize effective filament growth penetrating the insulator within a reasonable period. These voltages here may fit to the devices fabricated in this work, and further pulse operations were performed using voltage around these values.

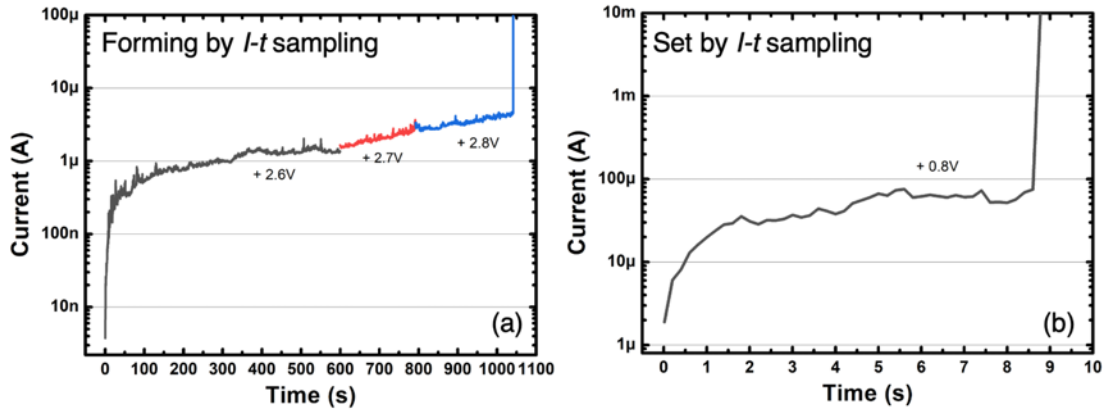


Figure 6-5. The two examples of forming and set operations that used I-t sampling using the w/ SiO₂ device. (a)The forming behavior by the I - t sampling. After the forming, the device was in the broken state. (b)A set operation by the I - t sampling after a sweep-based set-reset operations.

6.3.4. Pulse applications

As discussed earlier, the one-time analog switching capabilities were proved by the constant voltage applications. To control the resistance precisely and to gain essential durability, pulses were needed to separate the I - t characteristics into different resistance states. And by the internal current limiter in the measurement apparatus, the degradation can be also avoided.

In the former sections, it was suggested that the controllability of analog operation can be better by insertion of thin SiO₂ layer. In this section, the pulse operation is demonstrated using the w/ SiO₂ devices. The methods of pulse application can be found in figure 3-12. The used operation parameters are as follows: start-up time of 1 ms, voltage sustain time of 1 ms, shut-down time of 1 ms, and idling time of 1 ms. For every set or reset process, 200 pulses were used.

The read pulse was fixed to be low (+0.02V) to keep the memorized resistance. The voltage of functional pulse is marked in each graph of figure 6-6.

The 6 consecutive pulse based analog behaviors were summarized in figure 6-6. The initialization was performed with I - V sweeps. By applying carefully chosen voltage parameters, analog behaviors were achieved. The resistances after each pulse are summarized in figure 6-7.

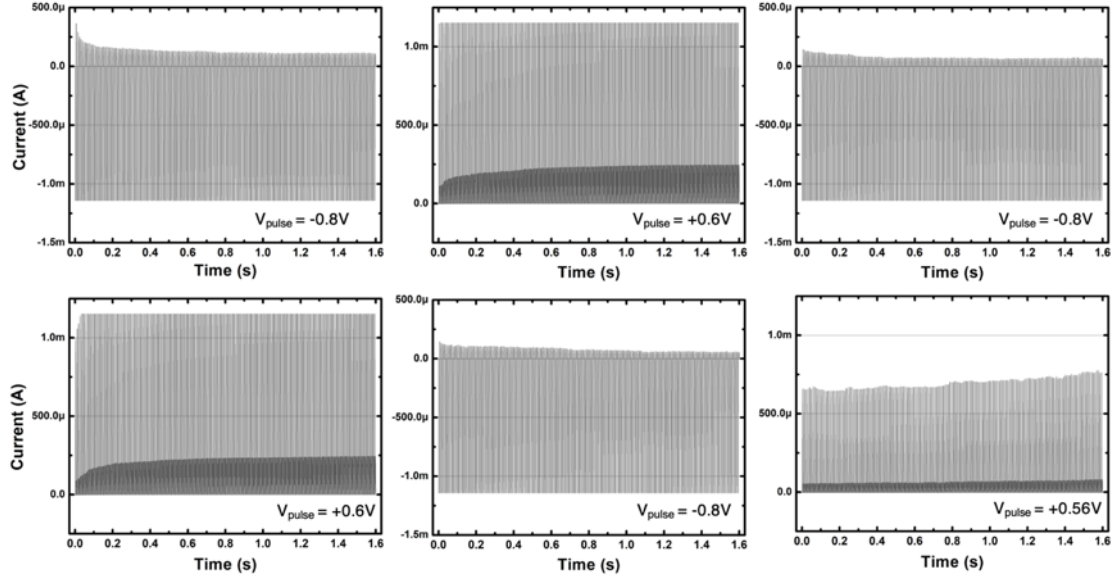


Figure 6-6. The gradual current change by set pulses and reset pulses. The functional pulse current appears to be constant because of the limitation of the apparatus (out of the limitation of current sensitivity). The current continued to change by looking to the read current. The current limit was fixed to 10 mA.

Clearly, gradual resistance changes were realized in our devices. Despite of the unevenness among each application, switching capabilities that more than 1000 pulses were fulfilled. Here, the unevenness appeared in the consecutive measurement is briefly discussed. As obviously appeared in figure 6-7, the first 0.6 V set and the second 0.6 V set produced completely different resistance windows. Here, the operation window and the possible resistance states must change continuously caused by the previous operation process. To gain stable switching behaviors, more precise control on the operation parameters would be necessary as predicted earlier in this thesis.

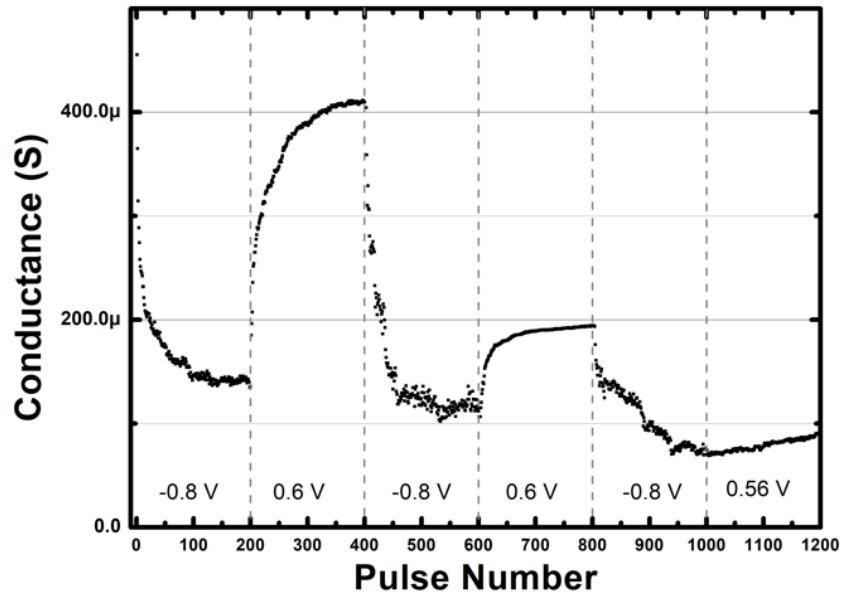


Figure 6-7. The reading resistance change by the pulse number from figure 6-6. The conductance was changing analogously with unevenness between each application.

6.4. Systematic studying the parameters

As shown in section 6.3, insertion of the SiO₂ current limiter layer reduces the forming power and gives good influence to modify the switching behaviors realizing analog operation also in the set process. In this section, to take full advantage of the high controllability gained by SiO₂ insertion, efforts to optimize the operation parameters are explained on the aspect of set current (I_{comp} : the compliance current) and reset voltage ($-V_{\text{max}}$: maximum reset voltage) as shown in figure 6-8.

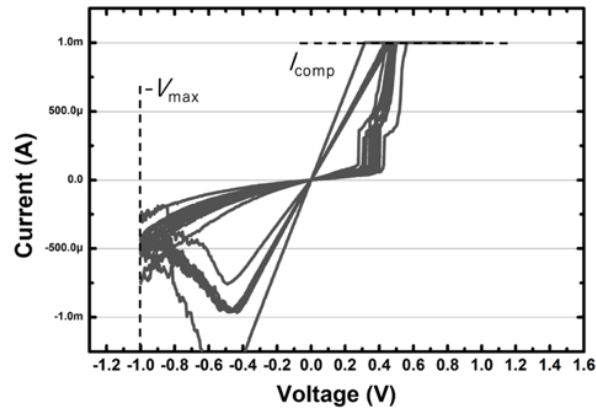


Figure 6-8. The two most effective parameters for the set and reset operations. I_{comp} is the current limitation on the sets and the $-V_{\text{max}}$ is the maximum voltage on the resets.

In the traditional I - V sweep measurements, the configurable parameters were limited to each operation. For the set operations, the controllable parameter is I_{comp} introduced by the measurement apparatus (or serially connected transistor) since it is hard to predict the timing of the current jumps. Although some studies showed the current limit is not effective because of the overshoot phenomenon, this limitation is still effective to control the set power. On the other hand, the applicable parameter for reset is $-V_{\text{max}}$ since the current limits are usually removed. In this work, the sweep rates were fixed (200 mV/s) for all operations. After the initialization processes, these two parameters were studied systematically.

6.4.1. The current limit (I_{comp})

As discussed in previous chapters, the operation current should largely change the filament formation. By limiting the current during the set operations, the filament forms in different degrees. In figure 6-9(a)-(f), continuous set-reset cycles, each of which contains ten I - V cycles, were performed with increase of I_{comp} from 200 μA to 1.2 mA for constant $-V_{\text{max}} = 1.0$ V. Set and reset characteristics changed by increasing I_{comp} . First, only rapid current jumps appeared in the set process for $I_{\text{comp}} = 200$ and 400 μA (figure 6-9(a) and (b)). Gradual set started to appear in the 600 μA and the 800 μA (figure 6-9(c) and (d)). In the cycles of 1.0 and 1.2 mA (figure 6-9(e) and (f)), stable gradual set behaviors can be clearly observed after small current jumps. This gradual developing set characteristics may imply a two-step model generating the metallic contact and the filament growth, which will be discussed later. Secondly, the reset maximum current increased significantly by increasing I_{comp} . This change also suggest that the filament formation of each set became more intensive that was able to carry higher current.

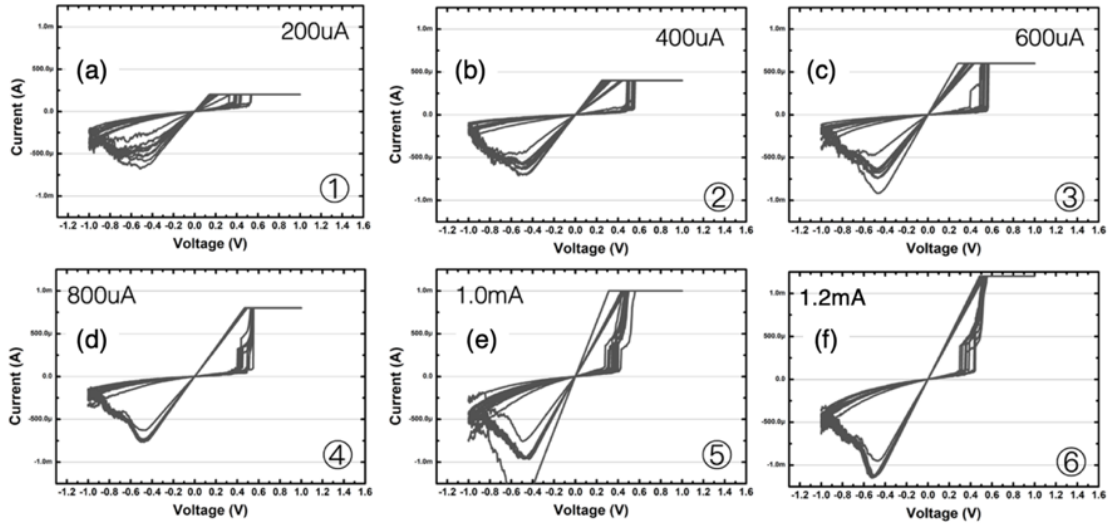


Figure 6-9. Consecutive I - V sweep cycle characteristics with I_{comp} parameter gradually increased.

To exclude the possibility that the characteristic change in figure 6-9 was caused by device degradation, subsequent operations were performed right after the 6th cycles with $I_{\text{comp}} = 1.2$ mA. By reducing the compliance current to be $I_{\text{comp}} = 500$ mA (figure 6-10(a)), the switching curve recovered to that of figure 6-9(b) operated with $I_{\text{comp}} = 400$ mA. While high I_{comp} was used prior to this measurement, the device still showed recoverable characteristics. This behavior directly excluded the degradation possibilities.

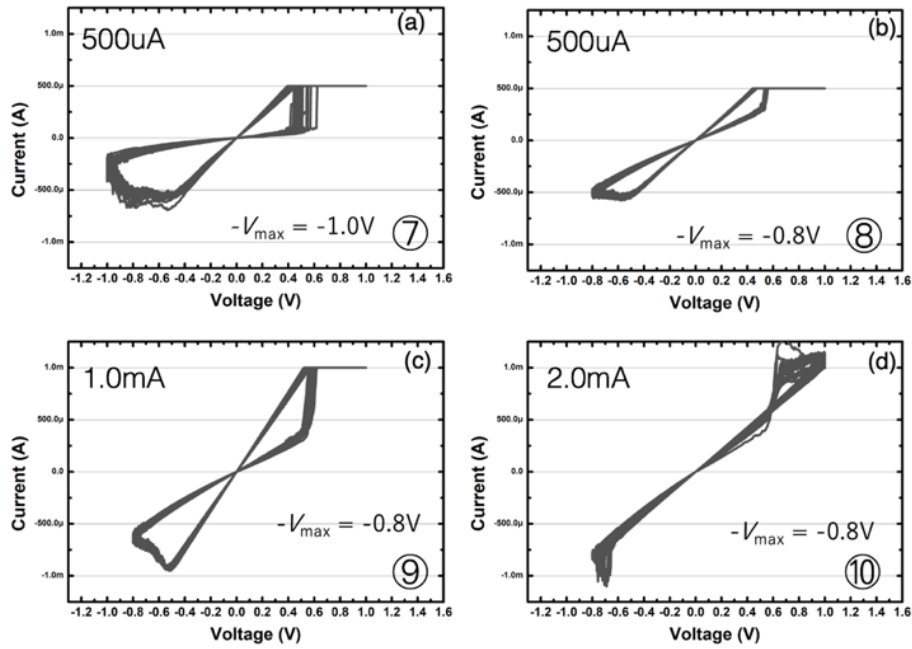


Figure 6-10. Operation cycles after figure 6-10 by reducing $-V_{\text{max}}$ and increasing I_{comp} . The number with a circle denotes the operation sequence following the cycles shown in figure 6-10.

The set process of this graph (i.e., figure 6-10(a)) showed abrupt switching again, though it was gradual in the previous cycles (i.e., figure 6-9(f)). This must be due to complete destruction of the filament showing gradual switching by large $-V_{\max}$ (thus large current flow) used in the reset process. To realize gradual set, $-V_{\max}$ was reduced to be -0.8 V in subsequent cycles as shown in figures 6-10(b)-(c). In figure 6-10(b) with keeping $I_{\text{comp}} = 500 \mu\text{A}$, the set-reset behavior changed much. The resistance decrease around +0.6 V became somehow gradual. In addition, the I - V switching curve became more stable while the R_{HRS} was low. In figure 6-10(c) with $I_{\text{comp}} = 1.0 \text{ mA}$, this tendency can be seen clearly. By increase of I_{comp} , R_{LRS} became low while R_{HRS} was maintained. This gave a reasonable memory window. In such optimized reset condition, we can reproducibly control the filament intensity giving different resistance state.

Another interesting phenomenon is seen in figure 6-10(d) with larger I_{comp} . The curve shape was completely different from the ordinal switching. A clearer curve is presented in Appendix at the end of the thesis (figure A-10). The switching characteristics of HRS \rightarrow LRS and LRS \rightarrow HRS in the set or reset processes was same as the complementary switching as reported in many reports. The filament at the set switching seems to be destructed via further large current flow.

6.4.2. The reset voltage ($-V_{\max}$)

As described in sub-section 6.4.1, the reset voltage plays an important role to control the filament growing in the next set. In this sub-section, systematic discussion about this issue will be presented. In figure 6-11, the evolution of the switching curves is demonstrated, which were measured by increasing $-V_{\max}$ with constant I_{comp} of 2.0 mA. With low voltage $-V_{\max} = 0.55\text{V}$, the switching behavior was barely observed (figure 6-11(a)). By increasing $-V_{\max}$ gradually, weak reset started to occur, and the resistance window started to open (figure 6-11(b)-(d)). Further increase of V_{\max} induced clear gradual set operations (figure 6-11(e)-(h)). Interestingly, the maximum reset current generally equals to $I_{\text{comp}} = 2 \text{ mA}$. Finally, in the case of $V_{\max} = -0.95\text{V}$, strong resets started to appear associating the wide window, however current change fluctuated much. The resistance change in these cycles are plotted in figure 6-12. R_{HRS} gradually increased with V_{\max} higher than 0.65 V while R_{LRS} was almost constant because of the same I_{comp} .

This series of result emphasized the functionalities of reset. By forming the filament similarly by the fixed I_{comp} , the filament destruction degree (accompanying the HRS resistance) can be

controlled by the respective reset voltage. And this influences the quality of the set operation as well. The results could be observed in the device with the thin SiO₂ but not in the device the without SiO₂ (the maximum reset current was extremely high). Successful prevention of intensive filament formation is important to achieve high controllability.

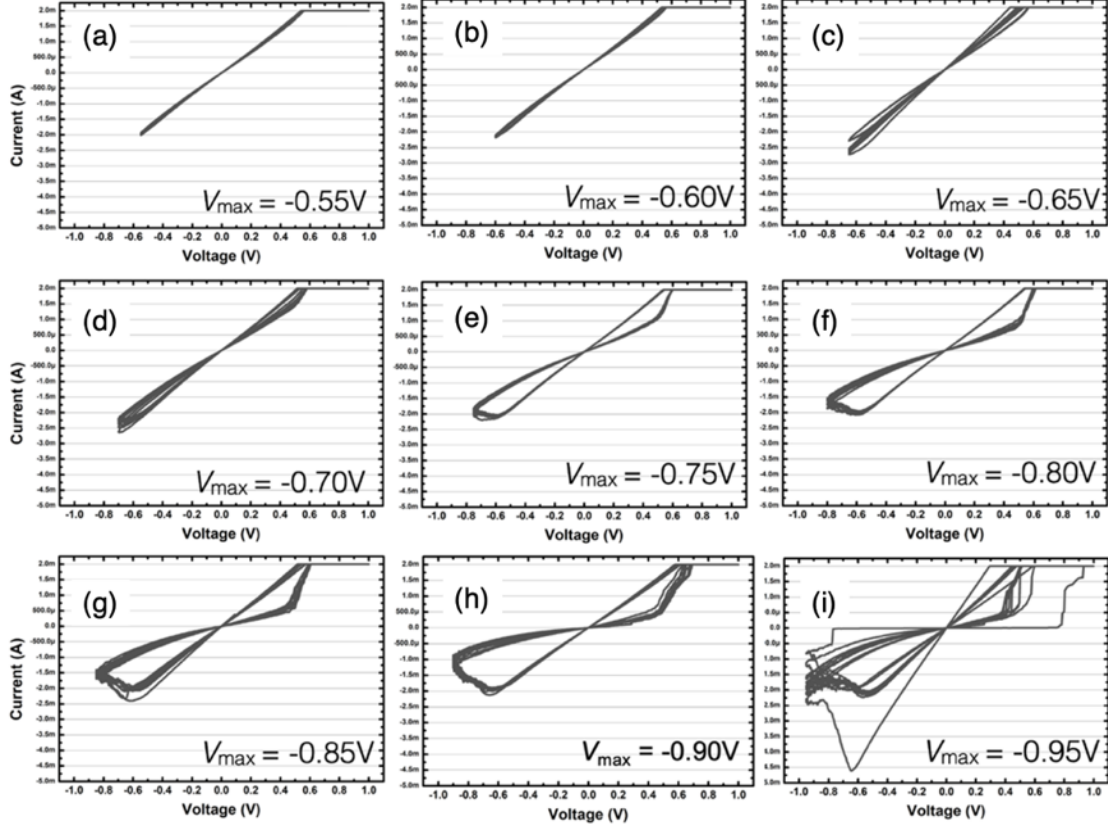


Figure 6-11. I - V sweep cycle characteristics with gradually increasing $-V_{\max}$ ($I_{\text{comp}} = 1$ mA for set).

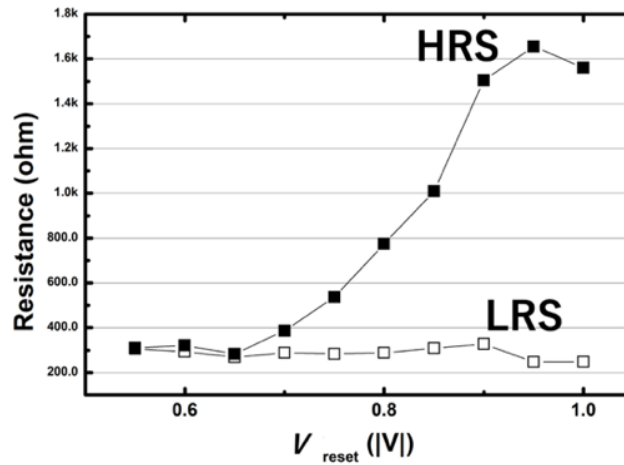


Figure 6-12. The device resistance in HRS and LRS. The median results of figure 6-12(a)-(i) are plotted.

6.5. Set-reset competition in the analog switching

Desired analogous resistive states are contained in the operation window demarcated by the present-states of HRS and LRS. As discussed in the section 6.4, the resistances of HRS and LRS are basically decided by $-V_{\max}$ and I_{comp} , respectively, which compete each other to give the adequate switching window. Limiting the discussion within conditions giving analog operations, the relationship in the stable analog operation range is schematically illustrated in figure 6-13 to express this competition between $-V_{\max}$ and I_{comp} . By increase of $-V_{\max}$ (dark brown), the LRS becomes low and overall resistance during operation is low. On the other hand, by increase of I_{comp} , it becomes high (dark blue). These are unbalanced situations, and its degree of unbalance can be drawn using gradient colors. Idealistically, the set and reset operation should be balanced (white square in the figure). While the window for analog operations is not so large at the upper-left condition, it increases when the power ($-V_{\max}$ and I_{comp}) becomes towards the right-bottom condition. However, when the power is too much, abrupt switching with binary or complementally operation will occur (out of the region shown in figure 6-13). In addition to the power balance between the set and the reset operation, the operation power itself should be carefully optimized to realize stable analog operations.

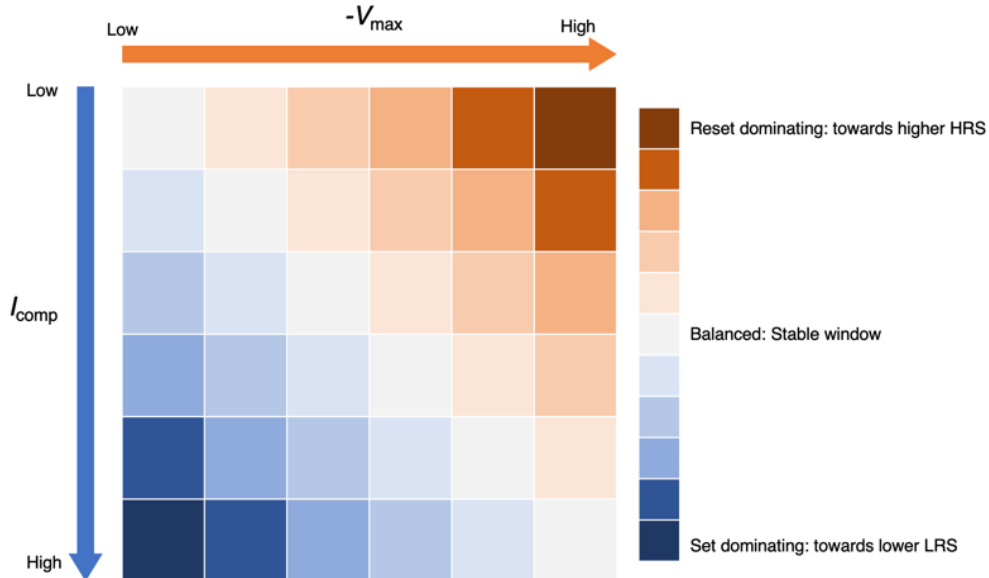


Figure 6-13. The competing relationship of the $-V_{\max}$ and I_{comp} .

6.6. Optimizing analog behaviors and STDP realization

6.6.1. Pulse optimization

Besides the switching behaviors based on the I - V sweep, the pulse parameters to fulfill the analog behaviors were studied. Since the parameters of the pulse operation were much different from those of the I - V sweeps, we can use voltage pulses: the set pulse voltage V_{set} influencing the set current like I_{comp} , and V_{reset} . In figure 6-14, two successful pulse operations are demonstrated. Figure 6-14(a) shows the hundred set-reset cycles (100 pulses each and thus totally 10^4 pulses). The operation voltages were $V_{\text{set}} = 0.7\text{V}$ and $V_{\text{reset}} = -0.9\text{V}$ which were about the set voltage and $-V_{\text{max}}$ in the I - V switching curves in figures 6-9, 6-10 and 6-11. Clear switching repetition was realized although the overall resistance gradually increased. Looking at the enlarged graph (inset of figure 6-14(a)), more or less analog operation is identified. In figure 6-14 (b) operated under the condition with slightly strong reset operation ($V_{\text{set}} = 0.5\text{ V}$ and $V_{\text{reset}} = -1.0\text{ V}$), the pulse cycles are also realized. However, the switching was less analogous having abrupt resistance change. By using higher V_{reset} , the HRS resistance (R_{HRS}) became large, but switching became abrupt as seen in figure 6-11(i). Thus, analog capability in this case was poor. The set and reset voltages giving analog I - V cycles are key factors to realize analog operation by using pulse inputs. Careful optimization is required to realize stable analog operations. In addition, other parameters like start-up or shut-down time may also be important to be optimized which were not studied in this work.

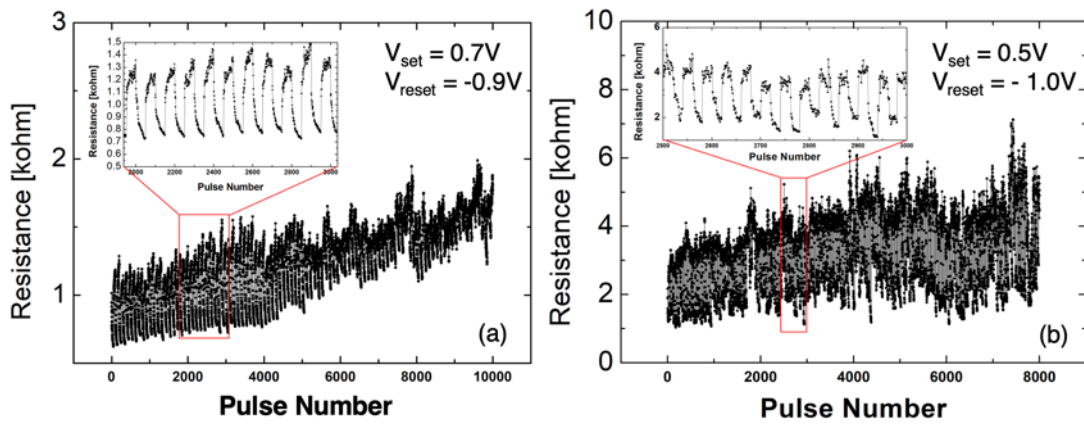


Figure 6-14. Two optimized pulse characteristics by adjusting the voltage using two individual devices; (a) $V_{\text{set}} = 0.7\text{ V}$ and $V_{\text{reset}} = -0.9\text{ V}$, (b) $V_{\text{set}} = 0.5\text{ V}$ and $V_{\text{reset}} = -1.0\text{ V}$.

6.6.2. STDP realization by modulated pulses

On the basis of the result of the pulse operation, the synaptic-like spike-timing-dependent plasticity (STDP) behavior (*e.g.* figure 1-5) is briefly demonstrated in this sub-section. Since the biological signals generated by neurons were extremely complicated, simple pulse signals were used as shown in figure 6-16(a). Here, two pulses (pre-spike and post-spike) were arranged to have slightly low voltages to prevent abrupt switching (figure 6-15(a)). These two pulses were composed with gradually changed time differences Δt . Some examples of the input signals to the device are shown in figures 6-15(b)-(d). A summary of the results is demonstrated in figure 6-16. A typical STDP characteristics were realized. With reduction of the operation power using insertion of thin insulator limiter (*e.g.* SiO₂) and input voltage, such a fundamental property used for AI functionalities could be realized. Power control is a quite important factor.

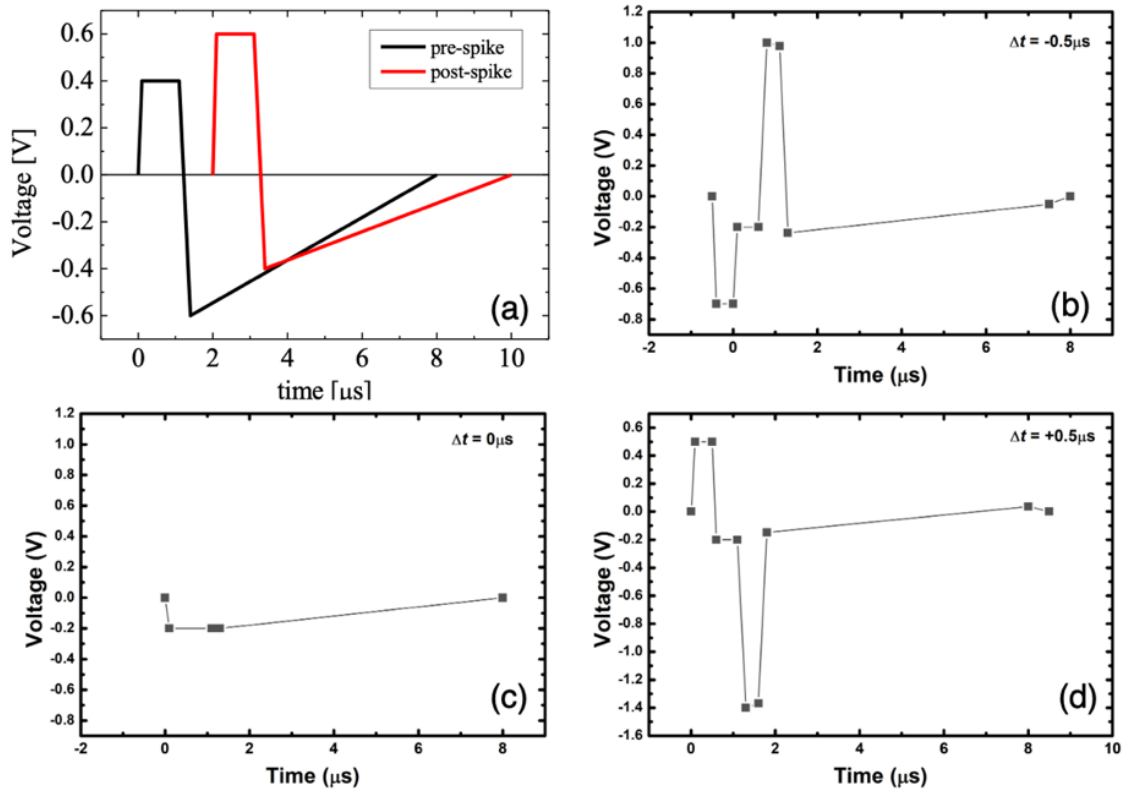


Figure 6-15. The used pulses of SDTP. (a) The pulse shapes of pre-spike and post-spike signals. (b)-(d) There examples of input pulses via composition of pre- and post-spike pulses with different Δt .

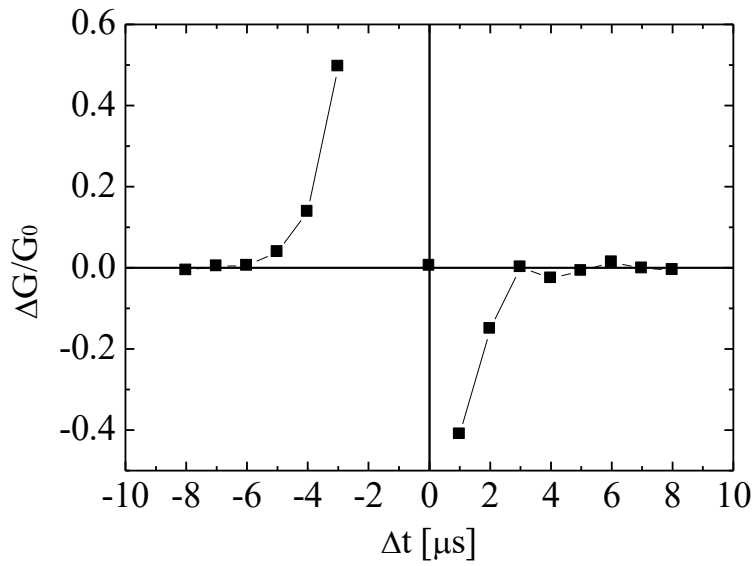


Figure 6-16. STDP realizations using optimized characteristics.

6.7. Discussions of model during switching

In this section, the resistance states giving a certain switching window is briefly discussed based on filament states expected in the Ta/Ta₂O₅/SiO₂ structure. The important electrical properties acquired in each part of operation are as follows:

1. **initial state and initialization**: (a) Different electrode had distinguishable R_{ini} . (b) In general cases, R_{HRS} after forming is much lower than R_{ini} .
2. **analog switching states**: (a) Multiple resistance states can be achieved in set and reset in w/ SiO₂ devices. (b) Unstable resistance window shifts were observed.

In figure 6-17(a), a schematic illustration describing the resistance states is presented. The color-gradient bar in the upper line represents the overall resistive states from the initial (or pristine) state to the malfunctional state after device destruction. For the VCM devices, initialization caused much resistance decrease from R_{ini} . By different applications of external voltage, different HRS and LRS can be realized. The resistance range giving functional operations (called the "switching window" in this report) is a subset of these states as shown in the bottom line. The switching window contains all achievable analog resistive states by systematically controlled set-reset sweeps or the electrical pulses. The HRS and LRS values are not necessarily the same during the switching operations, they are dynamically alternating during

the switching operations. By destructive operations, such as high-power forming or device degradation, the device will be switched to the malfunction state (usually extremely low LRS).

On the other hand, the important issues concerning the underlying mechanism are as follow:

1. **initial state and initialization**: Spontaneous oxygen scavenging behaviors occurred at electrode/insulator interfaces.
2. **analog switching states**: (a) Filament was destructed by reset but not completely since R_{HRS} was much lower than R_{ini} . (b) Filament control gained extra controllability by insertion of the SiO_2 current limiter.

Concerning these matters, the oxygen vacancy distributions of the initial and the malfunction states are schematically drawn in figure 6-17(b) and (g), respectively. States with no filament or having extremely thick conductive region bridging two electrodes are illustrated. The state giving the HRS shown in figure 6-17(c), where the filament destruction must be incomplete because the resistance was much smaller than R_{ini} . On the other hand, the LRS has a filament with a reasonable thickness (figure 6-17(f)). Resistance switch between these two states gives a binary operation with a certain memory window. Analog behaviors can be realized within this window by possibly changing the filament thickness as shown in figures 6-17(d) and (e). There were several hints suggesting how the filament behaved during the analog switching. There was a small current jump during set even for the w/ SiO_2 device (see figure 6-8, for example). This may suggest formation of filament pieces at the beginning of each set process (figure 6-17(d)). Afterwards, the thin filament grows in the horizontal direction to increase the diameter (figure 6-17(e)) with the help of Joule heat generated by the current flow [4-6].

This two-step formation process is a possible scenario to explain the gradual resistance change revealed in this study. Two-stage set operation observed in the device with SiO_2 current limiter supports this model. In figure 6-2(a), the set behaviors contained a rapid current jump at low voltage (formation of the filamentary fragments) and then the conductance can gradually increase (filament grows because of Joule heat). Another possible scenario is the multi-filament operation. The individual filament destruction in reset increases the device resistance only by a small amount and gives the analog behavior. The gradual set can also be achieved in this scenario. Whichever the major origin is, the power limitation by the SiO_2 current limiter layer is the

important factor for device design. In this work, no analog set was achieved for the w/o SiO₂ devices. In this case, the maximum current in the subsequent reset was much higher than that of the w/ SiO₂ devices. This difference suggested the filament intensity was much different: too strong (or thick) filament in w/o SiO₂ devices and mild filament in w/ SiO₂ devices. Only in the latter case, control to form thin filament shown in figure 6-17 or multi-filament state can easily be done. Without the current limiter, more accurate and complicated optimization process seems to be required.

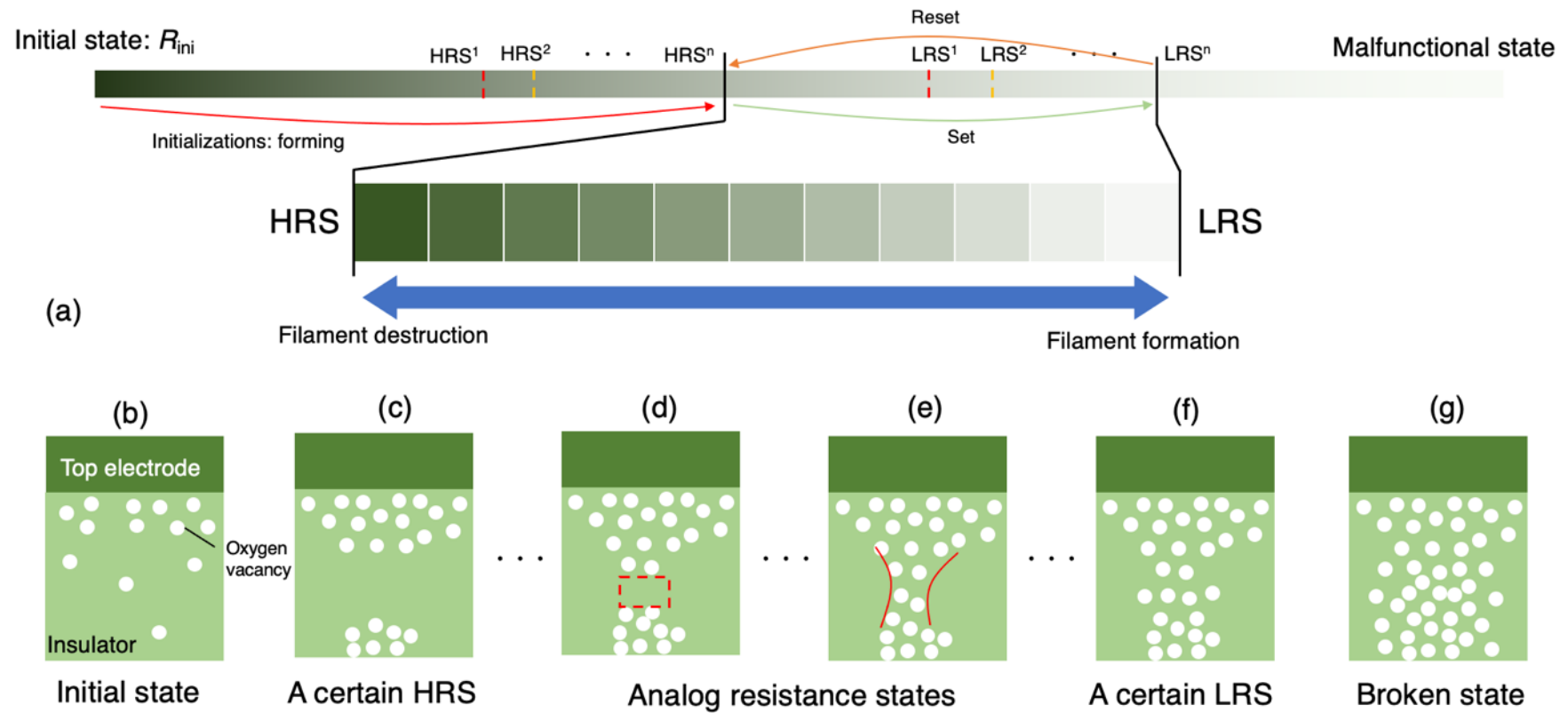


Figure 6-17. (a) The relationship between the overall resistance states (upside) and manipulative resistive states (downside). The HRS^n or LRS^n stand for the different resistive states that can be achieved by different operations of set or reset. (b)-(g) Possible filament states from the initial state to the malfunctional state. Specifically, (d)-(e) shows the filament conditions during the analog switching and the resistance changes can be thought caused by the metallic contact or the thickness of the filament. Models of ‘A certain HRS’ and ‘A certain LRS’ in (c) and (f) were illustrated in possible filament conditions of HRS^n and LRS^n . The filament conditions were not absolute and can be considered dynamic (between all possible resistive states) due to the set and reset operations.

6.8. Conclusions

In this part, the Ta/Ta₂O₅ resistive memory was chosen and the improvement of the behaviors by inserting the SiO₂ current limiter was performed. In the initializations, the device had already showed the distinguishable differences that suggested the forming behaviors occurs weaker. Because of the internal current limitation, the filament formed gained extra controllability in realizing the analog behavior on the set operations. To take full advantages of the characteristic improvement brought by the current limiter, we studied two main parameters during the switching. We also tried to optimize the pulse applications and the synaptic STDP was realized. From the results, the underlying filament formation and destruction mechanisms during switching were proposed.

6.9. References

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Chapter 7 Summary and conclusions

The requirement to build high performance ANN on chip requests new type of memory devices like the resistive memory. With scoping this perspective, variety of materials have been tested to realize the memory that having good controllability. However, the systematic study on the relation between material selection (switching oxides and electrode metals) and the device characteristics (pristine state and subsequent memory operation) is still lacking. In this study, a series of study focused on $\text{Ta}_2\text{O}_{5-\delta}$ based resistive memories having different oxygen deficiencies and different metal electrodes were performed, with investigating the underlying mechanism of the switching behaviors. The initial state and the initialization property of the device were clearly influenced by intrinsic and extrinsic oxygen vacancies. However, other factors such as vacancy distribution like formation of interfacial oxide were also clarified to strongly influence the properties. Afterwards, detailed correlations between initial states and analog operations of both VCM and ECM were established, and their individual analog switching capability were clarified. Finally, using Ta-devices as an example, design and operation optimization was investigated to control the injected power, especially current for Set and voltage for Reset, and pulse operations were demonstrated. The results summarized below should give a fundamental guideline to realize stable analog operation though details should be optimized depending on materials used for the resistive memory.

Initial state analyses of metal-mask samples

The electrical characteristics and the interface observations of $\text{Ta}_2\text{O}_{5-\delta}$ resistive memory was performed on 8 kinds of device that have different top-electrode materials and different δ . The initial resistances were affected by the intrinsic and extrinsic oxygen vacancy concentration. The intrinsic oxygen vacancies determined by δ can affects to the difference in extrinsic scavenging effects caused by top electrodes. In other words, the initial states were not mainly affected by a single parameter like the Gibbs free energy, because the conditions induced by the combination of the intrinsic and extrinsic oxygen vacancies are the more important aspect in a practical level. TEM-EDS analyses showed that the scavenging effects occurred differently at the electrode-insulator interfaces that should be considered as important factors influencing the forming properties.

Switching capabilities of scaled devices

Same scavenging electrode materials were used to achieve the analog switching capability and to investigate the relationship between the initial states and switching states. To give a comparison to typical VCM model, Cu as an ECM model was also introduced. The initial states were much different in VCM and ECM devices, and they influenced the respective analog behaviors. Ta-electrode based VCM devices showed that the analog behavior was relatively stable and identical to each other while the initialization characteristics showed dependencies to the initial resistances. On the other hand, Cu-electrode based ECM devices showed various forms of characteristics. Specifically, 20-nm ECM device showed high HRSs that were the possibilities that realizing the low-consumption switching. Ti and Al electrodes were also investigated for their analog capabilities and distinguishable characteristics were revealed for each.

Analog behavior optimizations of bilayer device

Based on the results, Ta/Ta₂O₅ composition to the more detailed characterizations was chose. In addition, optimizations of the behavior by inserting the SiO₂ current limiter to the Ta/Ta₂O₅ device were performed. The device had showed the different initial states that suggested the forming behaviors were alternated by the new layer. Because of the internal current limitation, the filament formed gained extra controllability in realizing the analog behavior on the set operations. To take full advantages of the characteristic improvement brought by the current limiter, two main parameters during the switching were studied. Based on the parameter study, optimizations of the pulse applications that enable the device to demonstrate the synaptic STDP. The filament behavior during the resistive switching was also discussed to complete our switching models from the initial states. The filament destruction and formation were closely relative to the stable analog switching behaviors, and the power input during set and reset processes are extremely important to the characteristics.

Appendix

I. The initial resistance of TiN, Ti, Mo devices

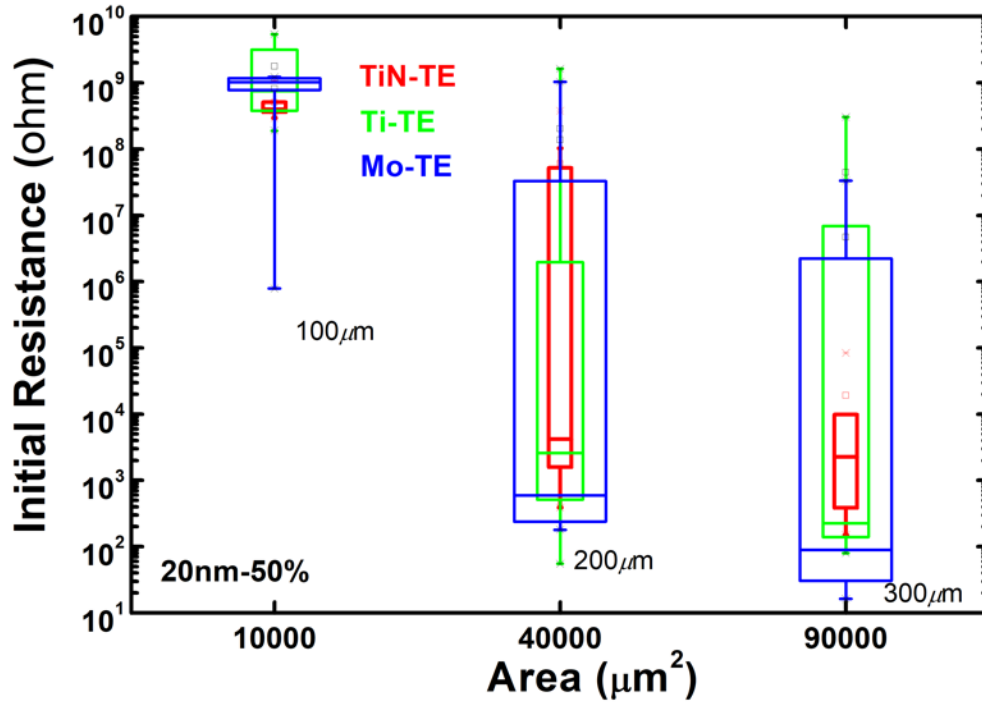


Figure A-1. The initial resistance results of 20 devices for each condition of TiN, Ti and Mo electrodes by the device size used in [chapter 4](#). Although the result did not show clear dependence on the material that used, the discussions that only used 100 μm devices successfully revealed the scavenging effect differences among different electrodes. The Mo electrode was selected to be a tester of the MM-structure.

II. The forming behaviors of TiN, Ti, Ta, Al devices

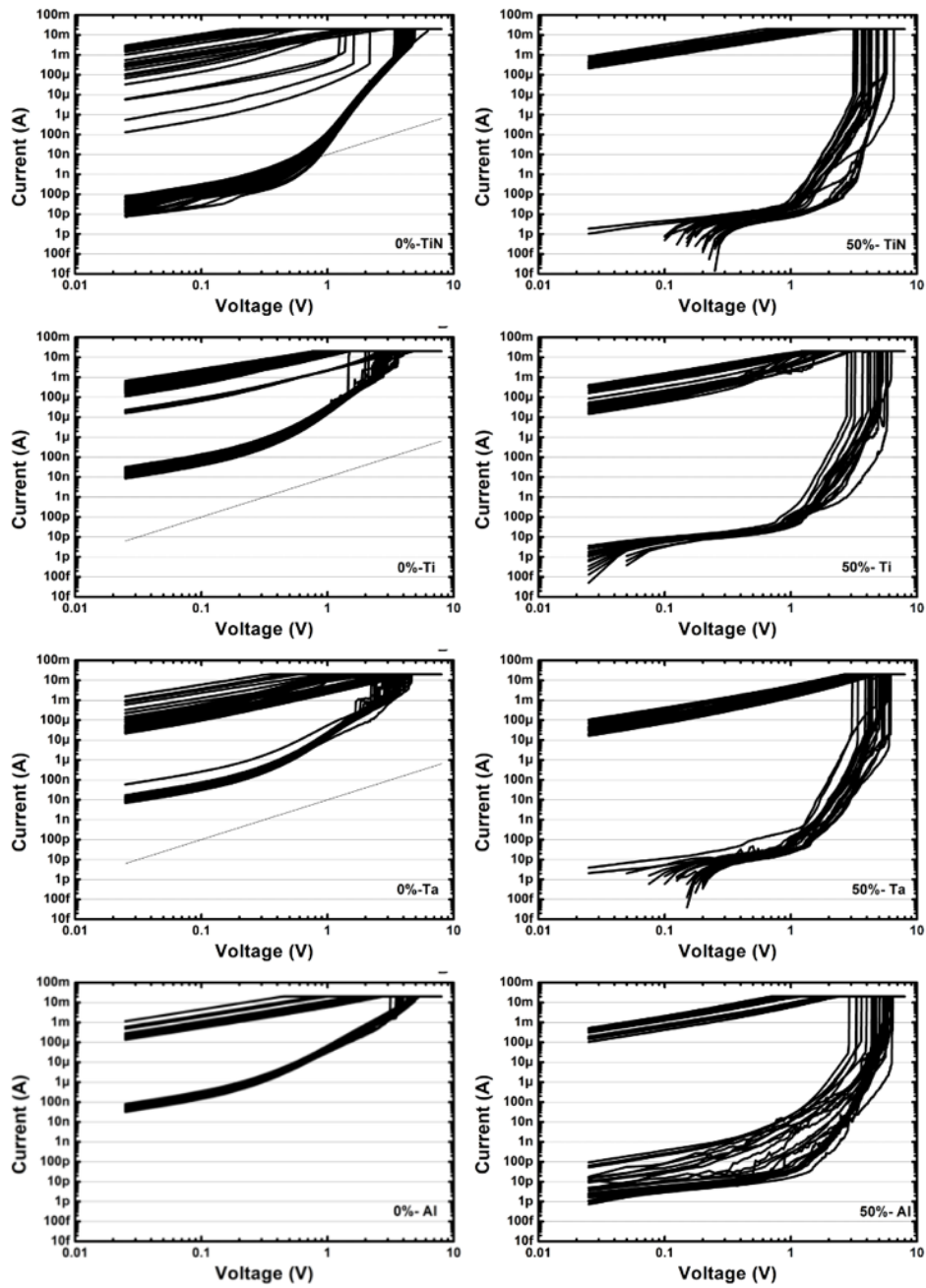


Figure A-2. Complete forming behaviors of at least 20 devices for each condition used in [chapter 4](#).

III. The initial states of MM-devices

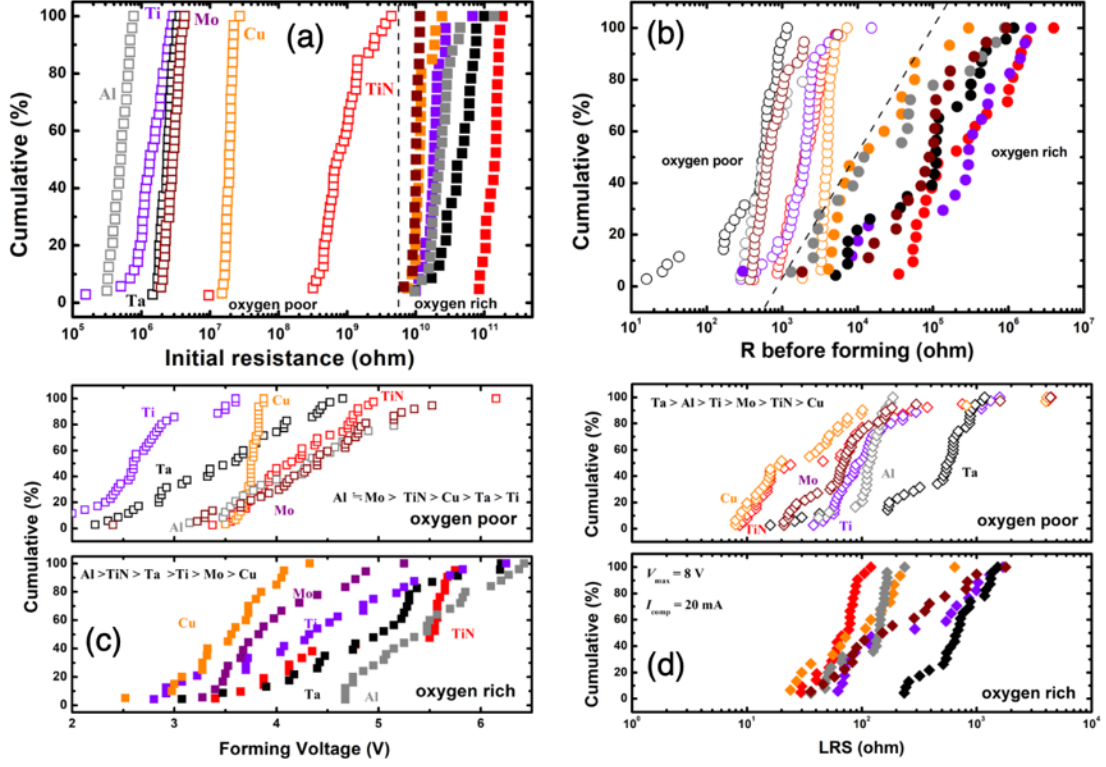


Figure A-3. Extra information about the initial states of the devices in [chapter 4](#). Cu and Mo were also used however the results were not conclusive. (a) the cumulative R_{ini} figure of measured devices. (b) the cumulative R_{set} of measured devices. The results were thought that indicating the filament statuses before the metallic contact of filament. (c) the cumulative V_{form} of measured devices. (d) the cumulative R_{LRS} of measured devices.

IV. Area dependent initial resistance

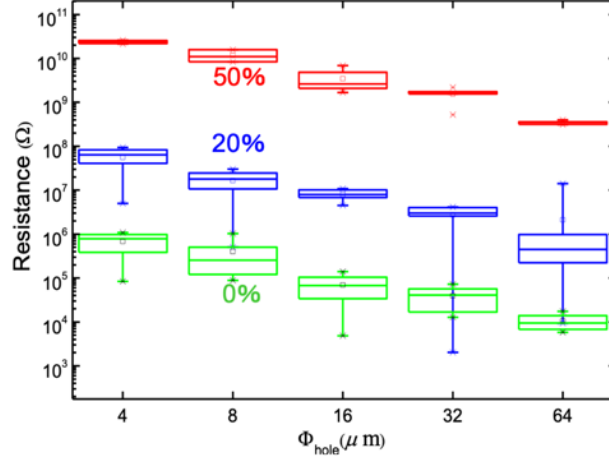


Figure A-4. Three example sets of the initial resistance distributions of 0%-10nm, 20%-10nm and 50%-10nm devices of Ta electrode used in [chapter 5](#), where in the chapter, only 8 μm devices were discussed. Clearly the distributions showed clear area dependency.

V. Analog switching and switching failures

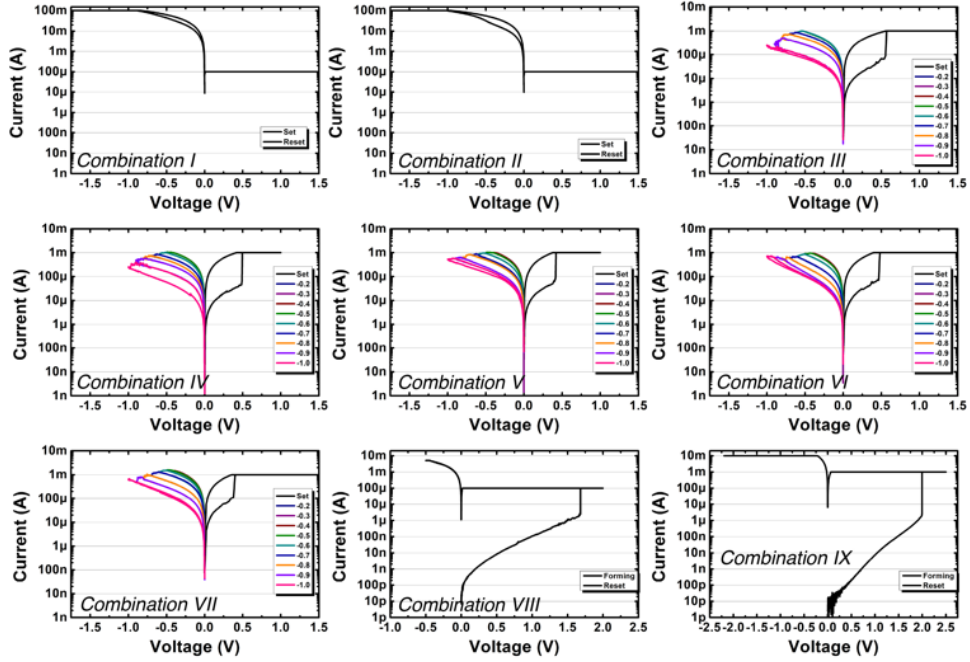


Figure A-5. Analog switching behaviors and two kinds of initialization failures of Ta devices in [chapter 5](#).

VI. XPS analyses

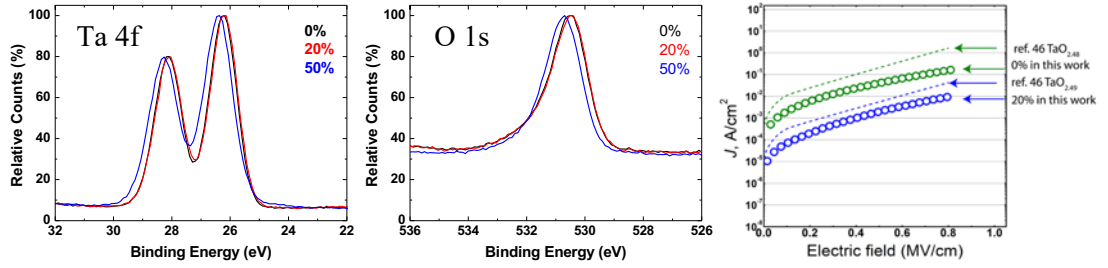


Figure A-6. (a, b) Results for Ta-4f and O-1s XPS results, respectively. (c) Converted I - V characteristics for TiN/Ta₂O_{5- δ} /TiN devices. Dotted lines are showing the I - V characteristics of TaO_{2.48} and TaO_{2.49} provided by ref. 11 in [chapter 5](#).

VII. Consecutive Set-Reset operations of VCM and ECM

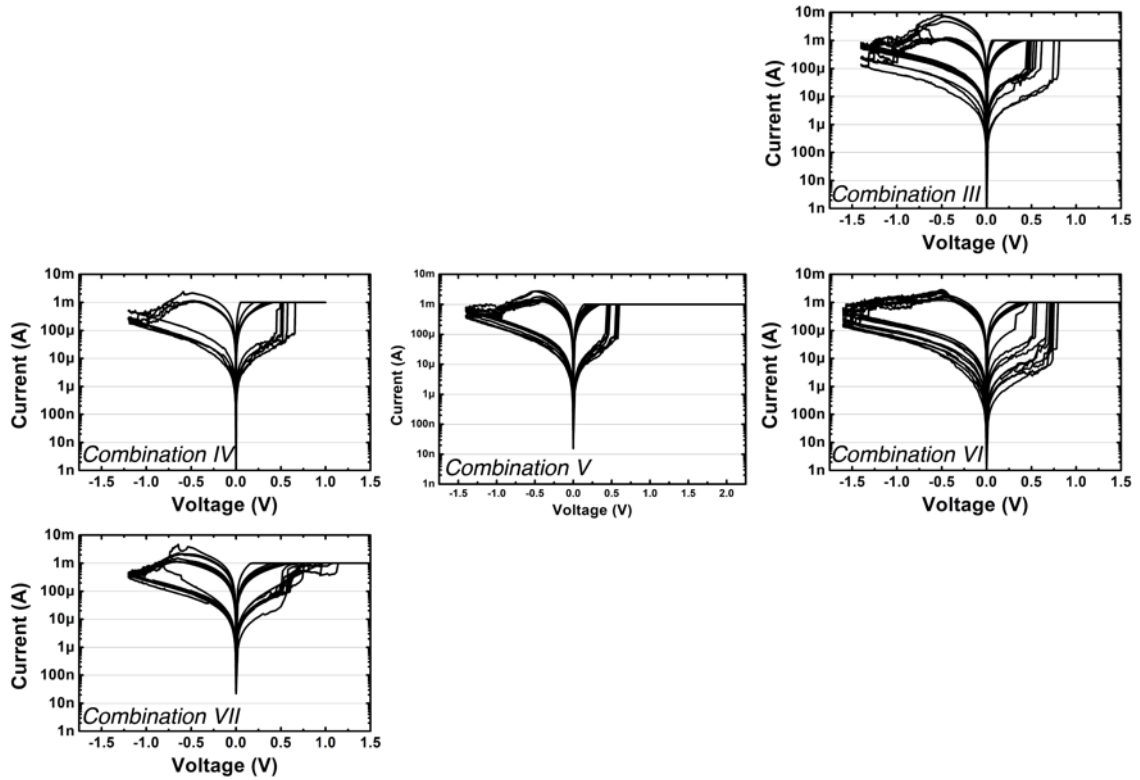


Figure A-7. 10 consecutive Set-Reset switching cycles using one Reset method on successfully initialized Ta devices in [chapter 5](#). Variations of the switching voltage (approximately 0.5 V) can be observed.

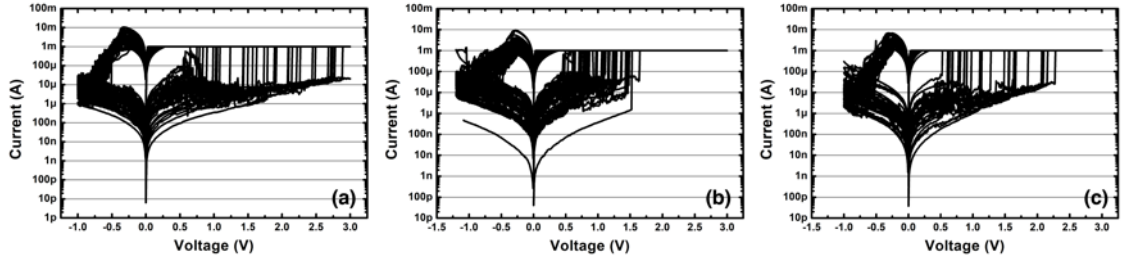


Figure A-8. Consecutive Set-Reset switching cycles using one Reset method on 20-nm Cu devices in [chapter 5](#). Variations of the switching voltage (>1.1 V) can be observed. Large variations of the Set voltage were observed.

VIII. Behavior variation and complementary switching

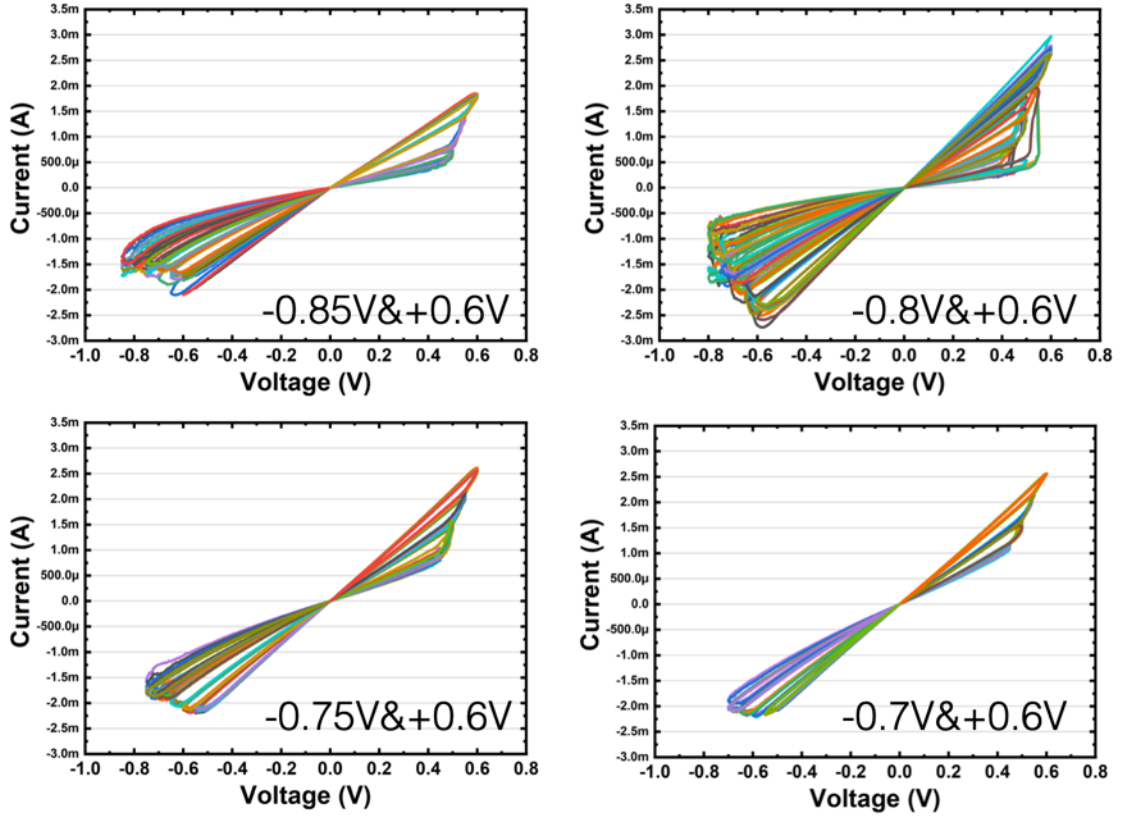


Figure A-9. Characteristic control by not applying I_{comp} , only changing the $-V_{\text{max}}$.

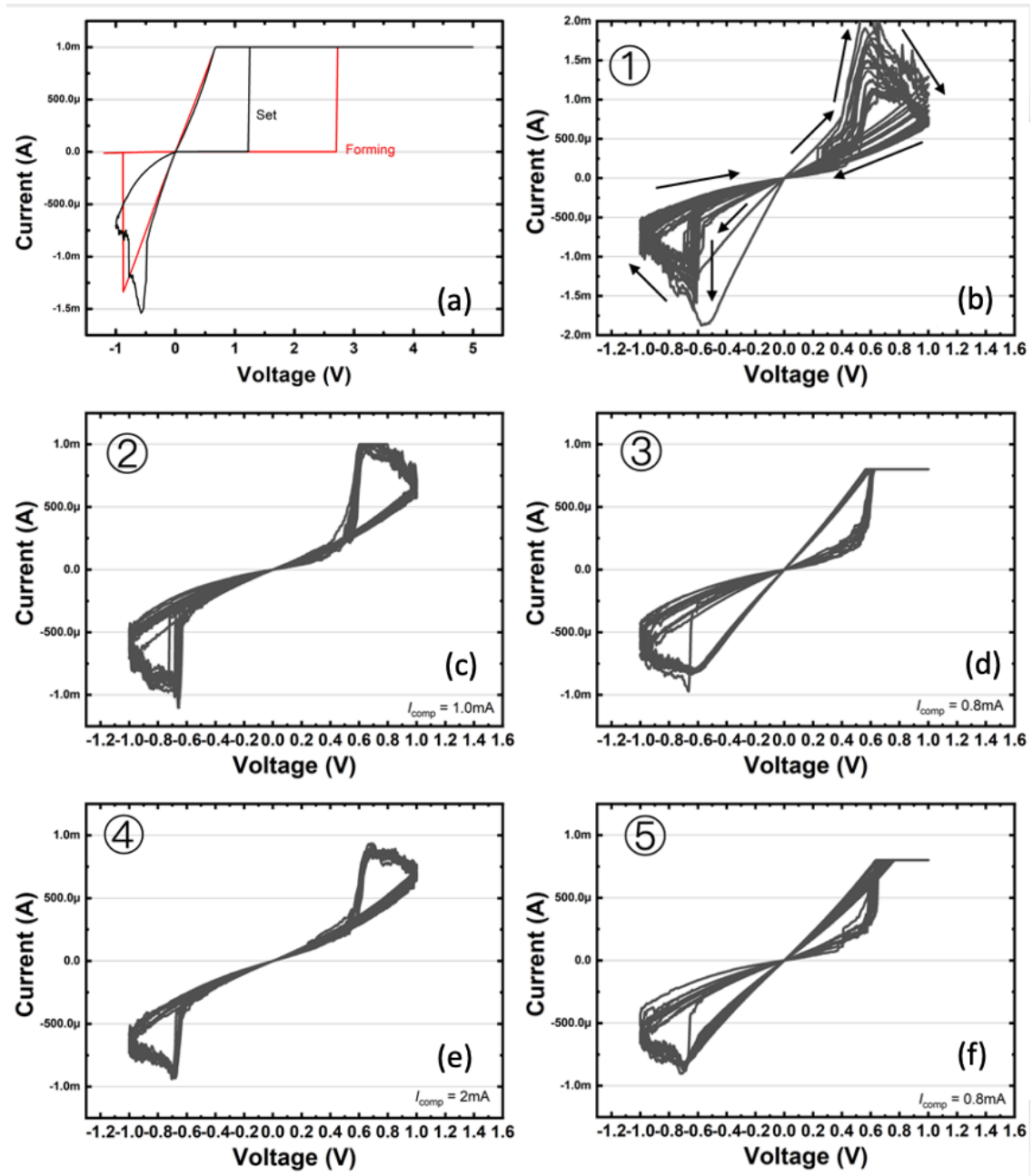


Figure A-10. This set of figure shows consecutive I - V sweep cycles after the first initialization using the device in [chapter 6](#). By releasing the current limit, complementary switching pattern revealed in (b). Next, the I_{comp} was decrease to 1mA to see the difference and the behavior became stable. In figure (d), interestingly, the behaviors were backed to the familiar states shown earlier. The different line in the reset is the remaining effect from (c). Then, to confirm the characteristics could back again to the complementary states, we increased the I_{comp} again. As we predicted, the complementary characteristics revealed again, and then similar phenomenon occurred again in figure (f). This kind of behavior often appeared in our measurement. However, detailed methods of entering this complementary mode were still unclear. We still

think this was a profound discovery since it showed more possibilities that could be gained by the application of current limiter.

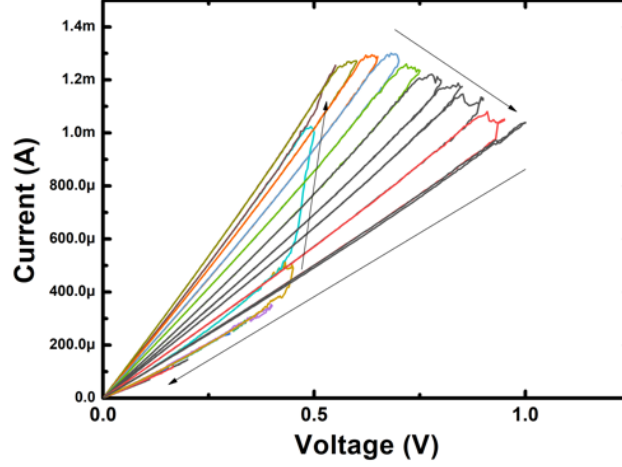


Figure A-11. Taking advantage of the characteristics we acquired in figure A-9, we successfully revealed the analog-like behaviors like we did in the earlier chapters. Clearly, more resistive states were fulfilled. This could be a profound characteristic in realizing alternative characteristics of artificial synapse in the future.

IX. The initial resistance comparisons

The initial states for the two kinds of devices were compared. The median values of R_{ini} are plotted in figure A-12 (a) and (b) and (a) is for the MM-devices and (b) is for the photolithography devices with 8- μ m via holes and 10nm insulator. 8- μ m devices did not show theoretical higher R_{ini} than the MM-devices by 24.88 times. The lower R_{ini} of 8- μ m devices should be considered due to the scavenging effect in such a short distance of 10 nm. The pristine Ta_2O_5 can be preserved in 20nm MM-devices to show extremely high R_{ini} even the area was large.

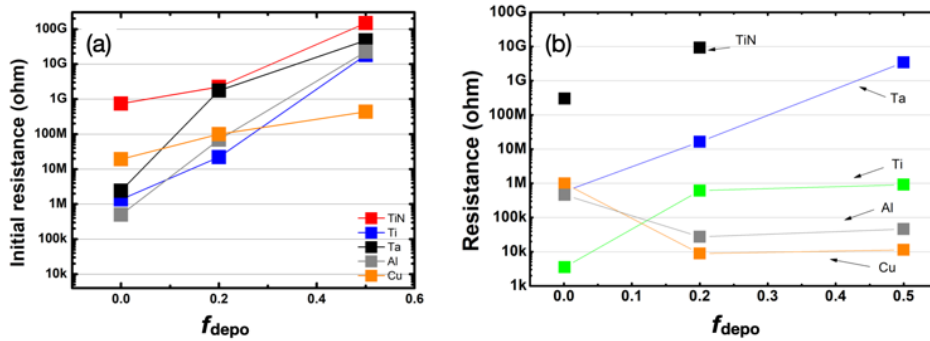


Figure A-12. The initial resistance comparisons.

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Without the assistance and support from people around me, this thesis would not be possible. I want to give my sincerest appreciation to them.

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