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III-V Quantum Devices and Circuits Based on Nano-scale Schottky Gate Control of Hexagonal Quantum Wire Networks

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Abstract

The concept, the present status, key issues and future prospects of a novel hexagonal binary decision diagram (BDD) quantum circuit approach for III-V quantum large scale integrated circuits (QLSIs) are presented and discussed. In this approach, the BDD logic circuits are implemented on III-V semiconductor-based hexagonal nanowire networks controlled by nano-scale Schottky gates. The hexagonal BDD QLSIs can operate at delay-power products near the quantum limit in the quantum regime as well as in the many-electron classical regime. To demonstrate the feasibility of the present approach, GaAs Schottky wrap gate (WPG)-based single electron BDD node devices and their integrated circuits were fabricated and their proper operations were confirmed. Selectively grown InGaAs sub-10 nm quantum wires and their hexagonal networks have been investigated to form high-density hexagonal BDD QLSIs operating in the quantum regime at room temperature.

Keywords: Quantum device; Nano-Schottky gate; Hexagonal nanowire network; GaAs; InGaAs; Logic circuit

I. Introduction

Nanoelectronics based on quantum devices is expected to open up new possibilities for the information technology(IT) beyond the scaling limit of the Si-based microelectronics. This is because quantum devices are potentially fastest switching devices with lowest power consumption where the delay-power product is close to the quantum limit set by the Heisenberg's uncertainty principle[1]. Thus, the quantum large-scale integrated circuit (QLSI) technology utilizing quantum devices will become the key technology of future.

Nanoelectronics is needed also as the core technology of nano-sensing, nano-control and nano- processing for the whole area of the emerging nanotechnology covering a much wider than IT, including MEMS, chemistry, biology and medical sciences, and so on.

However, in spite of intensive research on quantum electronic devices over 25 years, there seems to hardly exist realistic approach for large scale and high-density integration of the quantum devices towards QLSIs.

This paper presents the concept, the present status, key issues and future prospects of our novel hexagonal binary decision diagram (BDD) quantum circuit approach for III-V QLSIs. The BDD circuits are implemented on III-V semiconductor hexagonal nanowire networks controlled by nanometer-scale Schottky gates. The basic concept, design, fabrication and characterization of GaAs-based quantum BDD devices and circuits are presented. Then, formation of hexagonal InGaAs nanowire networks by selective growth is also discussed toward high-density integration and room temperature operation of BDD QLSIs.

2. Concept of Novel Quantum Circuits

2.1. Binary-Decision Diagram for QLSI

The present Si logic ULSIs are based on the Boolean logic gate architecture. The gates are realized by arrays of small and robust switching transistors and they require current drivability, a high voltage gain, precise output-to-input voltage matching and uniformity. However, it is difficult to satisfy all these conditions with quantum devices, since they manipulate small number of electrons, and thus they are sensitive and not robust. In order to realize QLSIs, an architecture suitable for quantum devices must be explored.

For this, we have proposed to use a binary-decision diagram (BDD) logic architecture for the QLSIs[2,3]. The BDD architecture was originally proposed by Akers in 1978 as a software tool of logic design on a computer[4]. Its hardware implementation in Si CMOS LSI was investigated by Yano et al.[5] Use of the BDD to single electron circuits was simulated by Asahi et al.[6] The BDD architecture is a representation scheme of a logic function by a directed graph as shown in **Fig. 1(a)**. It consists of many node devices, each labeled by variable, x_i, and a set of end terminals including terminal-1, terminal-0 and roots. The value of the logic function is determined by checking whether the messenger from the root can reach the terminal-1. Any logic function is represented by the layout of the node devices. Each node device has one entry branch and two exit branches as shown in **Fig. 1(b)**. The function of the node device is to switch the path of the messenger either to the 0- or 1-exit branch by gate input variable x_i.

2.2. Hexagonal BDD Quantum Circuit Approach

In our approach, a single electron or a few electrons are used as the messenger, and path switching at each node device is carried out by utilizing single electron transport or coherent

quantum wire transport.

For realization of large arrays of such quantum BDD node devices, we have paid attention to the basic three-fold branch symmetry of the BDD node device, and have proposed[2,3] to use closely packed III-V hexagonal nanowire networks controlled by our novel nano-scale Schottky in-plane gates (IPGs) and wrap gates (WPGs) explained in the next section. The concept is schematically shown in **Fig. 2**. It should be noted that the portions of nanowires other than the node devices are assumed to work as electron reservoirs used for interconnection. The quantum effect or the single electron transport are used only at gated portions for switching. Therefore, it is not necessary to ensure the phase coherence of electron in the entire circuit. Unnecessary interconnection can be cut off either by etching or by a focused ion beam.

It should be also noted that the present QLSI structure is obviously applicable, in future, to molecular nanowire networks or carbon nanotube networks.

Remarkable feature of our approach is that any logic function can be realized without any direct output-to-input connection. This implies that no large voltage gain, no precise input-output voltage matching, no large fan-in and fan-out numbers and no large current drivability are required. It fits fragile quantum devices.

Another unique feature is the circuit will work at ultra-small switching delay-power product near the quantum limit. In the case of a single electron switch[1], the switching time, τ and power, P, are roughly given by $\tau = C/G_0$ and $P = e^2/2C\tau$, where G_0 is the quantized conductance given by e^2/h and C is the dot capacitance, respectively. This makes the product of the switching energy $\Delta E = P\tau$, and the switching time roughly satisfies the Heisenberg's uncertainty principle $\Delta E \bullet \tau \sim \hbar$, realizing the quantum limit. In the case of QWR switch, the operation mode should be adjusted in such a way that each QWR switch operates between 0th and 1st quantized conductance ($2G_0$) in a

complementary way. Then, if, by suitable miniaturization, QWR switching takes place under charging of a small gate capacitance by a few electrons, then the same argument applies and the delay-power product of the node device becomes again close to the quantum limit.

It should be also mentioned that the present BDD quantum circuit node devices perform their proper functions also under non-quantum conditions by acting as many-electron classical path switches. In this sense, the circuit will work at room temperature at the sacrifice of increased delay-power products.

Our approach also has capability of high-density integration due to exploitation of hexagonal closely packed nanowire network. Another unique feature is that the circuits are connected by continuous nanowires and do not have ohmic contacts which are critical in the scaling down of the device size for high density integration. It should be also mentioned that device count for a given logic function is usually smaller in BDD than that in the logic gate architecture[5] and this helps high density integration.

2.3 Quantum BDD node devices and nano-scale Schottky gate technology

The possible equivalent circuit diagrams of the quantum BDD node devices are shown in **Figs. 3(a)-(c)**. They should be realized by suitable gate control of nanowires.

To construct such quantum BDD node devices, our two novel nano-scale Schottky gate technologies shown in **Figs. 4(a)** and **(b)** developed for GaAs- and InP-based materials are most appropriate. One is the Schottky in-plane gate (IPG) structure[7] that has nano-scale Schottky gates on the sides of III-V nanowires. The other is Schottky wrap gate (WPG) structure[8] that the Schottky gates are wrapped around the nanowire. Both structures are lateral structures and suited for high density planar integration. It has been found that both gate structures can realize

much stronger lateral confinement than split gates. Each of the gate structure has unique gate control characteristics[9]. Suitable designs of such blocks realize various types of quantum wire transistors (QWRTrs) and single electron transistors (SETs).

By using the IPG/WPG quantum device technology, various types of quantum BDD node devices can be designed. Four types of devices under investigation[2,3] are shown in **Figs. 5(a)-(d)**. The device in **Fig. 5(a)** is an IPG quantum wire (QWR) Y-switch, and one in **Fig. 5(b)** is a three-WPG single electron Y-switch. Both of these are node-switch type. On the other hand, devices shown in **Fig. 5(c)** and **(d)** are branch-switch type. They consist of a nanowire Y-junction where each of the exit branches has either one QWR switch or one single electron switch, respectively. Each branch-switch is operated in a complimentary fashion. Low current operation by manipulating single electron or a few electron operation of each node device can realize a small delay-power product near the quantum limit. The node-switch device is a more natural selection from the viewpoint of the BDD architecture, however, device size reduction for high temperature operation is much easier in branch-switch type.

3. GaAs-based hexagonal quantum BDD devices and circuits

3.1 Basic operation of the nano-scale Schottky gate-based quantum devices

To confirm the feasibility of the novel nano-scale Schottky gate technology, GaAs-based IPG and WPG quantum devices have been fabricated and characterized. The GaAs nanowires are formed by EB lithography and wet chemical etching. The IPGs are formed using EB lithography and a novel electrochemical process which has metal deposition selectivity[7], and we can successfully form the nano-Schottky gate just on the sidewall of the nanowire. The WPGs have

been formed by the EB lithography, conventional metal deposition and lift-off process.

Both of the GaAs IPG- and WPG-based QWRTrs exhibit excellent gate control characteristics at low temperature up to room temperature as shown in **Fig. 6(a)**. At low drain biases and low temperatures, clear quantization of conductance near pinch-off as shown in **Fig. 6(b)**. The first quantized conductance step has been visible up to 100 K[10] by structure optimization. By switching between conductance steps with gate charging by a few electrons, low power switching near the quantum limit can be realized[11].

The IPG and WPG SETs show conductance oscillations up to 30 - 40 K. The number of peaks is smaller, peak height is voltage and temperature dependent, and peak spacing is not periodic in the IPG and WPG SETs as shown in **Fig. 6(c)** for a WPG SET used as a branch switching in **Fig. 5(d)**. Such behavior can be explained in terms of lateral resonant tunneling of single electron through quantum states in the dot between the tunnel barriers[12]. The tight gate control was confirmed by the 3-gate type WPG SETs with voltage gain larger than unity[13] and the inverter logic gate having signal transfer gain of 1.3 have been successfully formed utilizing the WPG SETs[14,15].

3.2 GaAs-based quantum BDD node devices and their integration on hexagonal nanowire networks

All the devices shown in **Fig. 3** have been fabricated by applying the IPG/WPG control on GaAs etched nanowire pieces. Examples of SEM micrographs of fabricated quantum node devices are shown in **Fig. 7**. The typical nanowire width, W, was 500-700 nm. The gate length, L_G, was 400-600 nm for QWR devices and 50-100 nm for single electron devices, respectively. Each of the node device has shown clear conductance quantization or oscillations as shown in

Figs. 6(b) and **(c)**. With these, clear path switching characteristics such as shown in **Fig. 8** were obtained. The path switching can be realized as shown in **Fig. 8(b)** even at room temperature, since the present IPG and WPG structures can operate as classical FET switches.

In order to see the feasibility of our hexagonal BDD quantum circuit approach, an OR logic function having a BDD graph has been implemented on a single etched hexagon as shown in **Fig. 9(a)**. Here, one three-WPG single electron node-switch and two two-WPG single electron branch-switch are integrated. Note that a branch switch on the right branch is a dummy switch for test, and is not used for OR operation. As shown in **Fig. 9(b)**, this GaAs nanowire hexagon has shown correct logic operations at least up to 120 K by bias adjustments. This is because, with temperature increase, the circuit shows gradual transitions from the single electron quantum regime to a few electron quantum regime, and finally to the many electron classical regime, as already mentioned.

Since the present BDD circuit has much higher input and output impedance with reference to standard 50 Ω measurement systems, it is difficult to measure its speed directly on chip. Simple estimate of switching speed and delay-power product was made. In the case of single electron regime, the charging energy of 2.3 meV obtained from the Coulomb diamond chart of the node device gave a total capacitance of 70 aF. From this value and the observed tunneling conductance value, the delay time was estimated to be $\tau = 1$ nsec. From the drive current of the circuit of 0.1 nA with supply voltage, $V_{DD} = 1$ mV, power consumption was $P = 0.1$ pW. These values result in the $P\tau$ product of 10^{-22} J. This much smaller than the advanced CMOS transistor targeted for 2002 which is 10^{-15} J[19]. On the other hand, in the case of classical regime, the delay time is given by $\sim 1/f_T \sim 2\pi C_G/g_m$, where, C_G is a gate capacitance and g_m is a mutual conductance and the estimated delay time in **Fig.9(c)** is 200 nsec. Then the delay-power product

becomes 100 times larger than that in the single electron regime. In the classical regime, with the increase of the temperature, the current and V_{DD} should be increased for proper circuit operation at higher speeds. Then the power consumption becomes larger, finally approaching those of conventional circuits.

As a next step, we are currently investigating realization of a quantum two-bit adder using two-WPG single electron branch-switches. A hexagonal layout of a two-bit adder graph is shown in **Fig. 10(a)**. This layout has been carefully chosen so as not to include any crossover of nanowires[3]. In principle, any combinatorial logic function can be represented by a gate controlled hexagonal network without wire crossover, because its tree representation can be readily transformed to a BDD logic graph. The key design issue is how to reduce the number of node devices keeping no wire crossover by means of logic simplification and branch sharing. In the case of the layout for the two-bit adder in **Fig. 10(a)**, only 12 single electron branch-switches are required with one-level metalization for gates and terminals without source-drain ohmic electrodes and related metalizations.

The two-bit adder circuit in **Fig. 10(a)** has been fabricated as shown in **Fig. 10(b)**, and the circuit is currently under test. The details will be presented elsewhere[16]. We feel that our hexagonal BDD QLSI approach is a very realistic one and very promising for high density QLSIs.

4. InP-based wire networks toward high temperature operation and high density integration

In order to realize quantum-regime operation of the proposed hexagonal BDD QLSIs at room temperature, stronger quantum confinement in the nanowire network is required. This will

be achieved by the reduction of nanowire widths down to sub-10 nm range. Additionally, for further high-density integration, the hexagon pitch should also be reduced into the nanometer range. For this purpose, a selective MBE growth of InAlAs/InGaAs/InAlAs heterostructure nanowires on InP patterned substrates[18] has been investigated. The cross section of the structure is shown in **Fig. 11(a)**. It can realize completely embedded nanowires with the minimum effective feature sizes down to sub-10 nm. This approach has advantages including smaller wire sizes than the lithography sizes, the position and size controllability, and formation of defect-free high quality heterointerfaces. The self-organized fashion of the selective growth frees from the fluctuation of the structure.

To form hexagonal nanowire networks, the selective MBE growth is carried out on hexagonal mesa-patterns are formed on (001) InP substrates. Low-temperature atomic hydrogen (H*) cleaning of InP patterns and H* irradiation during MBE growth were applied to initial ridge structure formation and was found to be very effective for reducing the nanowire width and enhancing the wire uniformity. A minimum effective nanowire width of 6 nm has been achieved[19]. Overall optimization of the growth process has led recently to a successful formation of a submicron-pitched network structure shown in **Fig. 9(b)** [20]. This structure allows a node device density of 10^8 devices/cm^2, and now the efforts are being made towards the high node device density up to 1G devices/cm^2.

As the nanowire size is reduced, effect of the wire surface becomes increasingly important. Fermi level pinning phenomena deteriorates proper device operation, generates surface related off-set charge problems and causes reliability issues. Intensive efforts to understand and control Fermi level pinning at free surfaces and metal-semiconductor interfaces of III-V semiconductors in nanometer scale[21].

5. Conclusion

A novel hexagonal binary-decision diagram (BDD) quantum circuit approach for III-V quantum large-scale integrated circuits (QLSIs) is presented. The QLSIs based on the combination of hexagonal GaAs nanowire networks, nano-Schottky gates, and the BDD logic architecture have a unique possibility of operation at a delay-power product near the quantum limit.

The feasibility of the present approach was confirmed by the demonstration of GaAs-based quantum BDD node device and OR logic elements. The design and fabrication of a quantum BDD 2-bit adder was also discussed. For constructing hexagonal BDD quantum circuits operating at room temperature, selectively grown InGaAs sub-10 nm hexagonal nanowire networks on InP substrates was investigated.

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Figure captions

Fig.1 (a) BDD logic architecture and (b) BDD node device.

Fig.2 A hexagonal BDD quantum circuit.

Fig.3 Equivalent circuits of quantum BDD node devices. (a) QWR branch switch type, (b) single electron branch switch type and (c) single electron node switch type.

Fig.4 (a) Schottky IPG and (b) WPG structures.

Fig.5 IPG and WPG-based quantum BDD node devices with (a) QWR Y-node switch, (b) single electron node switch, (c) QWR branch switch and (d) single electron branch switch.

Fig.6 (a) I-V characteristics of a WPG structure and conductance characteristics of (b) WPG QWR switch and (c) 2-gate WPG SET switch.

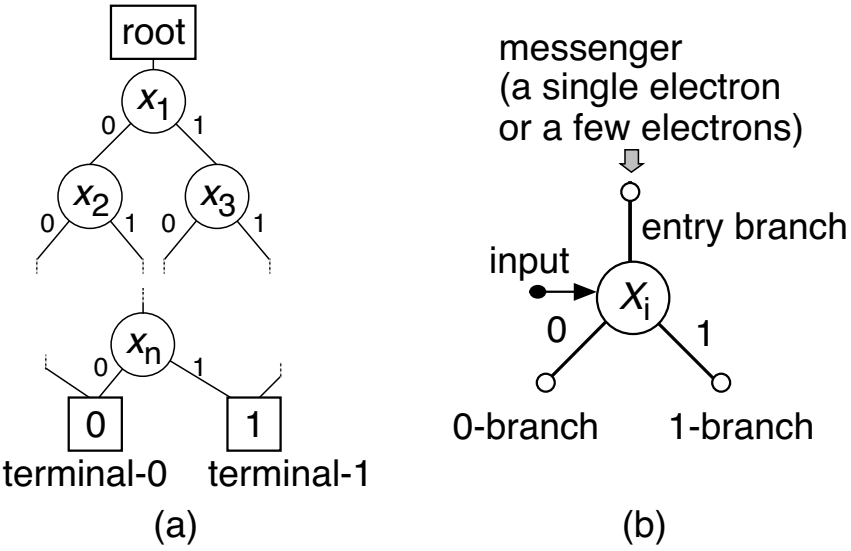
Fig.7 SEM images of (a) WPG QWR branch switch type, (b) single electron branch switch and (c) single electron node switch type BDD node devices.

Fig.8 Switching characteristics of BDD node devices. (a) Single electron node switch type and (b) QWR branch switch type devices.

Fig.9 (a) Fabricated WPG-based BDD OR circuit and their input-output wave forms (b) at 1.6 K and (c) at 120 K.

Fig.10 (a) Circuit diagram and (b) SEM image of a WPG-based BDD 2-bid adder.

Fig.11 (a) Cross section of a selectively grown InGaAs nanowire and (b) a hexagonal nanowire network.



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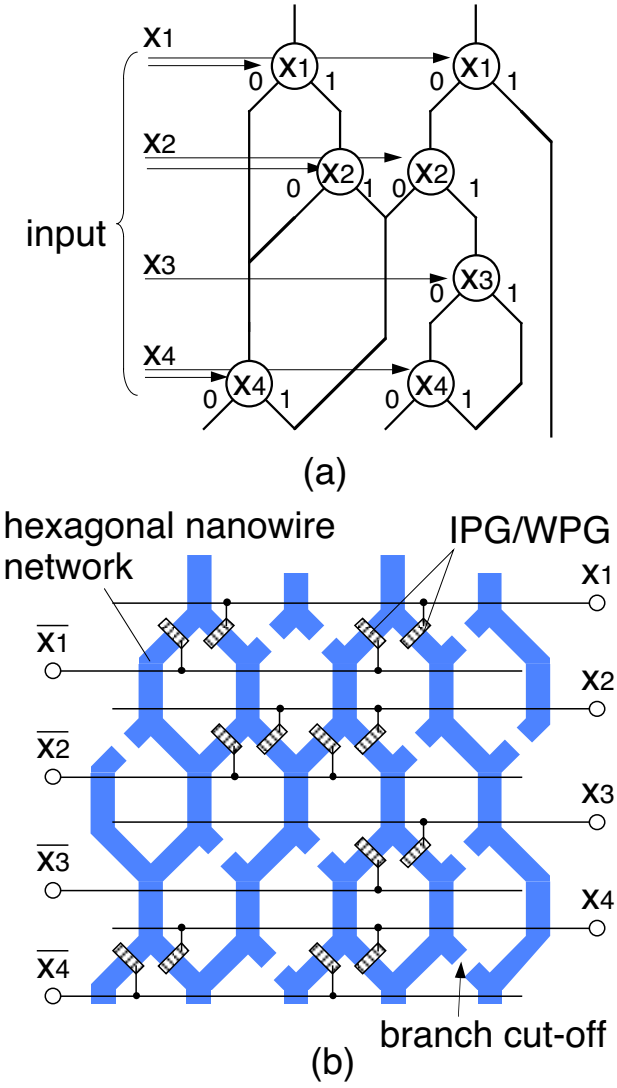

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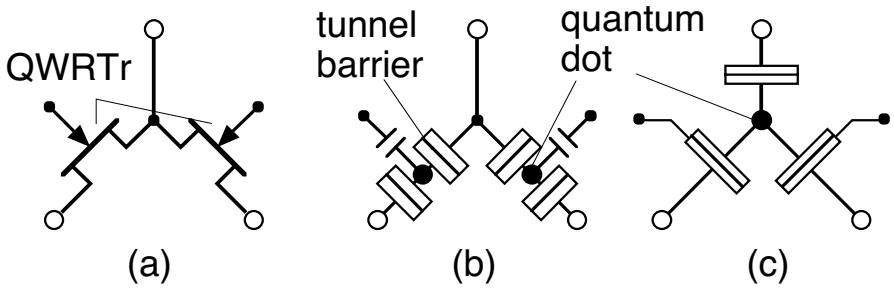

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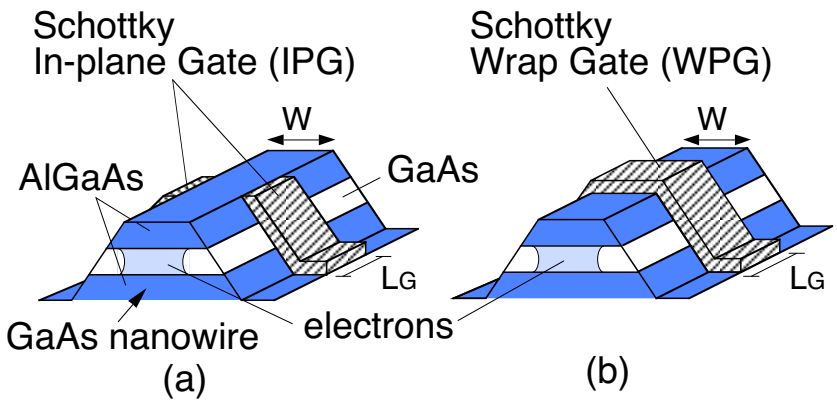

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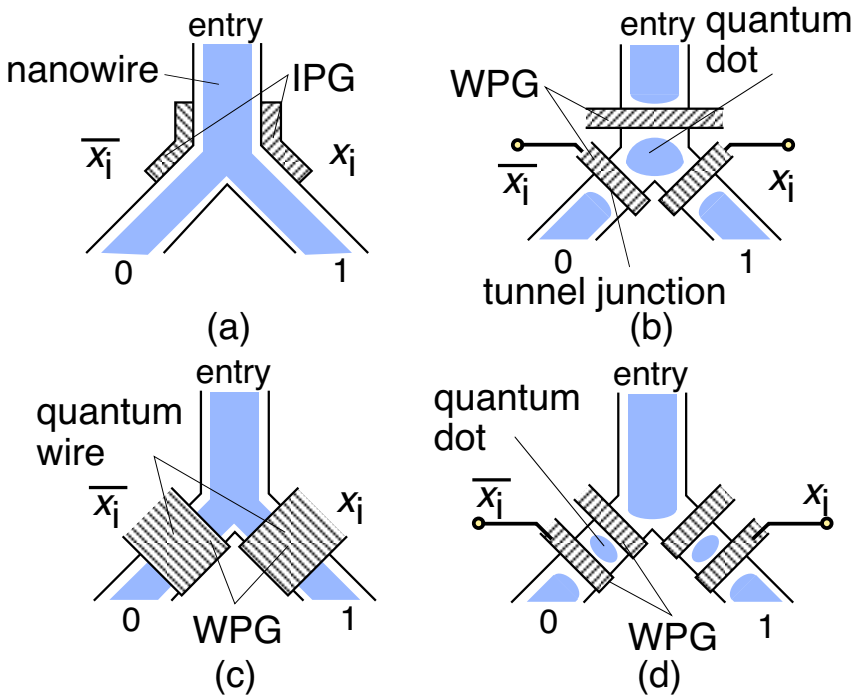

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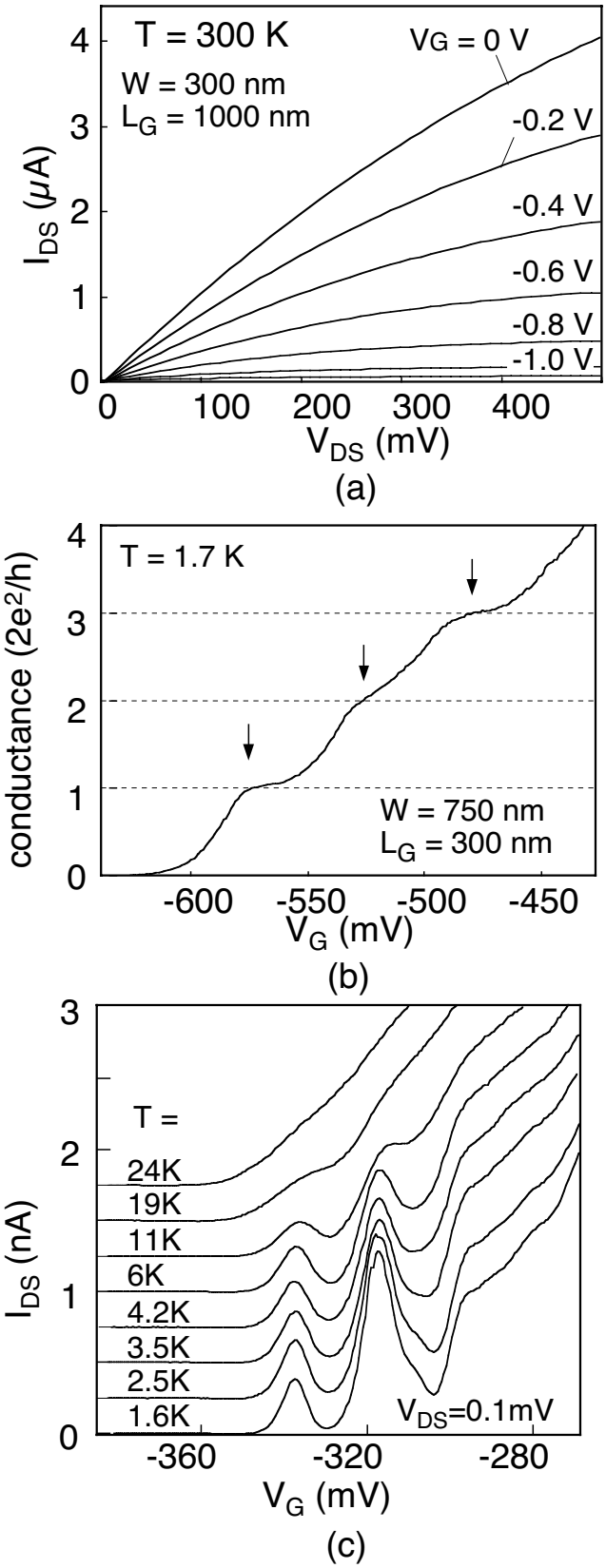

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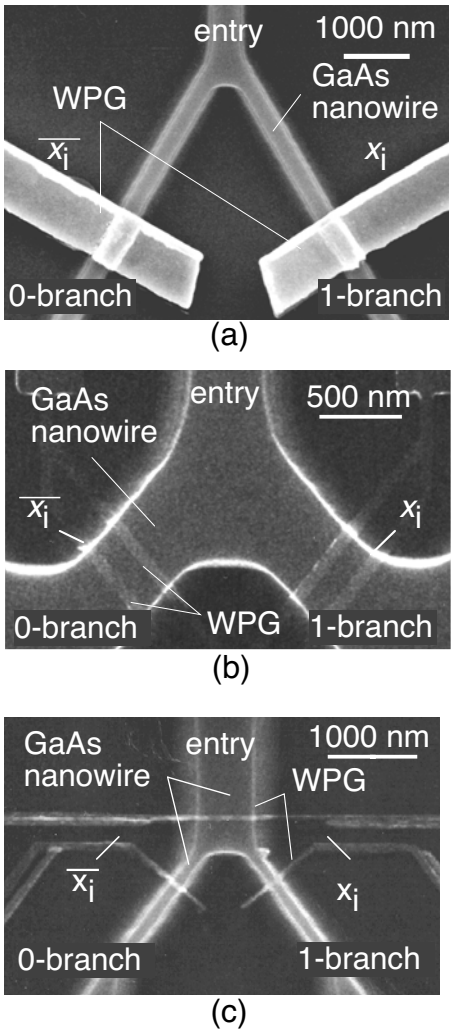
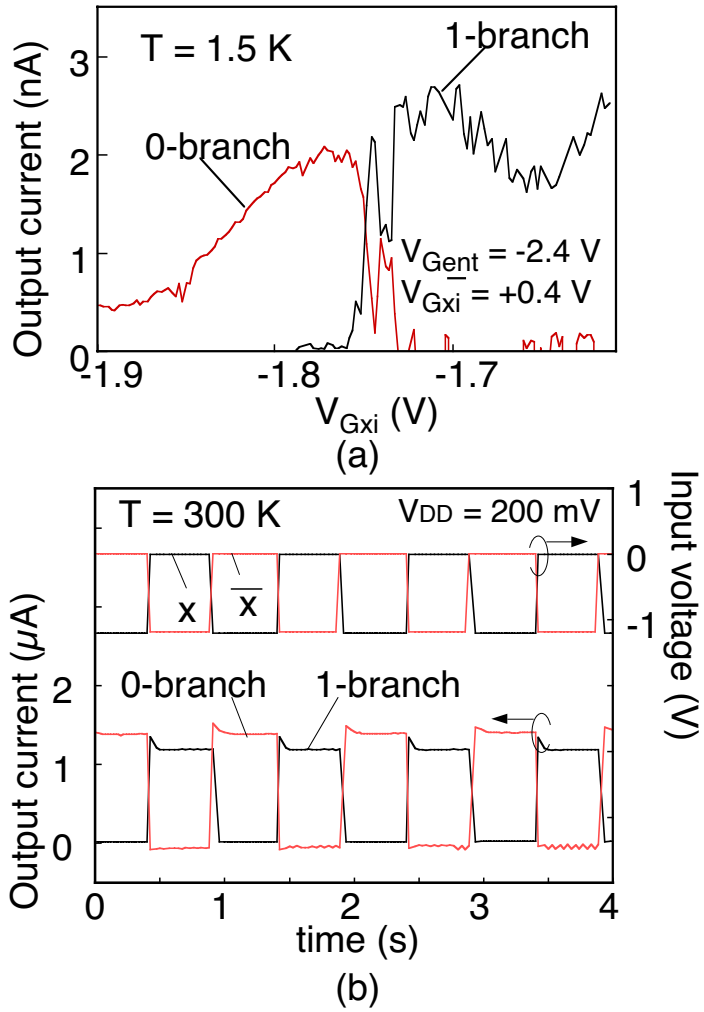


Figure 7 Kasai et al.



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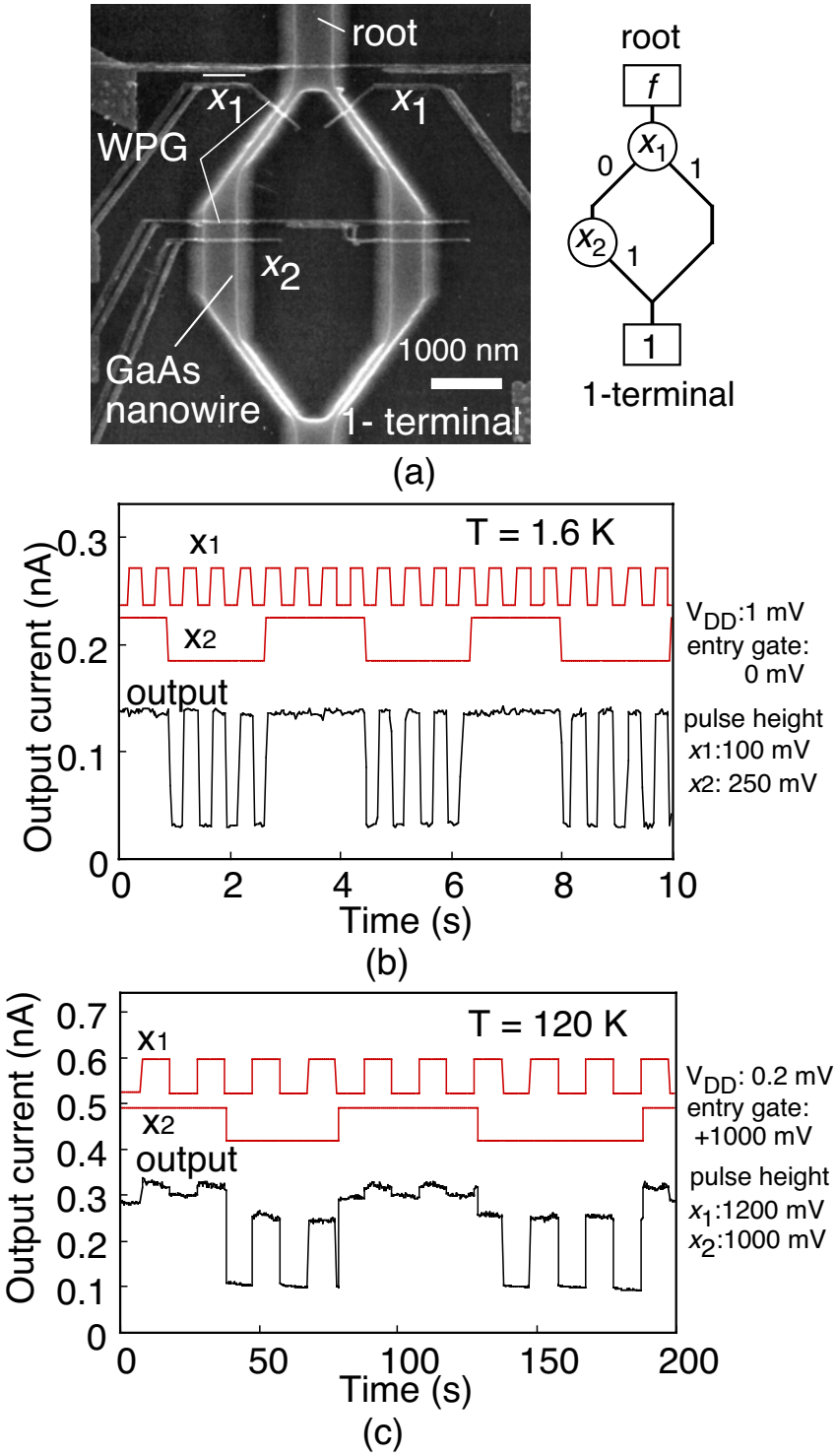

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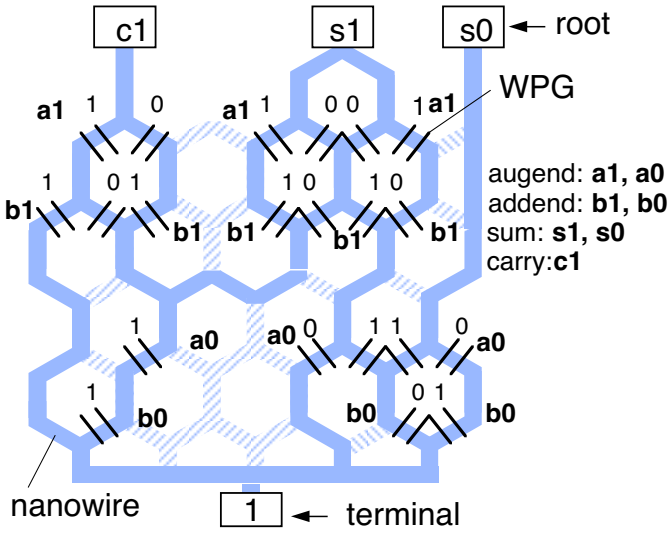

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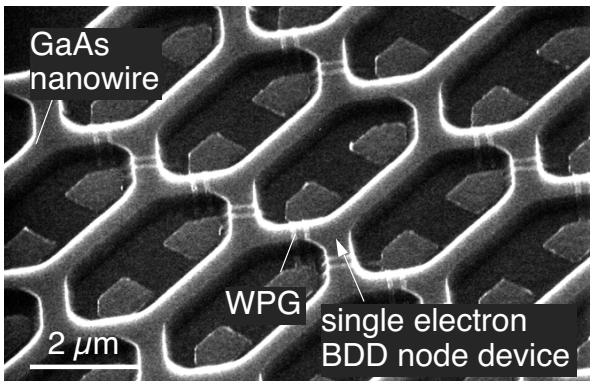

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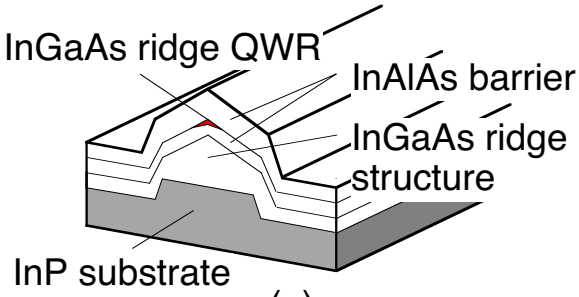

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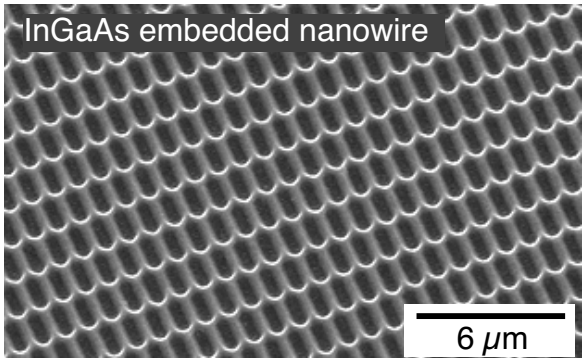

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