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Graph-Based Quantum Logic Circuits and Their Realization by Novel GaAs Multiple Quantum Wire Branch Switches Utilizing Schottky Wrap Gates

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Abstract

A novel approach for quantum logic circuits is described. In this approach, graph-based circuits are directly constructed on nanowire networks and controlled by multiple quantum wire branch switches. Potential advantages of the approach are briefly discussed. A novel GaAs branch switch using a nano-scale Schottky wrap gates (WPGs) on etched AlGaAs/GaAs nanowire was fabricated and its basic control characteristics were investigated. WPG realizes tight gate control of quantum transport near wire pinch off and shows clear conductance quantization at low temperatures. Simple circuits for BDD path switching and AND logic function were then fabricated, and they showed correct operation at low temperature. They could be operated at room temperature by increasing power consumption.

Keywords: Quantum wire; Branch switch; Graph; GaAs; Schottky wrap gate; Logic circuit

1. Introduction

Quantum devices are promising candidates for next-generation high-density and high performance integrated logic circuits. This is because quantum devices can realize a smallest possible value of switching power-delay product (PDP) allowed by quantum mechanics. However, quantum devices are weak and sensitive as compared with Si CMOS transistors. They are inherently not suited to the conventional logic gate architecture where various logic gates such as AND, OR and NOT gates are connected in cascade. In this architecture, large current drivability and threshold voltage (V_{th}) uniformity of the switching device are two key factors. However, quantum devices do not have strong current drivability and uniformity of their V_{th} tends to be poor due to their high sensitivity to off-set charges. For these reasons, there is no well established realistic approach for quantum logic LSIs at present in spite of long research history.

The purpose of this paper is to present a novel realistic approach to overcome this difficulty of quantum devices. Our novel approach is to use nanowire networks with multiple quantum wire (QWR) branch switches to implement graph-based logic architecture. Recently, we discussed a single electron switch version of a similar approach[1]. In this paper, use of QWR-based switches[2] is investigate. Namely, GaAs QWR branch switches controlled by Schottky wrap gate (WPG) were fabricated, and applied to realization of simple circuits for binary decision diagram path switching and AND logic function.

2. A Novel Graph Based Approach for Quantum Circuits and Its Advantages

It is well known in the system theory that a complicated function can be represented by a directed graph network schematically shown in **Fig. 1(a)**. Giving a path selection capability at each node as shown in **Fig. 1(a)**, complicated information transfer can be realized.

Our novel approach is shown **Fig. 1(b)**. The idea is to replace the abstract graph network directly with a physical nanowire network, and to realize path-selection function by multiple QWR branch switches. As shown in **Fig.1 (b)**, each branch switch has a suitable gate and controls the quantum transport within the nanowire in such a way as to cause switching between zero-th and first step of quantized conductance. If

this switching takes place at gate charging by a few electrons, the PDP of switching lies near the quantum limit.

The present approach is a very general one, and by forming suitable network structures, various types of graphs can be directly implemented on hardware. The simplest case of the graph-based approach is to use a Y-switch for two-way path switching at each node as shown in **Fig. 2(a)**. Here, according to the gate input, one of the two exit branches are chosen for the information messenger coming into the entry branch. Such a graph is called binary decision diagram (BDD), first discussed by Akers[3]. BDD can represent any combinational logic function. For hardware implementation of BDD, we have proposed to use a hexagonal nanowire network paying attention to basic three-fold symmetry of the Y-switch[2].

As basic examples, hexagonal nanowire layouts of AND, OR, and exclusive OR logic functions are shown in **Fig. 2(b)**. In each case, logic value of 1 or 0 of the logic function is determined whether the messenger starting from the root terminal reaches termnal-1 or terminal-0. In most cases, the terminal-0 can be omitted for simplicity, and the logic value is then determined whether there is electrical connection between the root terminal and the terminal-1, or not. As a more complicated logic circuit, a hexagonal layout of two-bit adder without wire cross-over was discussed previously[2]. It was found that the number of branch switches required for a BDD 2-bit adder is 21 whereas the standard Si CMOS implementation requires 42 transistors.

The expected advantages of our approach can be summarized as follows.

1) Power delay product near quantum limit can be realized.

2) No voltage gain is required.

3) No large current drivability is required.

4) High density due to the hexagonal close packed nanowire structure.

5) Device count is generally smaller than that for the logic gate architecture.

6) Average interconnection length is short, because ungated portion of nanowire network is used as interconnects.

7) Source/drain electrodes are not necessary within the network, thereby solving contact problem.

8) Only one gate metalization level is necessary in addition to terminals.

3. Fabrication and Characterization of a GaAs-based QWR Branch Switch

In order to test the feasibility of our approach, GaAs-based QWR branch switches were fabricated using the Schottky WPG technology developed by our group[4]. The structure of a single branch switch is shown in **Fig. 3(a)**. A nano-scale WPG electrode is wrapped around an AlGaAs/GaAs nanowire having a trapezoidal cross-section. The WPG constricts electrons into a narrow region in the nanowire and realizes one-dimensional quantum transport. As compared with the standard split gate structure, the WPG can realize much stronger confinement.

The sequence of the device fabrication was the following.

1) AlGaAs/GaAs heterostructure were grown by molecular beam epitaxy.

2) AlGaAs/GaAs nanowires were formed by electron beam lithography and wet chemical etching.

3) Terminal electrodes were formed by Ge/Au/Ni ohmic contact metalization.

4) Cr/Au Schottky WPGs were formed by EB lithography-based lift-off process.

In order to understand the gate control characteristics of WPG, the effective wire width under gate depletion was characterized as a function of gate voltage, using Shubnikov-de Haas oscillation measurements. The wire width was determined by fitting theoretical curves based on harmonic potential approximation to measured Landau plots. Theoretical effective wire width were also determined by a three-dimensional potential simulation on computer. As shown in **Fig. 3(b)**, experimental and theoretical curves agreed reasonably well. To obtain such agreement, it was necessary to assume that strong Fermi level pinning exists on the semiconductor free surface surrounding the gate. The calculation has also shown that threshold voltage is strongly influenced by the gate length, L_G, similarly to the so-called short channel effect in classical field effect transistors.

The fabricated GaAs QWR branch switches showed good control characteristics at low temperatures up to room temperature (RT). At low temperatures, the device showed clear conductance quantization as shown in **Fig. 3(c)**.

4. Fabrication of Simple Nanowire Circuits with Multiple Branch Switches

In the next step, we fabricated a QWR Y-switch having two branch switches. The

device showed clear path switching behavior, however, the heights of the conductance steps were somewhat smaller than the ideal value of $2e^2/h$. This was attribute to reflection of electron waves.

In order to investigate feasibility of the present graph-based approach for realization of logic functions, we fabricated a simple circuit which performs AND logic function according to a hexagonal BDD layout shown in **Fig. 2(b)**. The output waveform measured under pulsed condition at 1.6K is shown in **Fig. 4(a)**. It shows correct operation. The each switch showed clear path switching even at RT and the circuit also operated at RT as shown in **Fig. 4(b)**. This is because the device operation changes gradually from a few electron quantum regime to the many electron classical regime with increase of temperature. However, it should be noted that operation at RT is only possible at an increased value of power consumption.

Finally, a rough estimate of the PDP value of present QWR branch switches with L_G = 630 nm was made, using the QWR line density of carries from Landau plots, gate voltage swings, measured conductance etc. It gave a PDP value of 10^{-18} J at 1.6 K. It was one order of magnitude smaller than the best value of the latest Si CMOS transistor with L_G = 20 nm at 300 K[5]. However, the estimated PDP value of our device is still far away from the quantum limit due to the fact that more than one thousand electrons are required to charge the WPG having L_G = 630 nm. By reducing the gate length, a further large improvement should be possible.

5. Conclusions

A novel approach for quantum logic circuits based on graph-based circuits on nanowire networks controlled by multiple QWR branch switches is described. Its basic feasibility has been demonstrated by fabrication and characterization of GaAs branch switches and their simple circuits using WPGs. In order to operate proposed circuits in the quantum regime at room temperature, the width of the nanowire should be reduced in future from the present value of several 100 nm down to a value below 10 nm.

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Figure Captions

Fig. 1. (a) Basic concept of directed graph architecture and (b) implementation by QWR multi branch switches.

Fig. 2. (a) Y-switch and (b) examples of hexagonal nanowire layouts of AND, OR, and Exclusive OR

Fig. 3. (a) Basic structure of WPG, (b) its wire width control and (c) quantized conductance.

Fig. 4. AND circuit operation (a) at 1.6 K and (b) 300 K.

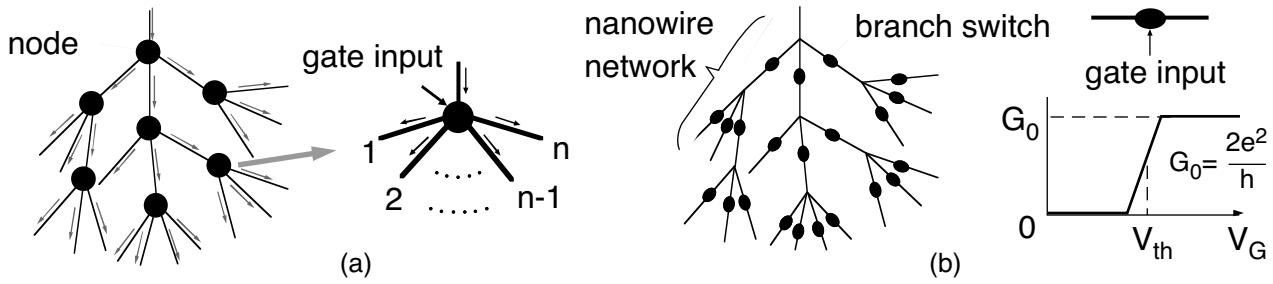
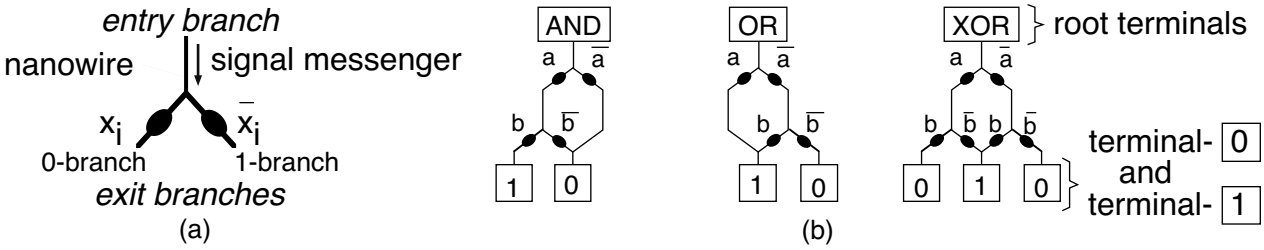


Figure 1 M. Yumoto et al.



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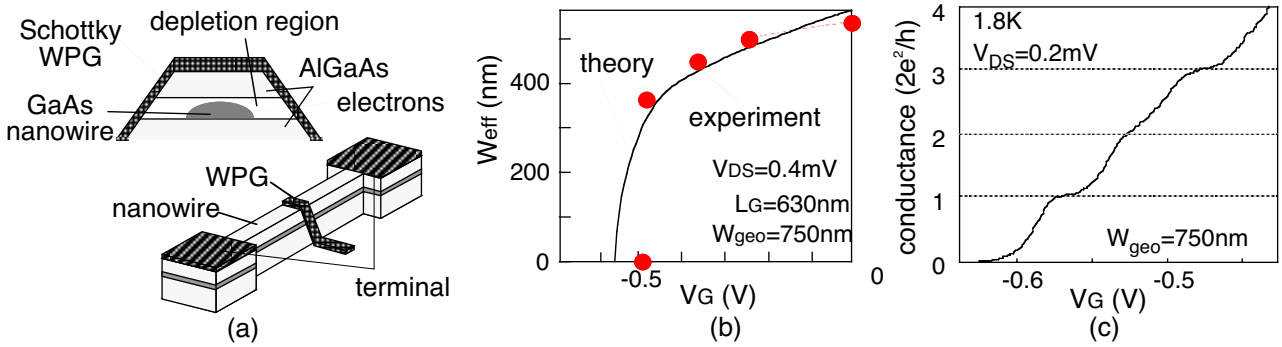

Figure 3 M. Yumoto et al.

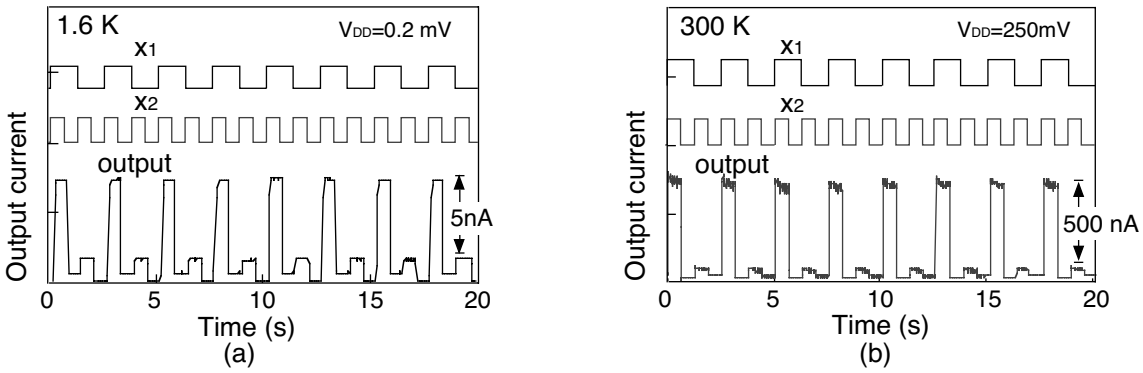

Figure 4 M. Yumoto et al.