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Hexagonal Binary Decision Diagram Quantum Logic Circuits Using Schottky In-Plane and Wrap Gate Control of GaAs and InGaAs Nanowires

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Abstract

Previous quantum device research has been done on discrete device levels and lacks a clear vision for high density integration. This paper proposes a new, simple and realistic approach for quantum large scale integrated circuits (QLSIs) where a binary-decision diagram (BDD) logic architecture is implemented by BDD node devices based on quantum wire transistors (QWTrs) and single electron transistors (SETs) realized by the Schottky in-plane gate (IPG) and wrap-gate (WPG) control of III-V hexagonal nanowire networks. To investigate the feasibility of the proposed approach, BDD devices having QWTrs were formed on GaAs/AlGaAs etched nanowire patterns. They showed expected complimentary quantized conductance switching as required to achieve operation at delay-power products near the quantum limit. Use of embedded InGaAs honeycomb wire networks grown by selective MBE on InP substrates is proposed for constructing circuits operating in quantum regime at room temperature.

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Keywords: binary decision diagram (BDD), quantum wire transistor, III-V semiconductor, Schottky in-plane gate, Schottky wrap gate

1. Introduction

The nanofabrication technology has opened up exciting possibilities of constructing novel quantum devices based directly on quantum-mechanical motions of electrons within artificial quantum structures. This may eventually create non-dissipative quantum coherent circuits dealing with a large number of qu-bits for quantum computation, teleportation and information processing. However, at the present, such circuits are extremely difficult to realize as solid-state circuits due to rapid decoherence even at very low temperatures.

On the other hand, energy dissipative switching devices in quantum regime can be constructed much more easily. They are potentially fastest switching devices with smallest power consumption, because their operation should approach the minimum possible delay-power product set by the Heisenberg's uncertainty principle (the quantum limit for switching) by a proper device structure and design. However, previous research has been done on discrete device levels without any clear vision on high density integration, although quantum devices are useful only at a high integration level.

The purpose of the present paper is to propose a new, simple and realistic approach for quantum large scale integrated circuits (QLSIs) consisting of quantum wire transistor (QWTr) and single electron transistor (SET) arrays. The idea is to implement a binary-decision diagram (BDD) logic architecture by arrays of QWTrs and SETs based on nano-Schottky in-plane gate (IPG) or wrap gate (WPG) control of III-V honeycomb nanowire networks.

2. BDD Logic Architecture Implementation for QLSIs

Judging from delicate nature of quantum devices, it is intuitively better to create a novel logic architecture for QLISs rather than sticking to the conventional Boolean logic gate architecture, as indicated by a pioneering work on quantum cellular automata [1]. We propose in this paper to implement a binary-decision diagram (BDD) logic architecture by hexagonal arrays of QWTrs and SETs. The BDD logic architecture was first proposed by Asahi *et al.*[2,3] for single electron devices. Here, as shown in Fig.1, a logic function is represented by a directed graph consisting of many wired node devices, each labeled by input variable, x_i , and a set of end terminals including terminal-1, terminal-0 and roots. The function of the node device is to switch the path of the information messenger according to the value of the input variable x_i . Then, the value of the logic function is either 1 or 0 depending whether the messenger from the root can reach the terminal-1 or the terminal-0. The terminal-0 can be omitted for layout simplicity.

In the conventional logic gate architecture, direct output-to-input connections of gates are necessary with a precise voltage level matching, reproduction of sharp on-off transient by

a large voltage gain and satisfaction of fan-in and fan-out requirements. In the BDD architecture, no cascade connection of node devices is made, therefore, none of voltage matching, large voltage gain and large drivability are necessary. Therefore, it is best suited to quantum devices such as QWTrs and SETs.

3. BDD Devices Based on Nano-Schottky Gate Quantum Wire Transistors

For construction of quantum BDD node devices, a single electron or a few electrons can be used as the information messenger, taking advantage of high charge sensitivity of quantum phenomena. Here, we propose to use nanowire-based BDD node devices shown in Fig.1(b). It consists of a wire Y-junction having entry and exit branches and two QWTrs or SETs that are placed in the exit branches and operated in a complimentary fashion. Here, it is assumed that quantum transport takes place only in the QWTr or SET and the rest of the structure including the node junction acts as classical electron reservoirs, so that the path conductance is limited predominantly by the conductance of QWTr or SET. In the case of SET, the delay-power product is known to lie close to the quantum limit. In the case of QWTr, the operation mode should be adjusted in such a way that each QWTr switches between zero-th and 1st quantized conductance in a complementary way as schematically shown in Fig.1(c). Then, if, by suitable miniaturization, QWTr switching takes place under charging of a small gate capacitance, C_G , by a few electrons, the delay-power product of the node device becomes again close to the quantum limit.

It should be noted that the node devices perform their proper function also under non-quantum conditions, acting as a many-electron classical path switch. In this sense, the circuit will work at room temperature. The point is that the delay-power product can be minimized to the quantum limit by operating the switch in the single or few electron quantum regime.

As for the device technology to produce node devices shown in Fig.2(b), we used our scheme based on nanometer scale Schottky gate control of nanowires. Here, GaAs etched nanowires such as shown in Fig.2(a) are controlled either by the Schottky in-plane gate (IPG)[4] shown in Fig.2(b) or by Schottky wrap gate (WPG)[5] shown in Fig.2(c). This has led to realization of various quantum devices on GaAs nanowires[6], including single and coupled QWTrs, SETs, a resistive load and a complementary GaAs single electron logic inverters[7]. Based on these, we have recently proposed a GaAs single electron BDD node device sitting at each Y-junction node and controlled by three WPGs, and demonstrated its basic operation[8]. However, quantum transport and reflection and in such SET-based or QWTr-based Y-switches will depend sensitively on material and structural details of devices,

making it practically impossible to achieve Y-switches that are small and uniform enough for high-temperature operation and large scale integration.

In order to test the feasibility of the proposed approach, quantum BDD node devices having IPG/WPG QWTrs were fabricated in this study. First, etched GaAs nanowires with width of several 100 nm were formed on MBE-grown AlGaAs/GaAs/AlGaAs 2DEG wafers by EB lithography and wet chemical etching. Then, IPGs and WPGs were formed. An example of SEM photograph of a WPG QWTr-based BDD node device is shown in Fig.3(a). It should be mentioned that one puts two short WPGs in stead of one, the device will work as an SET shown on the right of Fig.1(b), as we have already shown[5,7].

Gate dependent Shubnikov-de Hass (SdH) measurements showed that the wire width depletion characteristics of these gates against the gate voltage, V_G , are very different, as schematically shown in Fig.3(b). It was also found that both gate structures can realize much stronger lateral confinement than the conventional split gate structure.

Both type of BDD devices having IPG and WPG QWTrs showed excellent gate control characteristics from 1.5K up to 300K, as shown in Fig.4(a) and (b), respectively. At low temperatures, they showed clear conductance quantization near pinch off as shown in Fig.4(c) and (d), respectively. The result confirmed the feasibility of complimentary quantized conductance switching up to 20-30 K.

4. Formation of Quantum Wire Networks for BDD QLSIs

To realize a large scale BDD QLSIs operating in quantum regime at room temperature, a nanowire network structure suitable for BDD graphs should be developed and the wire width should be reduced down below 10 nm. Both are obviously difficult to realize by etched GaAs nanowires due to lithography limitation and chemical etching anisotropy.

We propose here to use networks formed by completely embedded InAlAs/InGaAs/InAlAs nanowires shown in Fig.5(a) which is grown by atomic hydrogen assisted selective MBE growth on patterned InP substrates. Using this, we have already realized arrays of wires, dots, and wire-dot coupled structures[6,9]. This approach has the advantage of realizing position and size controlled wires with widths that are smaller than the lithography size, being unaffected by lithography size fluctuation.

As for the circuit topology, we propose here to use a hexagonal nanowire network structure for high density of BDD graphs, judging from the basic three-fold symmetry of the node branches seen in Fig.1(a). As an example, a gated honeycomb layout of a two-bit adder graph is shown in Fig.5(b). It should be noted that this layout was carefully made not to include any cross-over of wires. This is important because formation of electrical contacts to

narrow embedded wires and effectively realize wire cross-over by metallization requires an additional process sophistication, although it is feasible.

Since the BDD logic architecture can be regarded basically as tree representations of binary logic functions, any combinatorial logic function can be implemented by gated honeycomb networks without wire cross-over. The key design issue is how to reduce the number of node devices and that of branches down to practically acceptable numbers in large logic systems by means of logic simplification and branch sharing. There does not seem to exist a general answer to this question at present, and requires a future research effort. An encouraging indication for us is that the BDD layout for the two-bit adder in Fig.5(b) requires only 12 QWTrs with one-level metallization for gates and terminals, and without any source-drain ohmic electrodes and related metallizations. In contrast, a typical Si CMOS implementation using XOR-NAND gates requires 42 MOS transistors with source-drain electrodes and two-level metallizations with cross-overs. This advantage continues to n-bit adders, n-bit multipliers, etc. Thus, we expect that the present approach will give reasonable results for large random logic systems, if a suitable design methodology is developed.

Another important question related to the proposed hexagonal BDD QLSIs is the bit error rates (BER) of such quantum circuits. For this, a computer simulation of a single electron version of the 2-bit adder similar to Fig.5(b) has been made recently by Kinoshita et al[10]. According to this result, the sources for bit errors are inherent quantum mechanical stochastic fluctuation of electron transport, fluctuation due to branch sharing, and thermal fluctuation of electrons. Actual value of BER thus depends strongly on many parameters involved. As an example, it has been shown that, using the layout shown in Fig.5(b) and assuming typical capacitance values of our present GaAs devices of 20-30 aF and tunneling resistance of 1 M ohm, BER values below 10^{-9} can be achieved up to 20K, if one uses a flow of 30 single electrons or so to represent 1 bit with a suitable averaging device.

For construction of the proposed hexagonal BDD QLSIs, high density honeycomb nanowire networks are required. In order to form such structures by selective MBE growth, various substrate patterns have been tried. This has led recently to successful formation of a submicron-pitched structure shown in Fig.5(c) whose details are discussed elsewhere[11]. This structure should allow a node device density of 10^8 devices/cm². As for the wire width reduction, we have realized a wire width of 6 nm by introducing atomic hydrogen cleaning of the InP pattern[12].

Thus, in conclusion, the proposed hexagonal BDD QLSI approach which implements BDD logic architecture by honeycomb nanowire networks controlled by IPG/WPG gates technology seems to be very promising for high density QLSIs that are operating at

delay-power products near the quantum limit at room temperature.

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Figure captions

Fig.1 (a) BDD logic architecture, (b) novel BDD node devices based on QWTrs and SETs, and (c) operation of each QWTr in quantum regime.

Fig.2 (a) GaAs etched nanowire, (b) and (c) structures of the IPG and WPG QWTrs gated nanowires.

Fig.3 (a) Photograph of a fabricated WPG QWTr-based BDD node device and (b) schematic comparison of gate control characteristics of wire width for IPG and WPG structures.

Fig.4 (a), (b) I-V characteristics of IPG and WPG BDD branch QWTrs, and (c),(d) their conductance switching behaviors, respectively.

Fig.5(a) Embedded InGaAs nanowires by selective MBE, (b) a honeycomb layout of a two-bit adder and (c) a honeycomb wire network by selective MBE.

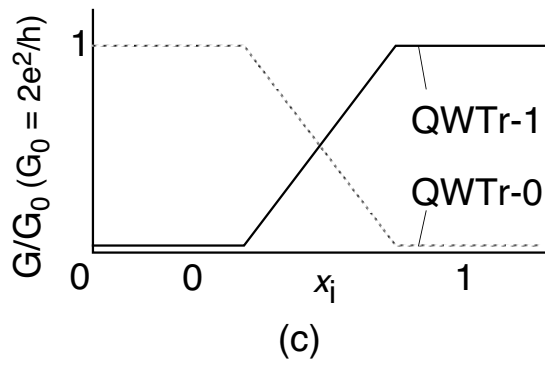
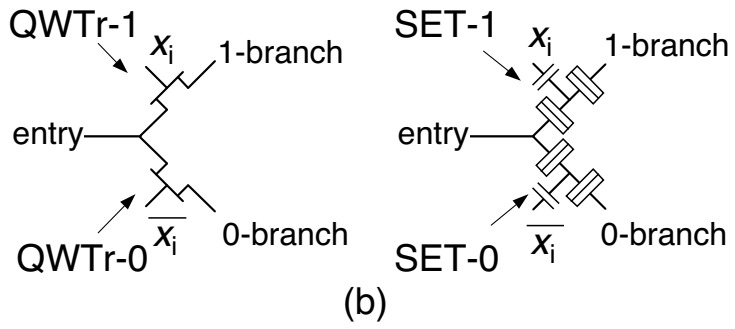
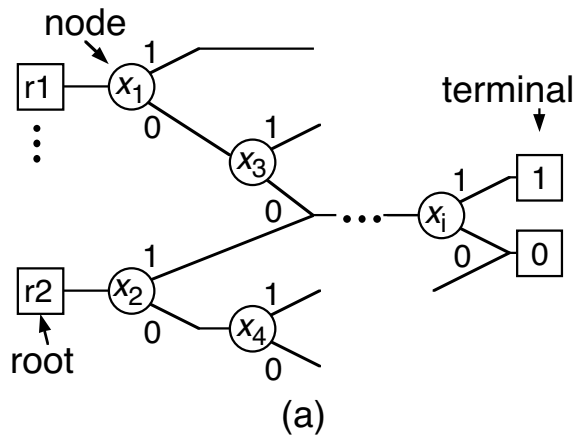
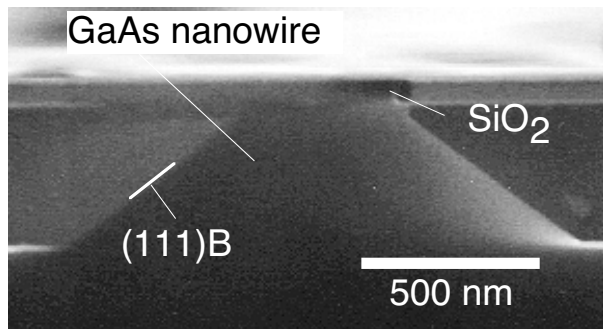
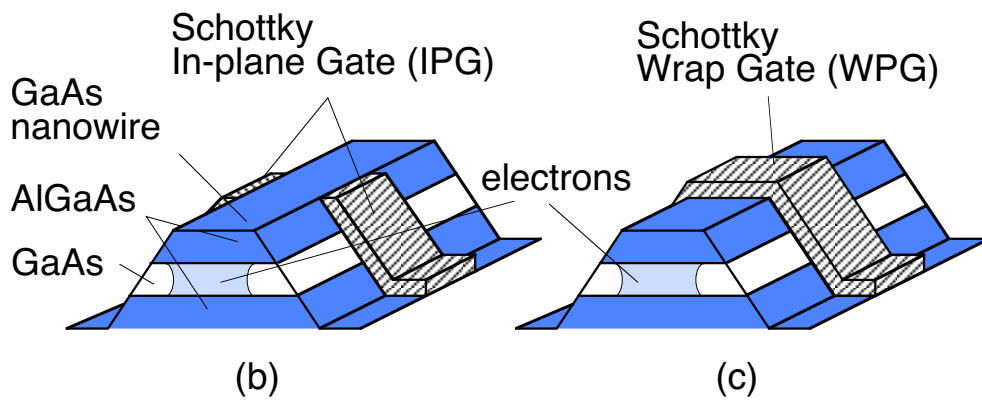


Figure 1 H. Hasegawa



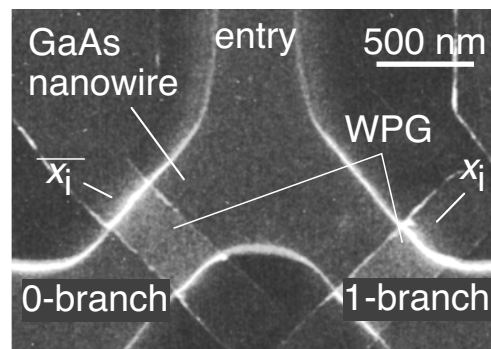
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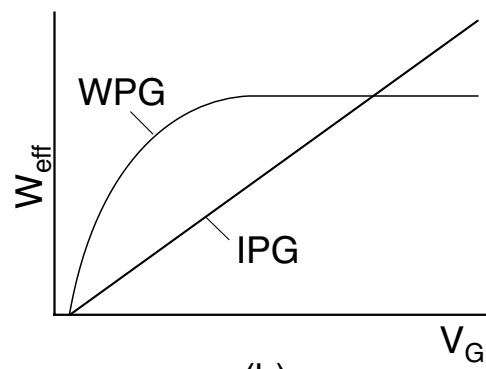
(b)

(c)

Figure 2 H. Hasegawa



(a)



(b)

Figure 3 H. Hasegawa

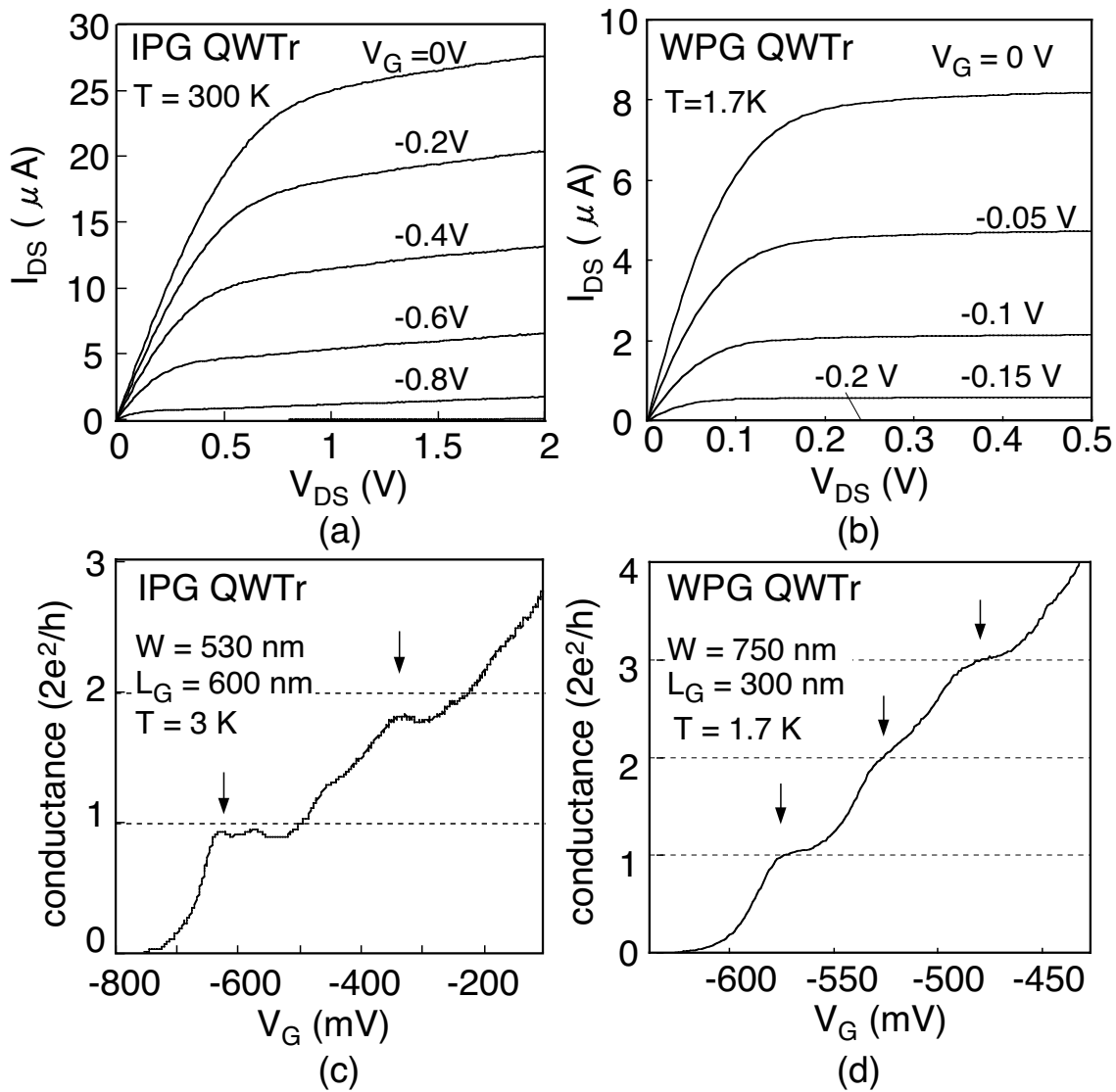
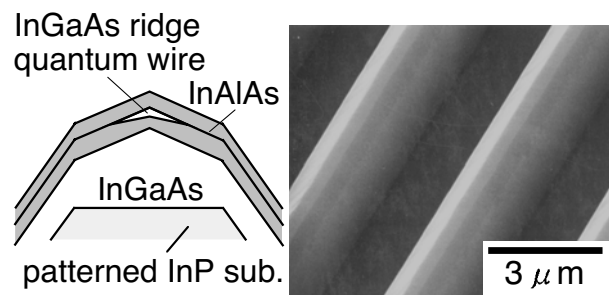
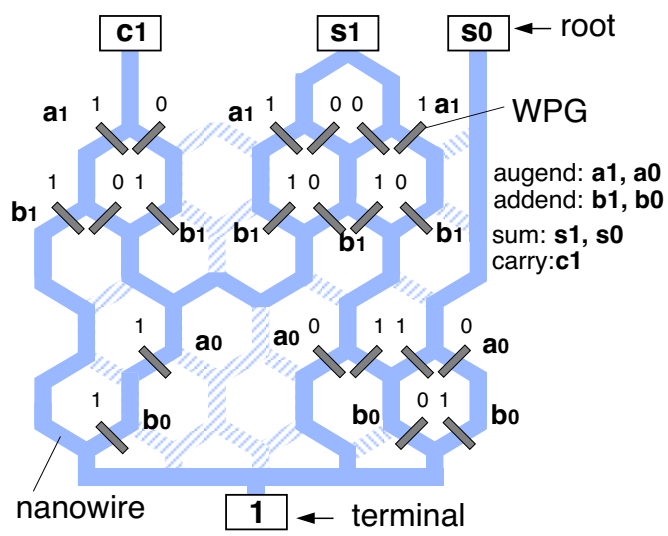


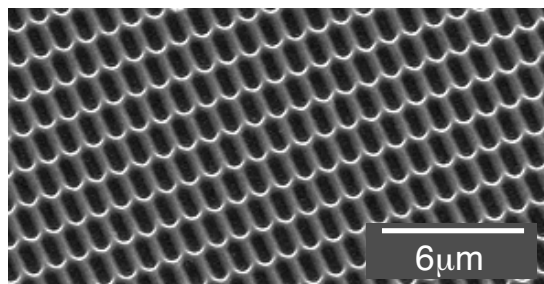
Figure 4 H. Hasegawa



(a)



(b)



(c)

Figure 5 H. Hasegawa