Optimization of Two-Dimensional Channel Thickness in Nanometer-Thick SnO_2-Based Top-Gated Thin-Film Transistors using Electric Field Thermopower Modulation: Implications for Flat-Panel Displays

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ABSTRACT: Transparent amorphous oxide semiconductors (TAOSs) based thin-film transistors (TFTs) are essential as the backplane for developing advanced flat panel displays. Among many TAOSs, amorphous (a-) SnO_2 is promising active material due to its abundance compared with the state-of-the-art a-$InGaZnO_4$. However, practical application of a-SnO_2-based TFTs has not been realized because of its unstable transistor characteristics coming from the high residual carrier concentration. Precise optimization of the two-dimensional channel thickness is required to stabilize the transistor characteristics of a-SnO_2-based TFTs. Here we use the electric field thermopower modulation analyses to show the two-dimensional channel thickness of a-SnO_2 for TFT can be optimized at ~2 nm. After the optimization of the channel thickness, we reduced the thickness of HfO_2 gate insulator film to further improve the transistor characteristics. The resultant TFT exhibited excellent transistor characteristics; on-to-off current ratio of ~10^5, normally off behavior (V_{th} ~+0.65 V), small subthreshold swing of ~230 mV/decade, high mobility (~10 $cm^2\ V^{-1}\ s^{-1}$), and stability in changing oxygen atmospheres. The present results would bring further possibilities for the development of next-generation low-cost and low-power electronic devices.

KEYWORDS: electric field thermopower modulation, effective channel thickness, amorphous SnO_2, Top-gated thin-film transistor, HfO_2 gate insulator

Transparent amorphous oxide semiconductors (TAOSs) are excellent materials as the two-dimensional channel for thin-film transistors (TFTs) owing to their high mobility, good uniformity over large area, and low fabrication temperature. Currently, amorphous (a-) $InGaZnO_4$-based TFT is widely applied as a backplane of commercially available organic light-emitting diode (OLED) displays due to its higher field-effect mobility (μ_{FE}) of ~10 $cm^2\ V^{-1}\ s^{-1}$, which is two orders of magnitude higher than that of a-Si.[1-4] Since indium is a rare metal, the low abundance in the earth's crust making it's not desirable for large-scale commercial applications. Therefore, it is urgent to find alternative high-performance materials with abundant composition elements and low cost.

Among many TAOSs, amorphous a-SnO_2 is promising active material because of high abundance compared to the state-of-the-art a-$InGaZnO_4$. SnO_2 is a transparent n-type oxide semiconductor with a wide bandgap (~3.6 eV).[5] The large overlap of its Sn 5s orbitals make it possible for SnO_2 to exhibit good electrical properties regardless of its crystallinity.[6] Therefore, many researchers tried to develop a-SnO_2-based TFTs with good

transistor characteristics.[7-8] However, reported a-SnO_2-based TFTs showed unstable transistor characteristics showing unusually high field-effect mobility (μ_{FE} > 100 cm^2 V^{-1} s^{-1})[9-12] with relatively high off current due to high residual sheet carrier concentration. Further, most of the reported TFTs were bottom-gate top-contact type, where the top surface of the a-SnO_2 channel was exposed to the atmosphere. This causes a stability issue since a-SnO_2 adsorbs oxygen gas on the surface, and carrier depletion occurs ~3 nm in depth.[13-14]

In order to overcome this difficulty, a-SnO_2-based TFTs with top-gate bottom-contact type would be preferable because the surface of a-SnO_2 channel is fully covered with dense insulators. In this regard, one remaining problem is that the residual carrier concentration of a-SnO_2 is extremely high (~10^{19} cm^{-3}) and difficult to reduce. Therefore, the thickness of the two-dimensional channel must be reduced to decrease the carrier concentration, so that transistor can be operated. This can be achieved with the channel thickness optimization using the electric field thermopower modulation analyses. By using this method, the electric field accumulated sheet carrier concentration (n_s) dependence of thermopower (S) can be clarified. With measured the relationship of films carrier concentration (n_{3D}) and S, the effective channel thickness (t_{eff}) of the TFT can be

extracted as $t_{eff} \equiv n_s/n_{3D}$. Hence, the electric field thermopower modulation method is useful to clarify the t_{eff} and the thickness of depletion layer of the TFTs. The optimum channel thickness can be further determined. It should be noted that *S* is insensitive to the film quality unlike the mobility. Previously, we analyzed the depletion layer thickness of the bottom-gate top-contact a-SnO_2 TFTs by the electric field thermopower modulation analyses and clarified that the depletion layer thickness was ~2.5 nm.[15]

Here we show the optimization and characterization of a-SnO_2 TFTs. Firstly, we precisely deposited 3-nm-thick a-SnO_2 film by pulsed laser deposition (PLD) technique; By ablating the SnO_2 ceramic target with focused KrF excimer laser in the vacuum chamber, the film thickness of a-SnO_2 can be controlled in sub-nanometer order. Then, we fabricated the TFT structure on the film (Figure 1). From the electric field thermopower modulation analyses of the 3-nm-thick a-SnO_2 TFT, we optimized the thickness of SnO_2 channel (~2 nm). Then, we reduced the thickness of HfO_2 gate insulator film to improve the transistor characteristics of top-gated a-SnO_2 TFTs. The resultant TFT exhibited excellent transistor characteristics; on-to-off current ratio of ~10^5, normally off behavior (V_{th} ~+0.65 V), small subthreshold swing of ~230 mV/decade, high mobility (~10 cm^2 V^{-1} s^{-1}), and stability in changing oxygen atmosphere. The present results would bring

further possibilities for the development of next-generation low-cost and low-power electronic devices.

We fabricated the top-gated a-SnO_2 TFT without using any wet process. We used stencil masks to fabricate the TFT structures. Figure 2(a) shows the schematic illustration of the top-gated a-SnO_2 TFT. a-HfO_2 was used as the gate dielectric (permittivity, $\varepsilon_r = 21-23$[16]). We expected that the gate voltage can be reduced significantly. The channel length L was 200 μm, and the width W was 400 μm. The resultant TFTs were fully transparent in visible region as shown in Figure 2(b). The detail of our experimental setup is described in the Methods Section.

The transistor characteristics of the a-SnO_2 TFTs were measured at room temperature in a dark shield box using a semiconductor device analyzer (B1500A, Agilent). Figure 3(a) shows the transfer (I_d-V_g) characteristics of the 3-nm-thick a-SnO_2 TFT with a 160-nm-thick HfO_2 gate insulator. The on-to-off current ratio was only 6 most likely due to large residual sheet carrier concentration (n_s) [Figure S1(c)], which was deduced from $n_s = C_i \cdot (V_g - V_{th}) \cdot e^{-1}$ where C_i is the capacitance per unit area (C_i ~120 nF cm^{-2}) [Fig. S1(b)] and V_{th} is the threshold gate voltage ($V_{th} = -6.5$ V).

In order to clarify the change in the effective channel thickness (t_{eff}) of the TFT, we measured the thermopower (S) during the V_g application. Details of our electric field thermopower modulation method is described elsewhere.[17-20] The change in $-S$ as a function of the V_g is also plotted in Figure 3(a). The S values were always negative, reflecting that SnO_2 is an n-type semiconductor. The $|S|$ slightly decreases from 50 to 40 μV K^{-1} with V_g due to an increase in n_s. Using the relationship between $S - n_s$ and $S - n_{3D}$, t_{eff} was extracted as $t_{eff} \equiv n_s/n_{3D}$, where n_{3D} is three-dimensional carrier concentration obtained from $S - n_{3D}$ relationship as shown in our previous work.[15] Figure 3(b) shows the t_{eff} of the 3-nm-thick a-SnO_2 TFT during V_g application. When V_g is −5 V, the t_{eff} is ~0.8 nm and it gradually increases with V_g. This behavior is due to the high residual n_s. On the other hand, 1.8-nm-thick depletion layer is naturally formed somewhere in 3-nm-thick a-SnO_2 film. The depletion layer thickness is a little smaller than that of bottom-gated TFT (~2.5 nm).[15] The decreased depletion layer when the top gate structure is adopted, which may be ascribe to the influence on SnO_2 surface when deposit the gate insulator.

The 1.8-nm-thick depletion layer was formed by the Fermi energy difference between the a-SnO_2 film and the glass substrate and/or that between the gate insulator and the a-SnO_2. Therefore, if the a-SnO_2 is thinner than the depletion layer thickness, the TFT does not show transistor characteristics. To validate this scenario, we fabricated 1.5-nm-thick a-SnO_2 TFT (Figure S1) and confirmed that the TFT does not show transistor characteristics. From these results, we narrowed down that the optimal a-SnO_2 channel thickness is ~1.8 nm. Then, we fabricated a 2-nm-thick a-SnO_2 TFT with 160-nm-thick a-HfO_2 film as the gate insulator. The resultant TFT showed good transistor characteristics; on-to-off current ratio of ~10^4 [Figure S1 (a)] and μ_{FE} of 8 cm^2 V^{-1} s^{-1} [Figure S1(d)]. This result clearly indicates that the optimal channel thickness is ~2 nm for top-gated a-SnO_2 TFT.

Next, we reduced the a-HfO_2 film thickness to 80 nm in order to reduce the required V_g of the 2-nm-thick a-SnO_2 TFT. Figure 4(a) shows the cross-sectional high-angle annular dark field scanning transmission electron microscopy (HAADF-STEM) image of the resultant TFT. A multilayer structure composed of a-ITO, a-HfO_2, a-SnO_2, and glass substrate was clearly observed. The corresponding energy-dispersive X-ray spectroscopy (EDS) mappings are shown in the Figures 4(b)-(d), which confirms the thickness of the a-SnO_2 layer (~2 nm) and the HfO_2 layer (~80 nm).

Figure 4 summarizes the transistor characteristics of the resultant 2-nm-thick a-SnO_2 TFT with 80-nm-thick HfO_2 gate insulator. Since the thinner gate insulator could provide stronger coupling capability, it could accumulate more charges (per unit area) at the channel area by the same applied V_g compare to its thicker counterpart.[21-22] The resultant TFT exhibits a maximum I_{ON} and minimum I_{OFF}, the highest on-to-off current ratio of ~10^5 along with a reduced subthreshold swing (SS) of ~230 mV/decade [Figure 5(a)], which is estimated from SS = $[d(\log I_d)/dV_g]^{-1}$. It also shows an improved μ_{FE} of ~10 cm^2 V^{-1} s^{-1} [Figures S2(b)]. The TFT performances greatly improved compared to the thicker gate insulator a-SnO_2 TFT (a-HfO_2 ~160 nm), which is attributed to the superior electrostatic control by the thinner gate insulator. The C_i value of 80-nm-thick a-HfO_2 is ~240 nF cm^{-2} [Figures 5(b)] which almost 2 times higher than that 160-nm-thick one (C_i ~125 nF cm^{-2}) [Figures S1(b)]. The gate leakage current (I_g) of these a-SnO_2 TFTs is lower by several orders of magnitude than the I_d, which guarantees that the TFT characteristics are unaffected by the I_g.

Since SnO_2 exhibits strong gas sensing characteristics, the film surface is easily affected by the surrounding atmosphere. Therefore, a large discrepancy in V_{th} was observed in air

and vacuum[15], and the bottom-gate top-contact structure of the SnO_2 TFT showed strong ambient sensitivity. In order to check if the top-gate bottom-contact structure of the SnO_2 TFT still show ambient sensitivity, we measured the transfer characteristics of the 2-nm-thick a-SnO_2 TFT with thinner gate insulator (a-HfO_2 ~80 nm) in vacuum. As shown in Figure 4(a), the transfer characteristic curve of this TFT remains unchanged after keeping in vacuum for 48 h. As shown in Figure 5(c), V_{th} of ~+0.65 V, which was evaluated by plotting $I_d^{0.5}$–V_g relationship, experienced no shifts. Therefore, by changing the bottom-gate top-contact structure of the a-SnO_2 TFT to top-gate bottom-contact structure, one can effectively relieve the ambient sensitivity of SnO_2 TFT. This may be attributed to the protective layer role of the gate insulator layer and the top gate electrode.

In order to investigate the long-term reliability of the 2-nm-thick a-SnO_2 TFT with 80-nm-thick HfO_2 gate insulator we performed the bias stress tests under V_{BG} = –3 V (NGBS) and V_{BG} = +6 V (PGBS) as a function of stress time, which was shown in Figure S4. The threshold voltage shift (ΔV_{th}) was calculated by $\Delta V_{th} = V_{th,\,BG} - V_{th,\,IN}$, where $V_{th,\,BG}$ is the threshold voltage after bias stress applied and $V_{th,\,IN}$ is the initial threshold gate voltage. The negative V_{th} shift under V_{BG} = +6 V (PGBS) with increased stress time, indicating that a small number of H_2O molecules diffused through the gate electrode ITO and gate

insulator HfO_2 into the a-SnO_2 active layer. The slightly positive V_{th} shift under V_{BG} = –3 V (NGBS) after 1000 s then keeps constant was found and attributed to the electrons trapped in the gate insulator or at the gate insulator/ a-SnO_2 active layer interface. Compared with the a-SnO_2 TFT under NGBS, the device degradation under PGBS was more obvious, indicating that H_2O molecules under PGBS has a greater impact on a-SnO_2 TFT. Further, in order to check the homogeneity of the 2-nm-thick a-SnO_2 TFTs, we tested several devices (200 μm × 400 μm) on the same substrate. As a result, more than 70% of the devices were operated normally, and the difference between the devices was small within the measurement error.

These achievements imply that the top-gated a-SnO_2 TFT have the potential to overtake a-$InGaZnO_4$ TFT for transparent electronics application. However, due to the high processing temperature of the SnO_2 (~400 °C), it is difficult to fabricate this top-gated a-SnO_2 TFT on flexible substrate. In order to meet the contemporary demand for foldable, flexible, and wearable devices, further improvement is required such as decrease the processing temperature of the SnO_2. We believe that our work on 2-nm-thick top-gated a-SnO_2 TFT with thinner gate insulator (a-HfO_2 ~80 nm) can introduce further possibilities for the next generation of low-cost and low-power electronics.

In summary, we demonstrated that the two-dimensional channel thickness of amorphous SnO_2 for transparent thin-film transistor was successfully optimized using the electric field thermopower modulation analyses of the 3-nm-thick a-SnO_2 TFT. The optimized a-SnO_2 thickness was ~2 nm. After the optimization of the channel thickness, we reduced the thickness of HfO_2 gate insulator film to improve the transistor characteristics. The resultant TFT exhibited excellent transistor characteristics; on-to-off current ratio of ~10^5, normally off behavior (V_{th} ~+0.65 V), small subthreshold swing of ~230 mV/decade, high mobility (~10 $cm^2\ V^{-1}\ s^{-1}$), and stability in changing oxygen atmospheres. The present results would bring further possibilities for the development of next-generation low-cost and low-power electronic devices.

Methods.

Fabrication of the TFTs. The top-gate bottom-contact TFTs were fabricated on alkali-free glass substrates prepared by pulsed laser deposition method. First, the SnO_2 film was deposited on the alkali-free glass substrate through a stencil mask. Then, A 100-nm-thick ITO films were deposited (source and drain electrodes, 400 μm × 400 μm). After that, the resultant device was heated at 400 °C for 30 min in air. Subsequently, a 160/80 nm-thick amorphous HfO_2 gate dielectric film (permittivity, ε_r = 21−23[16]) was deposited at room

temperature (KrF, ~2 J cm^{-2} $pulse^{-1}$, oxygen pressure: 4.5 Pa). Finally, 100-nm-thick ITO films (gate electrodes) were deposited. These deposition conditions were shown in our previous report.[23] The channel length L was 200 μm and the channel width W was 400 μm. We checked the homogeneity of the SnO_2 films using X-ray reflection. We fabricated several devices on the SnO_2 film and tested the reproducibility.

Electric field thermopower modulation analyses of the TFTs. Thermopower (S) of the resultant TFT channel was measured during the V_g application. Details of the electric field modulated S measurement are described elsewhere.[17-20]

ASSOCIATED CONTENT

Supporting Information

Supporting Information is available free of charge via the Internet at https://pubs.acs.org/doi/10.1021/acsaelm.xxxxxxx.

Transfer curves (I_d−V_g); Capacitance per unit area (C_i−V_g); Sheet carrier concentration (n_s−V_g); Field effect mobility (μ_{FE}−V_g) of the 1.5 nm, 2 nm and 3 nm-thick a-SnO_2 TFTs with 160 nm-thick HfO_2 gate insulators. Sheet carrier concentration (n_s) and field effect

mobility (μ_{FE}) as function of V_g; Drain voltage dependence of the transfer characteristics I_d−V_g in air of the 2 nm-thick a-SnO_2 TFTs with 80 nm-thick HfO_2 gate insulators; Threshold voltage shift ($\Delta V_{th} = V_{th,\,BG} - V_{th,\,IN}$) of the 2-nm-thick top gated a-SnO_2 TFT with 80-nm-thick a-HfO_2 gate insulator under V_{BG} = −3 V (NGBS) and V_{BG} = +6 V (PGBS) as a function of stress time; Transfer curves (I_d−V_g) of several 2-nm-thick a-SnO_2 TFTs with 80-nm-thick a-HfO_2 gate insulator on the same substrate; Summarize of the structure, on-off current ratio, threshold gate voltage (V_{th}), subthreshold swing factor (*S.S.*), field effect mobility (μ_{FE}), fabrication method for SnO_2 TFTs.

Author Contributions

D.L. and B.C. performed the sample preparation and measurements. B.F. and Y.I. performed the STEM analyses. D.L. and H.O. planned and supervised the project. All authors discussed the results and commented on the manuscript.

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Notes

The authors declare no competing financial interest.

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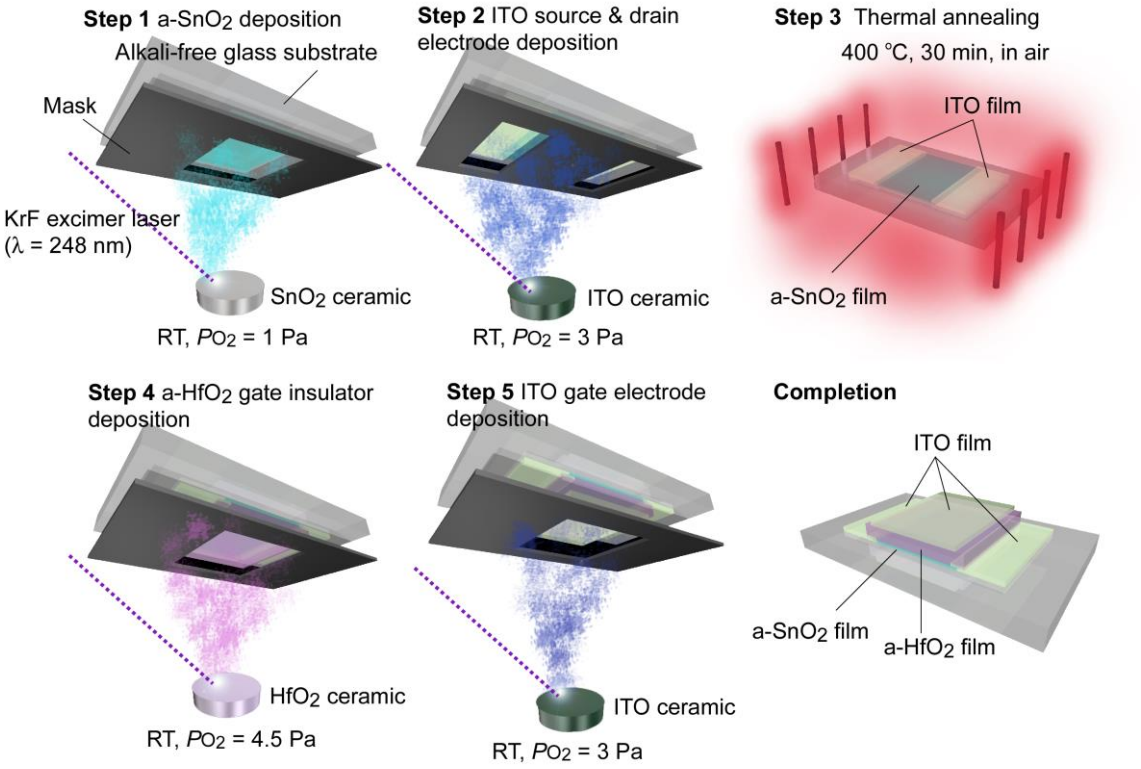


Figure 1. Fabrication scheme of the top-gated transparent thin-film transistor with a-SnO_2 active channel. The films of a-SnO_2, ITO for source and drain electrodes, a-HfO_2, and ITO for gate electrode were deposited by the pulsed laser deposition method using KrF excimer laser. After the deposition of ITO source and drain electrode, we annealed the sample at 400 °C for 30 min in air.

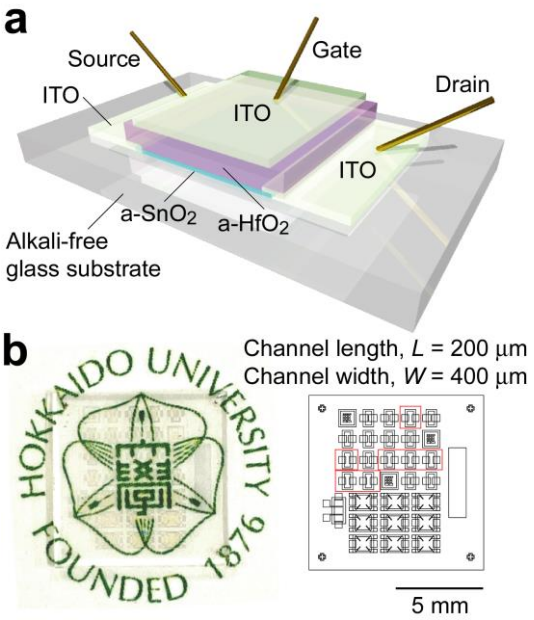


Figure 2. (a) Schematic illustration of the top-gated transparent thin-film transistor with a-SnO_2 active channel. Channel length and width are 200 and 400 µm, respectively. a-HfO_2 film is used as the gate insulator. (b) (Left) Photograph and (right) blueprint of the TFTs on a glass substrate. Green colored logomark located below the TFT is clearly visible. We measured the TFTs surrounded by the red frames. The logomark in (b) is reprinted with permission from Hokkaido University.

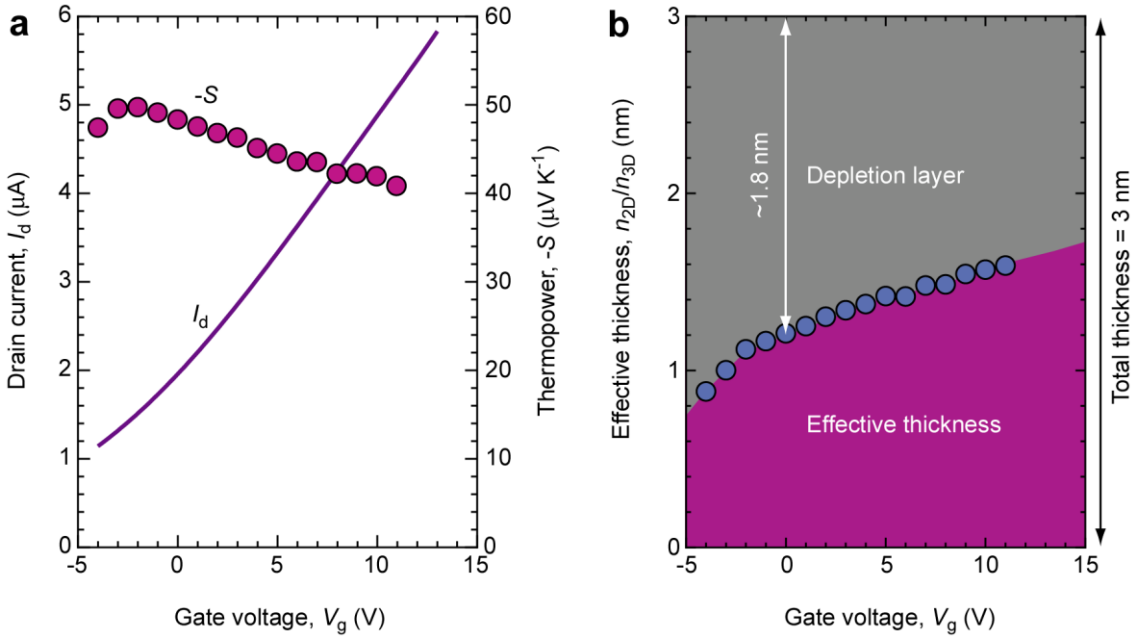


Figure 3. Electric field thermopower modulation analyses of the top-gate bottom-contact 3-nm-thick a-SnO_2 TFTs with 160-nm-thick a-HfO_2 gate insulator film. (a) Transfer characteristics (V_d = +0.1 V). Corresponding electric field modulated thermopower (S) at various V_g ranging from −5 to +11 V are also shown (purple circle). The $-S$ gradually decreases with V_g. (b) V_g dependence of the effective thickness (t_{eff}), which is defined as n_s/n_{3D}. When V_g is −5 V, the t_{eff} is ~0.8 nm and it gradually increases with V_g. This behavior is due to the high residual n_s. On the other hand, 1.8-nm-thick depletion layer is naturally formed somewhere in 3-nm-thick a-SnO_2 film.

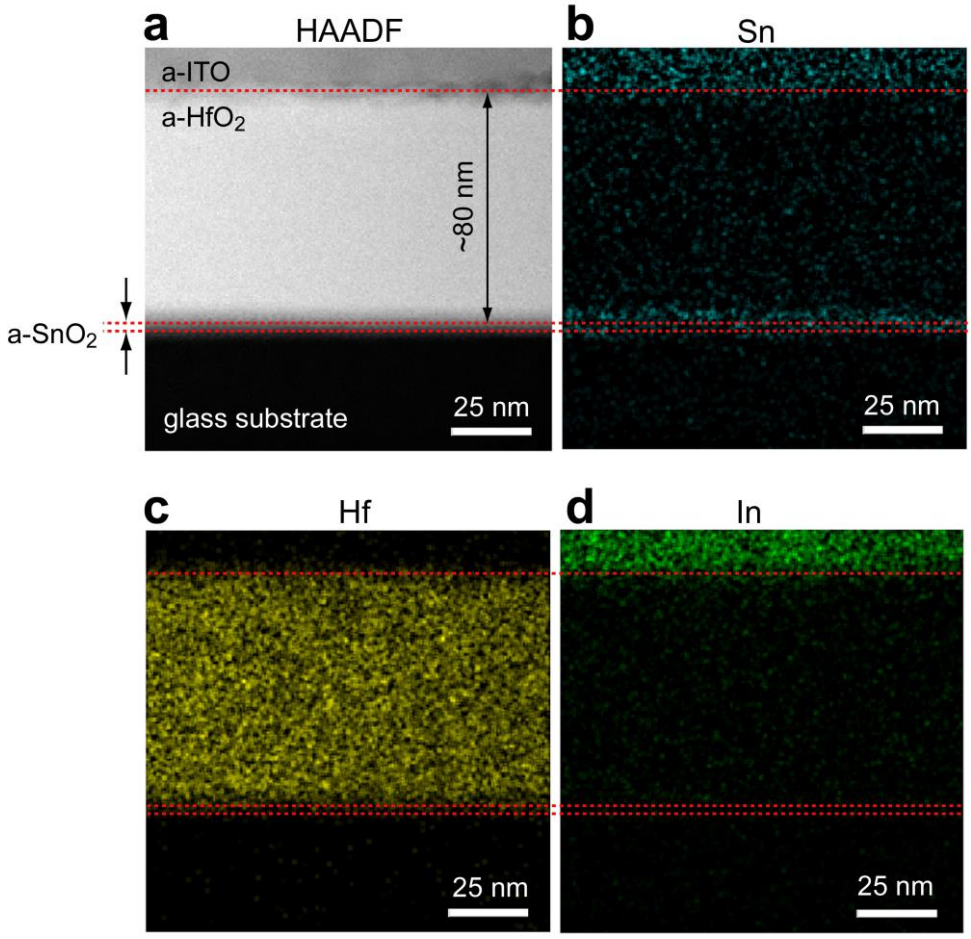


Figure 4. (a) The cross-sectional HAADF-STEM image and the EDS mappings of (b) Sn, (c) Hf, and (d) In for the resultant TFT. A 2-nm-thick a-SnO_2 active layer and an 80-nm-thick a-HfO_2 gate insulator is clearly visible.

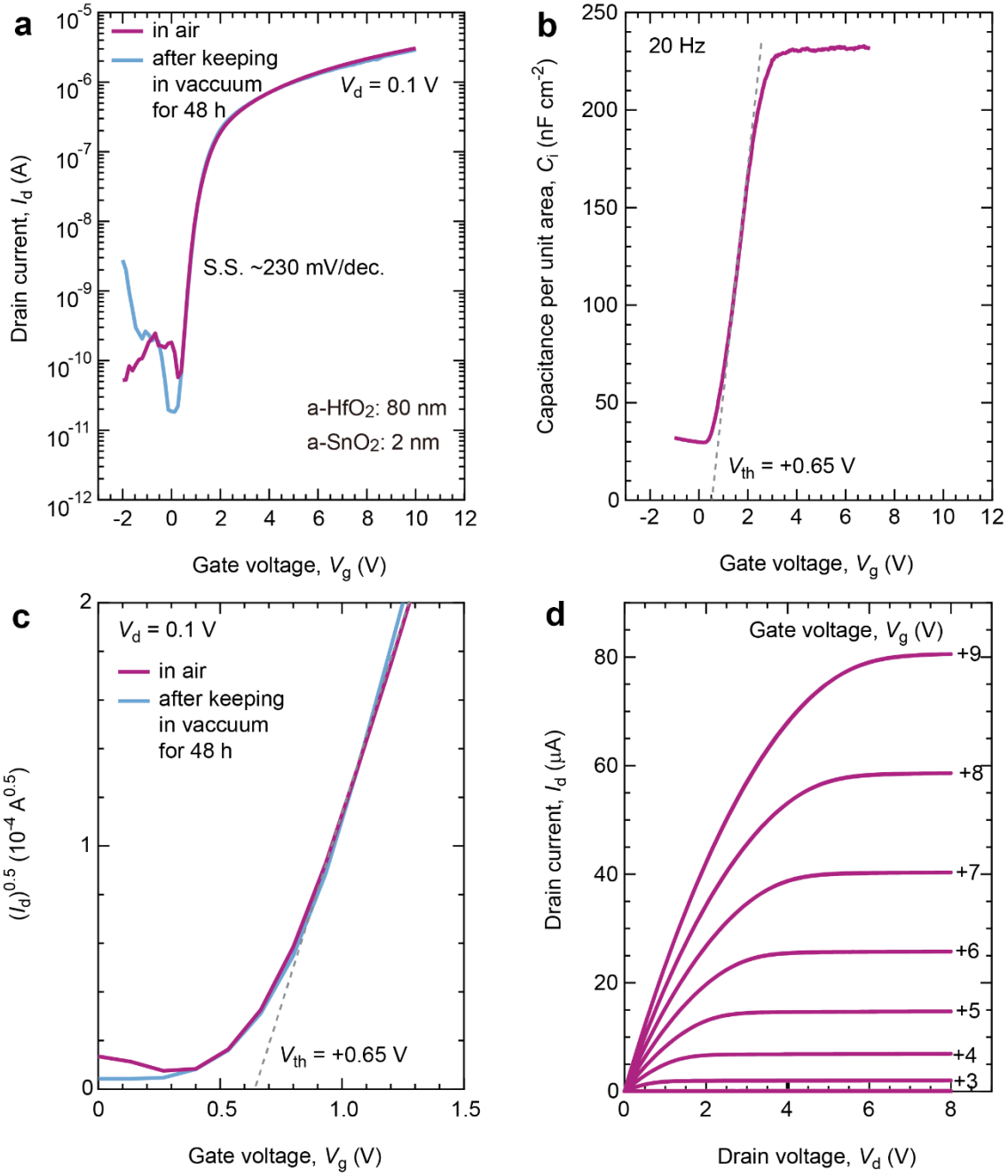
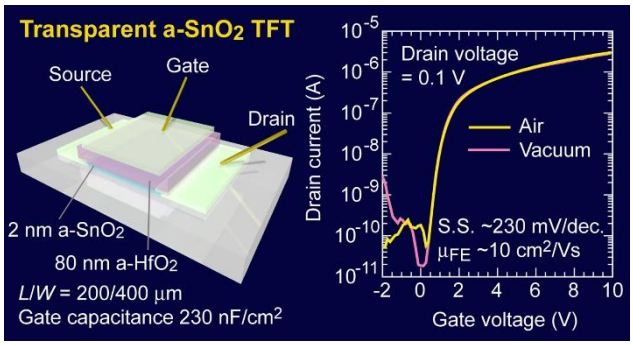


Figure 5. Typical transistor characteristics of the resultant 2-nm-thick a-SnO_2 TFT with 80-nm-thick a-HfO_2 gate insulator. (a) Transfer characteristics (V_d = +0.1 V) measured in air and in vacuum (after keeping in vacuum for 48 h). Note that the transfer characteristics remain unchanged. (b) Capacitance per unit area. (c) $I_d^{0.5}$–V_g plot. The V_{th} is +0.65 V and the V_{th} is insensitive to oxygen gas. (d) Output characteristics (V_g ranging from +2 to +9 V).


Transparent a-SnO2 TFT
Source
Gate
Drain
2 nm a-SnO2
80 nm a-HfO2
L/W = 200/400 μm
Gate capacitance 230 nF/cm2
Drain current (A)
10-5
10-6
10-7
10-8
10-9
10-10
10-11
Drain voltage
= 0.1 V
Air
Vacuum
S.S. ~230 mV/dec.
μFE ~10 cm2/Vs
-2
0
2
4
6
8
10
Gate voltage (V)