# Electrochemical Processes for Formation, Processing and Gate Control of III-V Semiconductor Nanostructures

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## Abstract

This paper reviews recent efforts by authors' group to utilize electrochemical processes for formation, processing and gate control of III-V semiconductor nanostructures. Topics include precise photo anodic and pulsed anodic etching of InP, formation of arrays of <001>-oriented straight nanopores in n-type (001) InP by anodization and their possible applications, and macroscopic and nanometer-scale metal contact formation on GaAs, InP and GaN by a pulsed in-situ electrochemical process, which remarkably reduces Fermi level pinning. All the results indicate that electrochemical processes can achieve unique and important results which the conventional semiconductor technology cannot realize, anticipating their increased importance in future semiconductor nanotechnology and nanoelectronics.

**Key words:**
III-V semiconductors, anodic etching, nanopore, electrodeposition, Schottky barrier

## 1.Introduction

It is widely recognized that artificial semiconductor nanostructures such as quantum wires (QWRs) and quantum dots(QDs) give rise to new rich functionalities to materials. They produce new quantum state spectra with novel state transitions and linear and non-linear quantum transport phenomena, and open up opportunities for novel quantum devices which control quantum-mechanical behavior of electrons and photons in various sophisticated ways.

The standard approach for semiconductor nanostructure formation is to use fine crystal growth techniques such as molecular beam epitaxy (MBE) and metalorganic vapor phase epitaxy (MOVPE). To fabricate devices, various standard etching and metal deposition techniques are used together with standard lithography techniques. However, the electrochemical approaches, if it attains sufficiently high controllability at the nanometer-scale, seems to be highly useful for nanostructure formation and processing. The expected advantages include: (1) process simplicity and versatility, (2) capability of self-organization, (3) low processing temperature, (4) low process induced damage, (5) precise electrical control and (6) low processing costs.

Some well known examples are porous Si formation [1,2] and use of anodized alumina as nanostructure templates for formation of carbon nanotubes [3].

The purpose of this paper is to review recent attempts by the authors' group at RCIQE, Hokkaido University, that have been carried out in order to investigate feasibility of utilizing electrochemical processes for nanometer-scale processing and nanostructure formation in III-V semiconductors. Topics discussed in this paper include controlled (1) anodic etching of InP,

(2) nanopore formation in InP by anodization and its possible application, and (3) macroscopic and nanometer-scale contact formation on GaAs, InP and GaN by pulsed in-situ electrodeposition.

## 2. Controlled anodic etching of InP by anodization

### *2.1 Wet etching and Behavior of n-InP anodes*

Reduction of device feature sizes into nanometer scale is a universal trend in all semiconductor devices including Si and III-V devices, being irrespective of whether they are traditional semi-classical devices or emerging quantum devices. Particularly, since InP-based materials provide fastest transistors of all semiconductors [4] as well as various photonic devices for long wavelength optical communication [5], any low-damage processing technique with nanometer scale controllability is of great interest for future progress.

In the Si technology, dry processing has been preferred as compare with wet chemical processing. However, wet processing such as the Damascene process [6] for Cu on-chip metallization has been accepted as a powerful Si VLSI processing technique, and such a trend may increase in future. On the other hand, in the III-V semiconductor technology, wet chemical etching in various acid solutions [7] is widely used in various processing steps of device fabrication owing to its low damage nature as compared with the dry etching. Quantum nanostructure fabrication by selective MBE or MOVPE growth on pre-patterned substrates [8,9] also requires highly controllable wet chemical etching for pattern fabrication.

The difficulty of wet chemical etching is, however, that precise control of the etching depth is extremely difficult in the nanometer length scale, because the etch rate is very sensitive to temperature variation as well as to local fluctuation of the etchant composition caused by accumulation of etching by-products.

On the other hand, electrochemical etching appears to be promising for achieving high controllability. This is because anodic reactions on semiconductors, which are known to involve holes rather than electrons, should be precisely controllable by the amount of charge supplied for reaction. Namely, the etch depth, t, can be related to the sheet charge density, Q, that has passed through the electrode surface, by the following equation based on Faraday's law of electrolysis.

$$t = \frac{M}{xFd}Q \qquad (1)$$

where F is Faraday's constant (96,485.3 C/mol), M and d are the molecular weight and the density of the semiconductor, respectively, and x is the number of holes required to etch one molecule of the semiconductor.

To actually perform electrochemical etching, understanding of the behavior of the semiconductor anode is essentially important. Although anodic reactions on GaAs [10] were studied in detail previously, not much attention has been paid on those on InP except for few reports [11-13]. From such a viewpoint, we have been studying anodic reactions on the (001)-oriented n-InP electrodes [14]. The set-up for the experiment had a simple standard cell configuration with three electrodes, i.e., an InP electrode, a Pt counter electrode and a reference saturated calomel electrode (S.C.E.). For current supply, GeAu/Ni ohmic electrodes sintered at 370˚C in $N_2$ flow were provided at the back or the front surface of the InP electrode, depending whether the electrode is a conducting n-type InP substrate or a Fe-doped semi-insulating one. The potential on the InP electrode was controlled with respect to the S.C.E. by a potentiostat in d.c., ramped or pulsed mode. Since holes required for anodic reactions are minority carriers in the n-type semiconductor, a sufficient number of them were supplied either by applying a high voltage to the substrate to cause avalanche breakdown or by illuminating the electrode with light to cause photo-generation.

Examples of measured typical cyclic voltammograms obtained in the dark on n-InP in an electrolyte of a dilute HCl solution with a pH of 1.0 are shown in **Fig.1**. In the dark, no anodic current flows at small overpotentials because of the presence of an electrolytic Schottky barrier at the n-InP/electrolyte interface. Above +1.0 V (vs S.C.E.), the anodic current started to flow. On the other hand, when illuminated by a tungsten lamp at an intensity of 20 $mW/cm^2$ from a distance of 5 cm, the photo-anodic current started to flow at -0.40 V (vs S.C.E.), indicating the onset of an anodic reaction even at a negative overpotential due to the photovoltaic effect. After the onset of anodic current, the cyclic voltammograms behaved in a fashion similar to **Fig.1**. Namely, they showed a peak and hysteresis, indicating the occurrence of the so-called active-passive transition [15]. At small overpotentials, active anodic dissolution took place, and at larger overpotentials beyond the peaks, the semiconductor surface was covered with a passive oxide film, leading to passivation with nanopore formation as discussed later. Scanning electron microscopy (SEM), electrochemical scanning tunneling microscopy (STM), atomic force microscopy (AFM) and x-ray photoelectron spectroscopy (XPS) studies have confirmed existence of two regimes of anodic reaction.

***2.2 Uniformity and controllability of anodic etching of InP***

Controlled etching in the active dissolution regime can be done either in the d.c. photo-anodic mode and in the pulsed avalanche mode as schematically shown in **Fig.2(a)**. As compared with the cyclic voltammogram taken on the initial air exposed surface, those taken after anodic etching in either mode showed increase of anodic current for the same overpotential due to removal of a current blocking oxide. On the other hand, it has been found in the pulsed mode that characteristics between the pulse peak voltage and the pulse current became very different from those in the voltammogram taken under a slowly ramped voltage sweep. Namely, the pulsed current is much larger than the slowly ramped current at the same overpotential, and does not show a peak. This can be explained by the fact that a finite time is required to cause active-passive transition as discussed in the case of anodic oxidation of GaAs [15]. Thus, no current-blocking oxide layer is formed in a short pulse of ms duration even at a very large pulse peak voltage and etching takes place during the pulse-on time, $t_{on}$. Then, the resultant high-density anodic reaction products are removed from the surface vicinity by diffusion during the pulse-off time, $t_{off}$. From such a viewpoint, the on-off ratio, $t_{on}/t_{off}$, should be carefully chosen for sufficient removal of the products. In the case of $t_{on}$ of ms duration, it has been empirically found that the on-off ratio should be smaller than 1/120.

An in-situ STM study of the surface just after anodic etching as well as an ex-situ AFM observation have both indicated that surfaces obtained after photo-anodic etching and pulsed avalanche etching are smooth and featureless with an minimum rms roughness value of 1.8 nm. This value is significantly smaller than that obtained after conventional sulfuric acid-based wet etching. For example, etching with a standard solution of $H_2SO_4 : H_2O_2 : H_2O = 3 : 1 : 1$ typically gives a minimum rms roughness value of 5 nm, sometimes resulting in a much rougher surface with height variations of 10-20 nm. XPS studies have indicated that anodically etched surfaces are free of native oxides.

As for the controllability of the etch depth, a detailed study has been carried out as a function of the integrated sheet charge density Q as shown in **Fig.2(b)** for both etching modes. Q was determined by integrating the anodic photocurrent or pulse current density. It is seen that the etching depth increases in proportion to the integrated sheet charge density. Thus, this result indicates that the etching depth can be controlled by monitoring and controlling the integrated sheet charge density, Q, supplied to the n-InP surface. Using a tungsten lamp, a typical etch rate of 30-40 nm/min can be realized. On the other hand, the etch depth should be controlled by the number of pulse in the pulse etching mode. An extremely small etch rate

of $3x10^{-5}$ nm/pulse has been obtained for $t_{on}/t_{off}$ =1/240 and $V_s$=5.0 V, indicating feasibility of an extremely fine control of etch depth in the pulse mode.

Finally, as for the basic anodic reaction for etching, one can determine the value of x in eq.(1), from the result shown in **Fig.2(b)**. Using M= 145.77 and d= 4.79 for InP, x has been found to be 8.0 for both etching modes. Thus, eight holes are required to etch one molecule of InP. This is different from the case of GaAs where six holes are consumed to etch one GaAs molecule [10]. In the latter case, the reaction involved is

$$GaAs + 6\ OH^- + 6h^+ = \frac{1}{2}Ga_2O_3 + \frac{1}{2}As_2O_3 + 3\ H_2O. \qquad (2)$$

However, no reliable value of x or a well-established reaction is reported for InP etching. Mention of x=6 was made in the anodic dissolution experiment work by Faur et al [13] as well as Notten et al [10], but no supporting data were given. This value of x=6 is difficult to explain because the existence of $P_2O_3$ has never been reported. On the other hand, the value of x=8 observed here can be explained either by

$$InP + 8\ OH^- + 8h^+ = InPO_4 + 4H_2O, \qquad (3)$$

or by

$$InP + 8\ OH^- + 8h^+ = \frac{1}{3}In_2O_3 + \frac{1}{3}In(PO_3)_3 + 4H_2O. \qquad (4)$$

All of $InPO_4$, $In_2O_3$ and $In(PO_3)_3$ have been mentioned previously as oxides obtained by oxidation of InP [16]. However, on the basis of detailed XPS analyses by our group and by others [17] ,we believe that the reaction in eq.(4) is most likely. The reaction seems to be very different from the case of the cathodic decomposition of InP in HCl where generation of $PH_3$ was observed [18].

## 3 InP nanopore formation by anodization and its applications

### *3.1)Formation of nanopores*

A very well known example of semiconductor nanostructure formation by an electrochemical process is formation of porous Si by anodization of n-type Si surface under light illumination [1-2]. Anodized porous Si exhibits a complicated tree-like structure with a lot of side branches, although it has a general tendency to align along the <001>-direction, when the anodization is applied on the (001) surface. Porous Si by anodization of p-type Si substrate usually exhibit highly random fractal-like characters [19]. It is also known that <001>-oriented straight pores without branches can be realized on n-type Si by a magnetic field-assisted anodization [20].

In III-V materials, anodization of (001)-oriented n-type GaAs and InP [21-25] has been reported to produce structures with lots of <111>-oriented branching [21-23, 25] similarly to the case of porous Si or structures with submicron grains [24]. On the other hand, formation of <111>-oriented straight pores without branches were reported by Takizawa et al. for (111) oriented n-InP [25-27].

We have recently shown that <001>-oriented nanometer sized straight pores, penetrating deep into the semiconductor, can be produced by anodizing (001)-oriented n-type InP in the passive region in a suitable electrolyte [28-30]. Such capability of forming <001>-oriented pores seems to be useful for various applications, since (001)-oriented substrates are technologically more important than the (111)-oriented one.

For the purpose of comparison, pore formation has been investigated in the following three kinds of electrolytes.

A: 1M HCl (200ml)

B: 1M HCl (200 ml) + $H_2PtCl_6$ (1 g) + $NH_4OH$ [pH=1]

C: 1M HCl(200ml) + $HNO_3$ (3ml)

Electrolyte B is the same as that used for electrodeposition of Pt discussed later, and this was investigated to see the feasibility of pore formation followed by in-situ deposition of Pt on the pore walls. Anodization was done with and without light illumination (tungsten lamp, 10 mW/cm$^2$), however, illumination caused no distinct difference in the structure of resultant nanopores.

In contrast to the featureless oxide-free surface obtained in the active region, the surface obtained by anodization in the passive region of the overpotential using above electrolytes showed various distinct features. The surface is covered by a thin oxide layer, as expected. However, a detailed SEM study has revealed that pores are produced by anodic etching in all of the above three electrolytes. This is distinctly different from the case of viscous eletctrolyte such as aqueous solution of tartaric acid mixed with glycol (AGW electrolyte [15,31]) where uniform anodic oxide films grow in proportion to the overpotential.

Overall structures of the nanopores formed in the above three electrolytes are basically similar. They have <001>-oriented long nano-pores with effective diameters of a few tens to handreds of nanometer, penetrating deep into the semiconductor bulk. The length of pore, or, the depth of the pore bottom, depends on the anodization time and remarkably uniform in the lateral direction. Depending on the electrolyte and anodization conditions, presence of an irregular top layer with a thickness of the order of 1 μm or less is seen on the top of the pore array. This irregular top layer seems to be a transition layer which is formed prior to formation of a more uniform array of pores deeper into the semiconductor bulk. Within the irregular top layer, merging of small pores and thinning of pore walls takes place, leading to formation of larger and more uniform pores below. An example of overall structure of nanopores formed in 1M HCl solution (Electrolyte A) under an overpotential $V_s$ = 5 V and at an anodization time $t_a$ = 1 min is shown in **Fig. 3(a)-(d)**. For structural characterization, plan-view and cross sectional SEM observations were carried out using a field-emission-type SEM system (Hitachi S4100) with a spatial resolution of 1.5 nm. Cross-sectional observation was made by cleaving the samples in (110) planes. In the case of **Fig. 3**, the pore diameter on the surface of the irregular layer was about 50 nm, whereas that below the irregular layer was about 160 nm. The behavior of anodic current is also similar. Namely, the current shows a rapid exponential decrease initially, and then shows a more or less constant value.

In spite of the overall similarity, specific details of the nanopore structures and their dependences on the anodization conditions are considerably different. The largest difference is the straightness of the pore. The electrolyte A always led to wavy pores as shown in **Fig.3(d)** whereas the electrolytes B and C gave very straight pores as shown in **Fig.4(a)** and **(b)**. At low overpotentials, the electrolyte A produced <113>-oriented branches as shown in **Fig.4(c)**, whereas no such tendency was seen in electrolytes B and C. The shape of the pore also depended on the electrolyte. The electrolyte A gave pores with circular cross-sections as shown in **Fig.3(b)**, whereas the electrolyte B and C gave square shaped pores defined by (100) planes, as shown in **Fig.4(d)** for electrolyte B. It is reported in reference (29) that the pores obtained by the electrolyte C were square ones defined by (110) planes rather than (100) planes, but this result could not be reproduced and this seems to be a mistake caused by sample mishandling.

The measured values of pore depth, average diameter, average pore period obtained by SEM observations are summarized in **Fig.5(a)-(d)**. It can be seen that pore depth, $D_p$, is a function of the anodization time. The depth of the porous layer shows a rapid increase up to $D_{p0}$ within first several seconds of anodization, $t_{a0}$, and then further increases almost linearly with the anodization time, $t_a$.

$$D_p = A (t_a - t_{a0}) + D_{p0} \qquad (5)$$

The data in **Fig.5 (a)** seem to suggest that the value of the slope factor A is nearly the same for the three electrolytes. It was also found that the depth is almost independent of the

overpotential $V_s$, and could be quite deep. In our study, a maximum depth of about 80 μm was achieved by anodization for 3 min. This value is much larger than the value reported for porous layers made on (111)A n-InP surfaces which had a maximum depth of 30 μm [25-27].

On the other hand, the lateral dimensions of the pore depend not on time, but on the value of the overpotential, $V_s$. To give an example, the average pore sizes, average pore wall thickness and minimum pore wall thickness were 170x170 $nm^2$, 20 nm and 14 nm, respectively, for square pore arrays obtained by using electrolyte B at an overpotential of $V_s$ =7 V. Thus, <001>-oriented straight nanopore arrays with fairly good structural uniformity can be realized in a self-organized fashion by single-step electrochemical anodization using electrolytes B and C. Parameters such as pore depth, diameter and period are strongly dependent on anodization conditions, and can thus be controlled electrically.

***3.2 Mechanism of nanopore formation***

Let us briefly discuss the formation mechanism of nanopores. As for porous Si, there exist two different models, namely "the Beale model" [32] and "the diffusion-limited model" [33] according to a review by Smith and Collins [19]. The former stresses the effect of electric field like that in the "tree" formation in electrostatic breakdown of solid-state insulators. The latter, on the other hand, emphasizes that the rate limiting process for pore formation is diffusion of holes that are responsible for anodic dissolution. Formation of straight pores without branching in the present InP nanopore formation seem to be more consistent with the latter model, although a fundamental similarity exists between these two models as mentioned by Smith and Collins [19].

From the viewpoint of the "diffusion limited model", pores are formed randomly at the initial stage of anodization on the surface due to random-walk of holes. Thus, fractal-like porous structures are formed by anodization of p-type Si, since holes can go inside the pore walls freely as majority carriers. Namely, their random-walk along the pore-electrolyte interface followed by a subsequent reaction leads to random structures. In the case of n-type Si, holes are minority carriers and a strong electric field with depletion of electrons exists near the semiconductor-electrolyte interface. Holes that are generated by photo-excitation or avalanche process feel this field and come to the interface to take part in anodic dissolution. Once a small pore is formed, the field is locally concentrated there, and this induces the selective dissolution at the pore tip, leading to the further growth of pores. As the pore formation proceeds, the pore walls become thinner and carriers are completely depleted at a certain point, making the further thinning of the pore walls impossible. Thus, there is a strong tendency that pores are separated periodically by the wall with the same thickness. An attempt [34] was made recently to include quantum confinement effect into a sophisticated computer simulation of formation of nano-meter sized Si porous structures. Here, increase of the effective bandgap due to the quantum confinement effect decreases excitation of holes in the nanometer thick pore walls and results in depletion of holes. As for the direction of pores, there will be a natural tendency that it follows the direction of strongest field with the highest supply of holes, i.e., in the <001>-direction on the (001) substrate. However, it will be modified, if there is a crystallographically preferred direction for anodic dissolution. In the case of (001) n-type Si, it is the <111>- direction and this explains the observed branching.

We believe that the above picture of pore formation also applies to the present case of InP. The reason why we obtain <001>-aligned straight pores in electrolytes B and C is most probably because the <001>- direction happens to the preferred one so that those electrolytes have a tendency to reveal (100) planes on anodic dissolution. On the other hand, the situation seems to be slightly different for the electrolyte A. The pores are wavy over the micrometer scale, as well as in a nanometer scale, exhibiting periodic lateral width variations with a vertical period of about 200 nm or so, as can be seen in **Fig.3(d)**. In addition, tilted pores directed in the <113>-orientation are formed at low overpotentials in the electrolyte A, as

shown in **Fig. 4(c)**. This indicates that the preferred direction of dissolution is not the <001>-direction in the electrolyte A as also reported by Takizawa et al. [25]. It is likely that the truly preferred direction is the <111>-direction, and that the observed <113>-direction may be a compromise between the field effect and the preferred dissolution. At low overpotentials, the field is still low, and holes can diffuse relatively freely with their thermal energy and attack the weak bonds on the pore/electrolyte boundary. At high overpotentials, strong <001>-oriented electric field restrict the hole motion along the <001>-direction and holes can reach only the pore tip. The wavy nature of the pore walls observed in the samples formed in the electrolyte A at high overpotentials in the present study can also be explained in terms of the present picture of competition between the pore formation along the preferential direction through random-walk of holes and the field-controlled pore formation by a <001>-oriented hole flow.

***3.3 Optical properties of nanopore arrays and possible applicaitons***

In order to investigate the optical properties of the nanopores produced by the electrolytes A,B and C, photoluminescence (PL) measurements have been performed over a temperature range from 20 K to 300 K, using the 488 nm line of an Ar+ laser as the excitation source. The PL signals were detected by an optical multi-channel analyzing system (Acton Research Cooperation) with a 0.75 m grating spectrometer and a CCD camera cooled by liquid $N_2$.

The nanopores produced by three kinds of electrolytes showed similar PL responses. As an example, the measured PL spectra from the nanopore arrays formed using electrolyte C with $V_s$ = 7 V and $t_a$ = 30 s, are plotted for various measurement temperature in **Fig.6(a)**. For the purpose of comparison, the PL peak position from a reference n-InP bulk sample is shown by the dashed curve. It is seen from **Fig.6(a)** that a blue shifted peak dominates at room temperature whereas a red-shifted peak dominates at 22K.

The observed PL behavior of the nanopore array can be explained in terms of the competition between two radiative transition processes each of which is dominant at high and low temperatures, respectively. In fact, fairly good fitting was obtained by using two components (labeled PW and S) indicated by broken curves in **Fig.6(a)** where the asymmetric peak shapes with low- and high-energy tails observed at 22 K and 300 K, respectively, are used for deconvolution. The model to explain the observed PL spectra is shown in **Fig.6(b)**. We assume presence of electron and hole quantum confined states inside the thin pore wall (PW) as well as presence of a broad surface state continuum (S) with a peak at 30 meV below the conduction band edge. The latter is a tentative assumption, and it could actually be located near the the valence band edge. The experimental fact that the intensity of the red-shifted emission peak did not change with the change of wall thickness (namely, crystal volume) at low temperatures strongly indicates that this peak is related to surface states, and not to some bulk defect level. At low temperatures, electrons are captured by the broad surface state continuum and, then, recombine radiatively with photo-generated holes, giving red-shifted surface state emissions (S). Around 90 K, the electrons begin to escape from the surface state continuum to the quantum state due to availability of thermal energy, reducing the intensity of the red-shifted component, S and making the blue-shifted component, PW, visible. At room temperature, almost all the photo-generated carriers can occupy the quantum confined state in the pore wall and the blue-shifted component, PW, becomes dominant, as seen in **Fig. 6(a)**.

Finally, let us briefly discuss about possible applications of the <001>-oriented straight nanopore arrays. They possess fairly good structural uniformity and can be realized in a self-organized fashion on the technologically important (001) surface of III-V semiconductor by a single-step electrochemical anodization. The conventional “top-down” semiconductor VLSI technology can never produce such arrays of deep pores with nanometer feature sizes into high quality semiconductors. Potential applications include (1) high speed and highly

sensitive photodetectors, (2) large capacitors for memory nodes and for energy storage for RFID (radio frequency identification) chips, (3) templates for growth of III-V quantum wires and dots, (4) formation of photonic crystals and other optical applications and (5) various sensor applications. However, whether such applications can be actually realized depends on fine structural tunability and additional processing capabilities of the nanostructures. For example, applications (1) and (2) require covering of pore inner surfaces with metal. However, our initial attempt to form Pt film on the pore surface by the pulsed electrodeposition process described in the next section using the electrolyte B, did not produce encouraging results so far, and it requires further work.

As another initial attempt [30], we have recently tried utilize anodized InP pores as templates for MBE growth of InP-based quantum wires (QWRs) and quantum dots(QDs). In particular, shollow pore depths are required to grow QD arrays. For this purpose, a pulsed pore formation process has been successfully developed by which pore depth can be well controlled in the nanometer range by adjusting the number of the applied pulses. MBE growth of InGaAs was attempted onto the templates having shallow nanopores in order to form QD arrays. Cross-sectional SEM image showed that growth of InGaAs into pores took place into a substantial depth of about 20-60 nm. On the measured PL spectra, red-shifted surface state peak present before MBE growth disappeared, and a new peak appeared at about 1.2 eV in addition to the PL emission from the InP substrate and that from the InGaAs top layer. The new peak, which is much stronger than the InP peak, has been assigned to the peak arising from InGaAs QD arrays embedded in InP pores.

Additionally, judging from the promising results obtained on anodized alumina [35], application of present pores to two dimensional photonic crystals seems to be a promising one, although we have not investigated so far. As compared with selective MBE and MOVPE approach for growth photonic crystals, anodization can realize much larger aspect ratios for pores with a very much reduced processing cost. The feature size range and filling factors available with the present nanopore arrays seem to be suitable, judging from a calculation on the dispersion relation of two-dimensional semiconductor photonic crystals [36].

In this connection, recently reported new structures such as patterned arrays of anodized porous InP [37] and anodized porous InP superlattices [38], both using the electrolyte B, seem to add new structural possibilities and may lead to new optical applications as well as to gas and bio sensing applications.

## 4. Metal contact formation by a pulsed in-situ electrochemical process

### *4.1. Fermi level pinning at metal-semiconductor interfaces*

Schottky barriers formed at a metal-semiconductor (MS) interface play important roles in many of III-V semiconductor electronic and optoelectronic devices. Especially, III-V quantum devices require nanometer-sized Schottky contacts for gate control. Here, tight gate control becomes extremely important, because it should control of quantum transport of a single or few electrons within a nanometer-sized space. Therefore, control of Schottky barrier heights (SBHs) and reduction of leakage currents become even more important issues in the nanoscale devices as compared with the traditional devices.

However, the formation mechanism of the Schottky barrier has been a long standing issue which has not been completely resolved. In the ideal limit, called Mott-Schottky limit, one assumes a simplest mutual alignment of the energy bands which keeps their energy distance with respect to the vacuum level unchanged at the MS interface. The SBH values, denoted as $\phi_{Bn}$ and $\phi_{Bp}$ for n-type and p-type materials, are then given respectively by

$$\phi_{Bn} = \phi_m - \chi_s \qquad \text{and} \qquad \phi_{Bp} = E_g - (\phi_m - \chi_s) \qquad (6a)$$

where $\phi_m$ is the metal work function, and $\chi_s$ and $E_g$ are the electron affinity and band gap energy of semiconductor, respectively. If this model is valid, the metal Fermi level position

can be placed at various positions of semiconductor bands, covering over more than 4eV by changing the metal species. This means that Schottky barriers with various SBHs, ohmic contacts for n-type and p-type materials, and high energy electron and hole injectors can be realized by selecting a suitable metal.

However, at realistic MS interfaces, the metal Fermi level is strongly pinned in the neighborhood of a certain characteristic energy, $E_0$, for a given semiconductor [39]. This phenomenon is called "Fermi level pinning" at the MS interface, where the SBH value becomes, either independent of, or only very weakly dependent on, the metal work function. Usually, the dependence of SBH on the metal work function is represented by the slope factor $S \equiv d\phi_{Bn}/d\phi_m$. In the strongly pinned limit, called Bardeen limit, the SBH value for n-type materials, $\phi_{Bn}$, and that for p-type materials, $\phi_{Bp}$, are given by

$$\phi_{Bn} = E_c - E_0 \qquad \text{and} \qquad \phi_{Bp} = E_0 - E_v \tag{6b}$$

Here, the SBH value is independent of the metal species, and S=0. For III-V materials, values of S are usually small and all the previous attempts to control the SBH values by changing metals so far have failed due to the strong Fermi level pinning.

It is well known that the above Mott-Schottky type band alignment takes place at the electrolyte-semiconductor Schottky interface. Why the strong electronegativity of metals is almost totally screened at solid-state MS interface is not well understood up to now. Most of the previous models for Fermi level pinning assume presence of interface states whose charging screens the metal electronegativity. The origin of the interface states is ascribed to stoichiometry related defect states (Unified Defect model [40]), to metal induced gap states (MIGS model [41,42]) or to disorder induced gap states (DIGS model [43]).

As shown in the next section, we have recently found that a pulsed in-situ electrodeposition process can form macroscopic and namometer scale MS interfaces with reduced Fermi level pinning where the SBH values become strongly dependent on the metal work function.

### *4.2. Formation of macroscopic MS interfaces by pulsed in-situ electrodeposition*

The pulsed in-situ electrochemical process [44-47] consists of controlled anodic etching of semiconductors followed by subsequent cathodic deposition of metal in the same electrolyte including metal ions, using the waveforms show in **Fig.7(a)**. Electrochemical deposition of Bi on GaAs was reported by Vereecken et al [48]. Epitaxial growth of Ni on GaAs has also recently reported [49].

With reference to **Fig.7(a)**, typical values of $V_{he}$, $t_{we}$ and $t_{pe}$ used in our study are 15 V, 10μs and 400μs, respectively. After the etching of the surface, metal deposition is initiated by changing the polarity of the potential, and using various values of $V_{rd}$, $V_{hd}$, $t_{wd}$, and $t_{pd}$. Pt, Ni, Co, Ag and Sn have been deposited onto n-type (001) GaAs, n-type (001) InP and n-type (0001) GaN surfaces using this process. Detailed XPS in-depth profile analyses have shown that this pulsed in-situ electrochemical process forms an intimate contact without inclusion of appreciable amounts of interfacial oxide layer. However, this may depend on the details of anodic processing and characterization procedure, and a contrary result has been reported recently for Pt/GaAs [50].

Formation process of macroscopic MS interfaces has been investigated in detail by SEM and AFM. At the initial stage of the electrochemical deposition, nanometer-sized metal particles are formed in a self assembled fashion on the surface of semiconductor substrate, as shown in **Fig. 7 (b)** for Pt on n-GaAs. Further deposition does not increase the size of the individual particles, but increases the number of the particles, as shown in **Fig. 7(c)**. Eventually, remarkably smooth Pt films could be obtained after uniform coverage by the size-saturated Pt particles. Raman experiments revealed that such Pt/InP interfaces are remarkably free from stress [46]. As for the Co, Ni. Ag and Sn deposition, nano particles are similarly formed on the surface at the initial stages, but the size and their uniformity are strongly

dependent on the metal species. Pt deposition has produced smallest nano partilces with smallest size deviation.

The size and size uniformity of nano-particles also depend strongly on the electrochemical conditions. As an example, size distributions of the nano-particles measured on Pt/InP macroscopic samples are shown in **Fig.8** for different sets of parameters, $V_{rd}$, $t_{wd}$, and $t_{pd}$ defined in **Fig. 7(a)**. Compared with the usual dc mode, the pulsed mode produced smaller and more uniform Pt particles on the semiconductor surface. In the pulsed mode, the size distributions is strongly influenced by the pulse conditions. Both the average particle diameter, d, and the its standard deviation, $\sigma_d$, decrease with smaller $t_{wd}$ and longer $t_{pd}$.

Furthermore, we have found that the electrical properties of macroscopic Schottky contacts have a remarkably strong correlation with the size and size distribution of metal particles. To show this, the SBH values of the macroscopic InP Schottky contacts formed by the electrochemical process are shown in **Fig.9 (a)** and **(b).** The SBH value changes with the metal work functions from 0.35 eV to 0.86 eV, indicating remarkable reduction of Fermi level pinning at the MS interface. Furthermore, the SBH value for Pt shows a surprisingly large change of 340 meV, depending on the size of the Pt particles, as seen in **Fig. 9(b)**. As the particle size decreases, the SBH rapidly increases toward the value of the Mott-Schottky limit, and there is no indication that the Fermi level is "pinned". Our interpretation for this observation is the following. We believe that strong Fermi level pinning usually encountered at MS interfaces prepared by conventional technologies is due to the disorder induced gap states (DIGS) [43]. They are consequence of bond disorder caused by deposition of high energy metal atoms in the conventional vacuum deposition, electron beam deposition and sputtering processes. On the other hand, the electrochemical deposition process is an extremely low-energy room temperature process where metal ions are attached to semiconductor by gentle electron transfer. Thus, generation of bond disorder is minimized under the optimal conditions, leading to SBH values near to the Mott-Schottky limit.

Additionally, the AlGaN/GaN system is a new material system recently attracting so much of attention for blue/UV photonic and high power electronic device applications. One of the serious problems, concerning the AlGaN/GaN high power transistor, has been unusually large leakage currents in Schottky gates. By using the optimized pulsed electrochemical process, we have recently achieved large reduction of reverse leakage currents on GaN Schottky contacts [51] as shown in **Fig.10**. This result has been explained by the thin surface barrier (TSB) model proposed by author's group [52,53]. Namely, the conventional high energy metal deposition process produces a high density of nitrogen-vacancy related defect donors at MS interface. These donors are ionized and decrease the thickness of Schottky barrier, leading anomalously large leakage currents due to tunneling. On the other hand, the low-energy electrochemical process reduces generation of such nitrogen-vacancy related defect donors.

An electrochemical surface treatment to reduce leakage currents [54] as well as pH sensitivity of GaN surface [55] have been reported recently, showing increased interests in electrochemistry of nitride semiconductors.

***4.3 Formation of nanometer scale Schottky contacts***

The pulsed in-situ electrochemical process has been formed suitable also for formation of nanometer scale Schottky (nano-Schottky) contacts [47, 56] that are required for gate control of quantum devices. This is because this process can form contacts consisting of metal nano-particles with nearly ideal MS interfaces that are free from interfacial oxides, and very accurate control of thickness is possible by controlling the numper of pulses. For the definition of the Schottky contact, the standard electron-beam (EB) lithography can be applied.

As an example, a SEM image of an array of Pt nano-Schottky contacts formed on n-GaAs is shown in **Fig. 11(a)**. Here, circular open windows with a diameter of 100 nm are patterned on the top of the GaAs surface by standard electron-beam (EB) lithography, and the nano-Schottky contacts are selectively formed within the open windows through which current supply from the semiconductor substrate is made. Interestingly, metal dots with a smaller diameter of about 50 nm are formed at the center of the window pattern of a diameter of 100 nm.

We have been also studying electrical properties of such nano-Schottky diodes in detail by I-V and C-V measurements [56-60]. **Figure 11(b)** shows forward I-V curves of the Pt/, Ni/ and Sn/n-GaAs nano-Schottky contacts with a diameter of 90 nm. I-V measurements have been carried out on each of individual nano-Schottky contacts by using an AFM system equipped with a conductive probe. For the nanometer-sized Schottky contacts with such small contact area, the current measurement by the Aglilent semiconductor parameter analyzer (HP-4156A) is difficult at low bias region, because the current levels are close to the detection limit of $10^{-14}$ A of the equipment.

I-V characteristics of nano-Schottky contacts are found to be very much influenced by the presence of Fermi level pinning on the free surface (air-semiconductor interface) near the contact periphery. The theoretical I-V curves obtained by the computer simulation which takes into this effect [57, 58] have provided excellent fitting to all I-V curves of the nano-Schottky contacts, as shown in **Fig. 11(b)**. The SBH values of 1.0 eV, 0.65 eV and 0.52 eV were obtained for the nano-Pt/, Ni/ and Sn/n-GaAs contacts by the theoretical fitting. These obtained SBH values are plotted in **Fig. 11(c)** against the work function of the barrier metal. The value of the slope factor defined by $S = d\phi_{Bn}/ d\phi_m$, is 0.38, showing strongly metal work function dependent SBH values. These results indicate that the electrochemical process can produce the nanometer-sized Schottky interfaces with very much reduced Fermi level pinning for III-V materials. This opens up an exciting possibilities for nano-scale deices where metal nanostructures play far more important and active roles for controlling semiconductor nanostructures.

## 5. Summary

In this paper, recent attempts by the authors' group at RCIQE, Hokkaido University, to investigate feasibility of utilizing electrochemical processes for nanometer-scale processing and nanostructure formation in III-V semiconductors have been reviewed. Topics included precisely controlled anodic etching of InP, controlled formation of InP nanopore arrays by anodization and their applications, and controlled formation of macroscopic and nanometer scale metal contacts on GaAs, InP and GaN by a pulsed in-situ electrodeposition which leads to substantial reduction of Fermi level pinning and reverse leakage currents.

All the results reported in this paper indicate that electrochemical processes can achieve unique and important results which can not be obtained by the conventional semiconductor technology. We strongly believe that further refinements of the electrochemical processing technologies will enhance their roles in semiconductor nanotechnology and nanoelectronics in the near future.

## Acknowledgements

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**Figures**

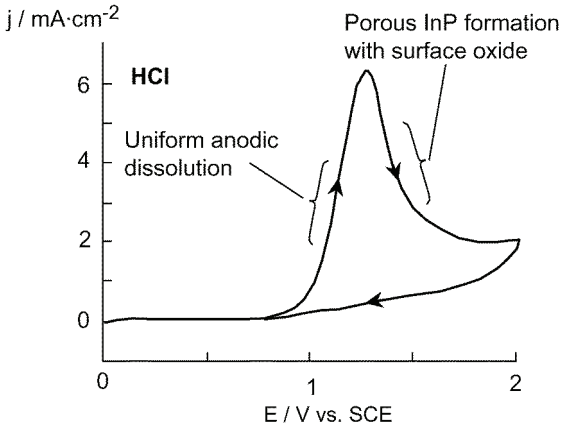


**Fig. 1** Cyclic voltammogram of n-InP in a dilute HCl solution with pH of a 1.0 in the dark.

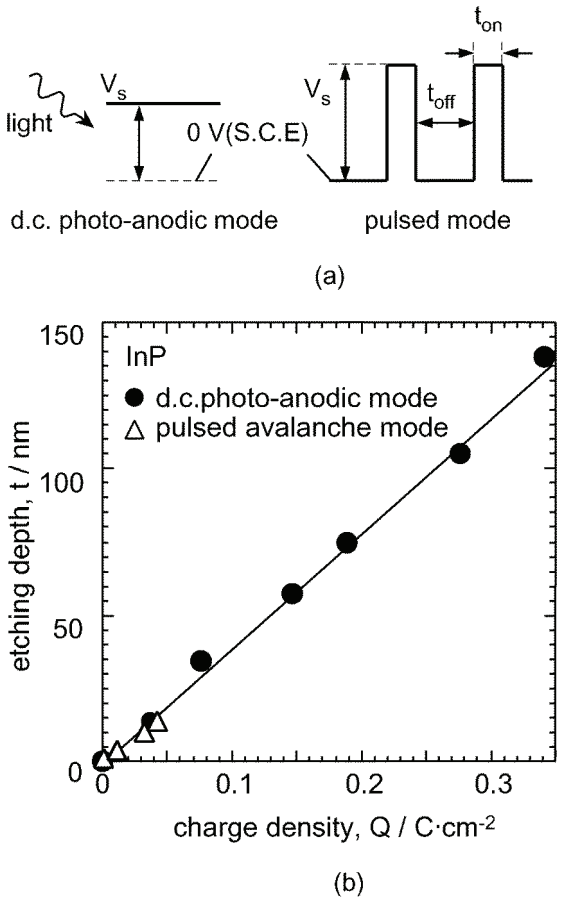


**Fig. 2** (a) The potential waveforms used for anodic etching and (b) relationship between etching depth, t, and charge density, Q, in the d.c. photo anodic mode and the pulsed avalanche mode.

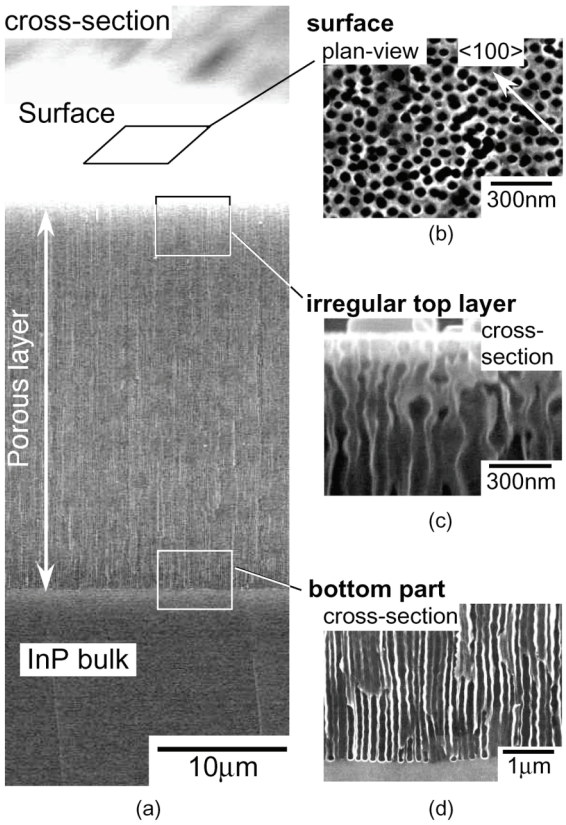


**Fig. 3** SEM images of wavy porous structures formed in Electrolyte A under $V_s$ = 5V and $t_a$=1min with light illumination.(a) Overall structure, (b) surface, (c) irregular top layer and (d) bottom part.

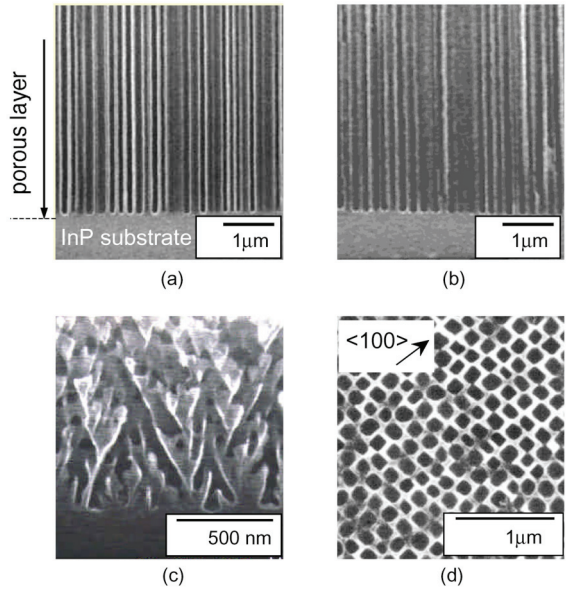


**Fig. 4** SEM images of <001>-oriented straight nanopore arrays: (a) the cross-section of straight nanopores obtained in Electrolyte B, (b) the cross-section of straight nanopores obtained in Electrolyte C, (c) nanopores with <113>-oriented branches obtained in Electrolyte A at $V_s$=2V and (d) plan view of InP nanopores formed in Electrolyte B.

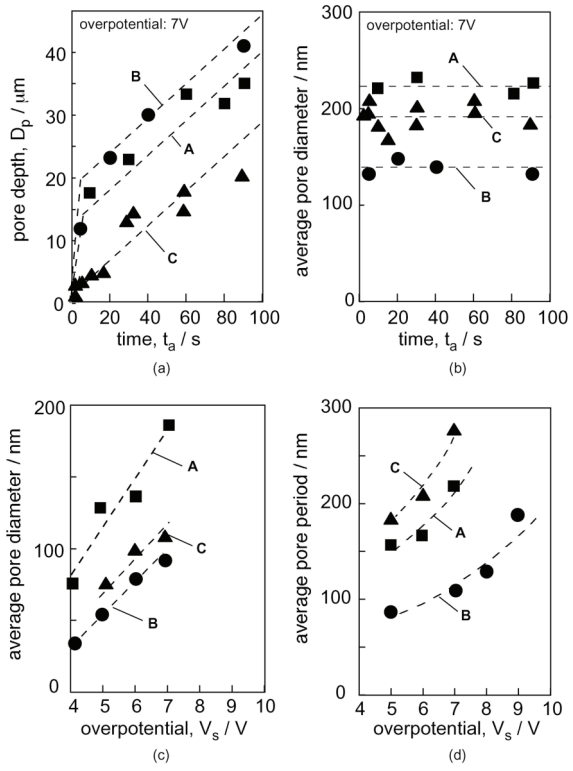


**Fig. 5** The measured data of (a) pore depth vs. time, (b) average pore diameter vs. time, (c) average pore diameter vs. $V_s$ and (d) average pore period vs. $V_s$ obtained by cross-sectional SEM observation.

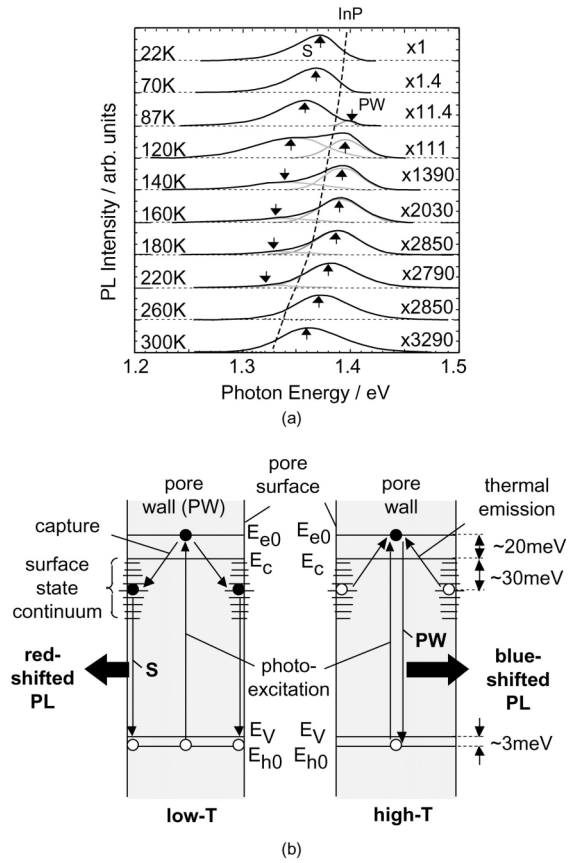


**Fig. 6** (a) PL spectra taken from nanopores formed in Electrolyte C at various measurement temperatures, showing presence of pore wall (PW) and surface state (S) components, and (b) a model for energy levels and radiative transition processes for PW and S emissions. The dashed curve in (a) shows PL peak positions of InP band edge emission.

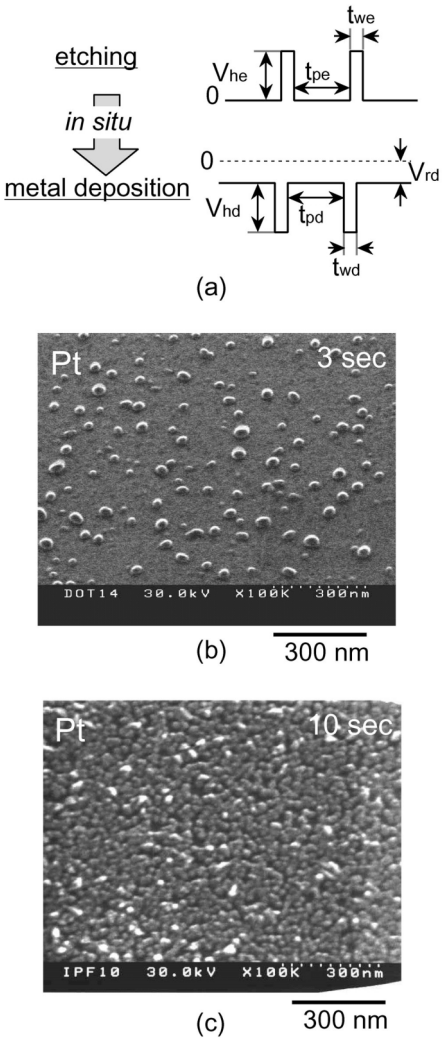


**Fig. 7** (a) Potential waveforms for etching and plating modes, (b) SEM image of self-assembled nanometer Pt particles after 3 sec of deposition and (c) that after 10sec of deposition.

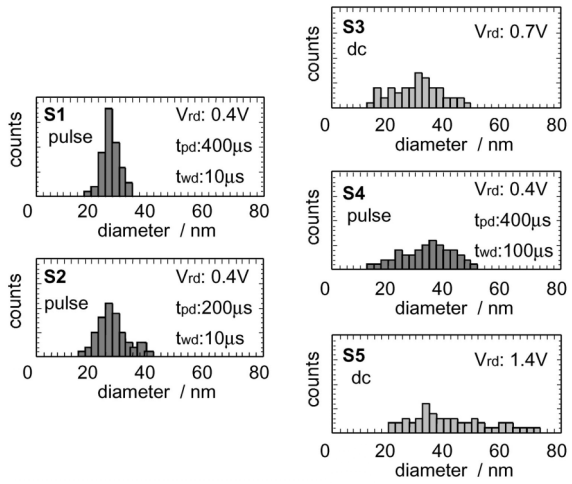


**Fig. 8** Size distribution of Pt nano-particles measured by AFM on five Pt/InP macroscopic Schottky samples, S1-S5, prepared under different electrochemical conditions.

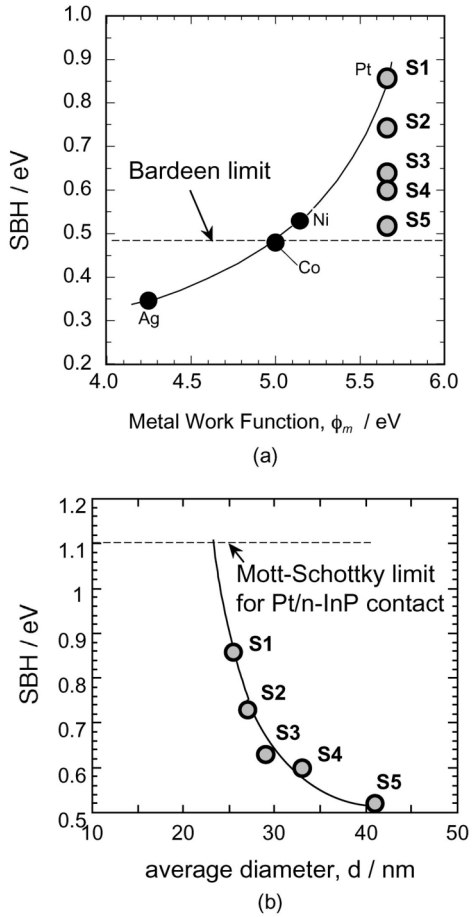


**Fig. 9** SBH values of various InP Schottky contacts; (a) metal work function dependence of SBH and (b) SBH values plotted vs. average particle diameter, d. S1 - S5 correspond to those in Fig. 15.

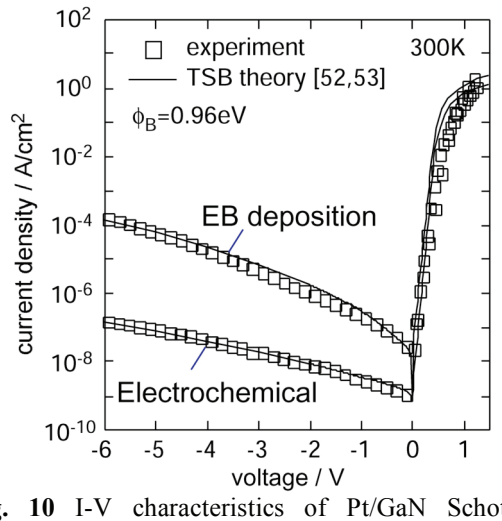


**Fig. 10** I-V characteristics of Pt/GaN Schottky contacts formed by the electrochemical process and by electron beam (EB) vacuum deposition process.

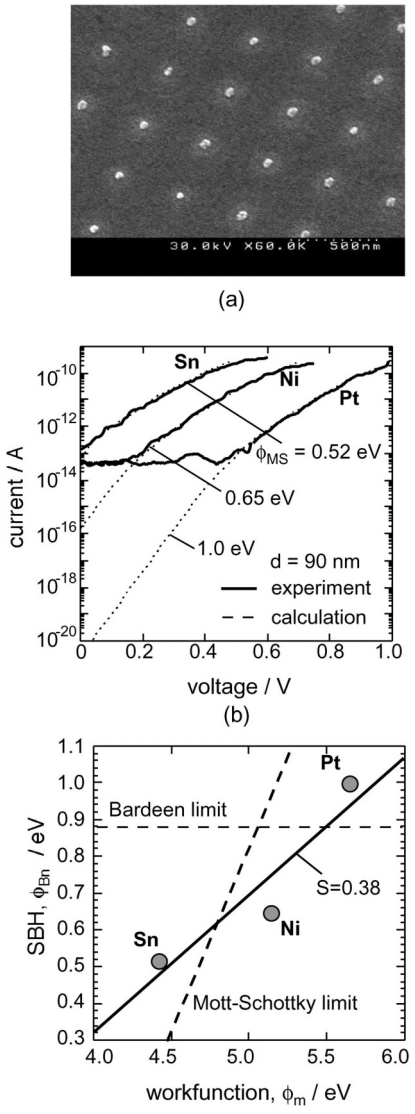


**Fig. 11** (a) SEM image, (b) forward I-V characteristics and (c) metal work function dependence of SBH of GaAs nano-Schottky contacts.