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学 位 論 文 内 容 の 要 旨

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学 位 論 文 題 名

Ring-VCO-based ADC design for low-energy smart sensing devices

(低電力スマートセンシングデバイスに向けたリング VCO 型 A/D 変換器の設計手法)

The rise of IoT sensor nodes enables continuous background monitoring of our internal physiological (blood oxygen, electrocardiography) and various external (surrounding) environmental (air quality, humidity, moisture, pressure, sound, and temperature) signals.

In recent years, Internet of Things (IoT) sensors are being powered using energy harvesters, motivated by mobile and battery-less operation in remote areas. Additionally, key to smart sensing is embedding or integrating IoT sensors with artificial intelligence, and it is a significant challenge due to their energy and resource requirements. In this thesis we report the development of a novel ring VCO-based ADC architecture suitable for ultra-low energy smart IoT sensors.

Analog-to-digital converters (ADCs) are a necessary part of the data acquisition in IoT sensors, and we designed a voltage-controlled oscillator based ADC using all digital circuits. Our motivation is based on the theory that VCO-based ADCs can be implemented very efficiently with a ring oscillator, which is a simple digital circuit. Fundamentally, a ring-VCO can generate digital code by counting its pulse frequency. Low energy IoT devices can benefit from scaling down the CMOS technology, this can reduce the operating voltage, therefore, minimizing power dissipation. Although the operating voltage is scaled down, the threshold voltage of transistors is not significantly reduced. VCO-based ADCs have been widely studied in a great deal of papers and it is known that one of its main drawbacks is the non-linearity of voltage-to-frequency (V-to-F) tuning characteristics it presents.

Furthermore, operating at a lower voltage could adversely affect the linearity of the V-to-F tuning characteristic. One of the objectives of this thesis is to improve the linear V-to-F characteristic of the ring-VCO, in which IoT systems are constrained in their supply voltage by ambient energy sources. We approach the new linearity improvement technique called complementary bias voltage control to achieve linear V-to-F characteristics of fully pseudo-differential current-starved inverter-based delay elements without using body bias. The complementary bias voltage control consists of the independent voltage-to-current (V-to-I) conversion,

which provides the linear bias current source and sinks matching for the current-starved transistor of delay elements. Additionally, the best nonlinearity error can be optimized by selecting an optimal transistor size. The second contribution of this thesis will facilitate reducing the size and area costs of future IoT sensor devices. By simplifying the development of fully pseudo-differential current-starved ring oscillators as observed in our first contribution. From our studies, reducing the number of transistors will not adversely affect the linearity of the V-to-F tuning characteristic.

Finally, inspired by AI-enabled intelligent sensing networks, we propose a pulse neuron circuit in

which fully pseudo-differential current-starved inverter-based delay elements with linearity technique are served as ReLU linear activation functions using their V-to-F tuning characteristic.

Furthermore, our experiments and studies show the nonlinearity effect of process variation, and we propose a compensation technique. All the three proposed circuit contributions have been proven by using Cadence Spectre (Virtuoso Design Environment version IC6.1.8-64b).

The simulation results with a 0.5V power supply circuit designed in TSMC 180nm CMOS technology are observed as follows:

(i) The measured maximum nonlinearity error is below 0.24% for 4-stage and below 0.49% for 8-stage ring-VCO.

(ii) Only 4-stage ring VCO can generate 8 phase signal, and it normally requires more than 9 numbers of delay cells.

(iii) The designed pulsed neuron circuit which can be used in DNN is benchmarked by MNIST performance, and we report average validation accuracy among five possible corners at approximately over 97%.