Significant Reduction in the Switching Time of Solid-State Electrochemical Thermal Transistors

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ABSTRACT: Thermal transistors that electrochemically switch the thermal conductivity (κ) of an active material have attracted growing attention as a device that controls heat flow. Although several thermal transistors have been demonstrated thus far, they would not be practical because of the use of liquid electrolytes. Recently, we have realized the first solid-state thermal transistors that electrochemically control the κ

of $SrCoO_x$ ($2 \leq x \leq 3$) using 0.5-mm-thick yttria-stabilized zirconia (YSZ) single crystal substrates as the solid electrolytes at 280 °C. However, because of the high electrical resistivity of YSZ at 280 °C, the applicable electric current is low (50 μA), and thus the κ switching takes time (~3 min). In this study, we fabricated several $SrCoO_x$-based thermal transistors using YSZ substrates with varied thicknesses. Regardless of the YSZ thickness, the x in $SrCoO_x$ was controlled between 2 and 3, and the κ was switched between 0.97 and 3.86 W m^{-1} K^{-1}. The overall electrical resistance decreased with decreasing the YSZ thickness. Consequently, when a 0.1-mm-thick YSZ substrate was used, the applicable current was increased to 1 mA and the switching time was significantly reduced to ~10 seconds.

INTRODUCTION

With the miniaturization and ultra-high integration of electronic devices, the heat generated in ultra-microscopic areas on the nanometer scale causes device malfunctions and failures. Therefore, heat sinks or Peltier devices are used to remove the heat. On the other hand, if such minute heat can be effectively reused as energy using thermoelectric conversion technology, for example, it will be possible to reduce energy loss. However, unlike electrons, heat easily diffuses outside the system. Hence, in order to effectively reuse heat without waste, it is necessary to develop a "thermal circuit"[1] that receives heat near the heat source and transports it as a heat flow.

In the case of electronic circuits, transistors play a central role to control electron flow. For example, in a thin film transistor, the conductivity of the active layer can be adjusted by applying a gate electric field to switch the current flowing between the

source and the drain. In thermal circuits, as in electronic circuits, if the heat flowing through the circuits can be regulated, it would be a great step towards efficient reuse of heat. In recent years, a "thermal transistor"[2], which can be said to be a "heat flow version" of a transistor that controls current, has been proposed theoretically[3-5] and has attracted attention.

There are two types of thermal transistors. In 2007, Wang and Li theoretically proposed a thermal transistor that modulates heat transport by a heat input[3]. Very recently, Castelli *et al*. demonstrated such thermal transistors utilizing paramagnetic/ferromagnetic switching of a magnet that mechanically controls the heat conductance[6]. On the other hand, in 2014, Ben-Abdallah and Biehs theoretically proposed a thermal transistor that modulates the thermal conductivity of the active material (VO_2) electrically[5]. It is known that VO_2 shows insulator-to-metal transition around 68 °C and a metallic VO_2 shows large electrical conductivity ($\sigma \sim 10^4$ S cm^{-1})[7]. According to the Wiedemann-Frantz law [$\kappa_{ele} = L \cdot \sigma \cdot T$, where L is the Lorentz number (2.44×10^{-8} W Ω K^{-2}) and T is the absolute temperature], it is expected that a metallic VO_2 shows large electron thermal conductivity (κ_{ele}) at least ~7 W m^{-1} K^{-1} higher than the insulator VO_2[7]. However, in reality, the κ values of VO_2 before and after the insulator-to-metal transition are almost the same (~6 W m^{-1} K^{-1})[8].

Recently, several electrochemical thermal transistors have been demonstrated using various active materials[9-18]. In 2014, Cho *et al*. realized the first thermal transistor that modulates the κ of Li_xCoO_2 electrochemically[9]. κ of the $LiCoO_2$ film was reversibly modulated in the range of ~5.4–3.7 W m^{-1} K^{-1}. The ON/OFF κ ratio was ~1.5. After

that, several electrochemical thermal transistors with various active materials such as black phosphorous (ON/OFF κ ratio ~6)[10], MoS_2 (ON/OFF κ ratio ~10)[11], $SrCoO_x$ (ON/OFF κ ratio ~10)[12], and $La_{0.5}Sr_{0.5}CoO_{3-\delta}$ (ON/OFF κ ratio ~5.4)[18] were demonstrated. These electrochemical thermal transistors that can be operated at room temperature display rather large ON/OFF κ ratios. However, these electrochemical thermal transistors are composed of liquid electrolytes or ionic liquids. Thus, they are inappropriate for practical devices as they must be placed in containers and sealed to prevent liquid leakage.

In 2023, we realized the first solid-state thermal transistors that can be operated at 280 °C in air by using 0.5-mm-thick yttria-stabilized zirconia (YSZ) single crystal substrates as the solid electrolyte and $SrCoO_x$ ($2 \leq x \leq 3$) as the active material[16, 17]. The operatable temperature is higher than that composed of liquid electrolytes or ionic liquids (room temperature) because of the low oxide ion conductivity of YSZ ($\sigma \sim 10^{-15}$ S cm^{-1} at room temperature. $\sigma \sim 10^{-6}$ S cm^{-1} at 280 °C (**Fig. S1**). *cf*. Ultrapure water (major origin of oxidation and protonation when use of ionic liquids): $\sigma \sim 0.55 \times 10^{-6}$ S cm^{-1} at room temperature). The ON/OFF κ ratio is ~4, which is comparable to that for liquid electrolyte-based thermal transistors[9-15]. However, the electrical resistance of the 0.5-mm-thick YSZ single crystal[19] substrate in these $SrCoO_x$-based solid-state thermal transistors is very high (~100 kΩ at 280 °C). Hence, the applicable electric current is low (50 μA), and thus the κ switching takes time (~3 min). In order to reduce the operating temperature, we should use other solid electrolytes that exhibit high ionic conductivity at lower temperatures such as CeO_2-based materials[20, 21]. On the other hand, the κ switching time might be shortened by reducing the thickness of the YSZ

single crystal substrates because the applicable electric current increases. The electrical conductivity of YSZ bulk single crystal at 280 °C is ~1.5 μS cm^{-1} (**Fig. S1**). Thus, the electrical resistance of YSZ ($R_{YSZ\ bulk}$) is 250 kΩ when the YSZ substrate is 5 mm × 5 mm × 1 mm. Reducing the YSZ thickness from 1 mm to 0.1 mm should yield $R_{YSZ\ bulk}$ of 25 kΩ. However, the influence of the YSZ thickness on thermal transistor fabrication and operation remains unclear. If the thermal transistor fabrication and operations are unaffected, then a larger current can be applied, which should significantly reduce the κ switching time.

In this study, we fabricated $SrCoO_x$-based solid-state thermal transistors using YSZ substrates with various thicknesses (**Fig. 1a**). For all samples, the x in $SrCoO_x$ was between 2 and 3, and the κ was switched between 0.97 and 3.86 W m^{-1} K^{-1}. The overall electrical resistance decreased with decreasing the YSZ thickness. Consequently, when a 0.1-mm-thick YSZ substrate was used, the applicable current was increased to 1 mA and the switching time was significantly reduced to ~10 seconds.

RESULTS AND DISCUSSION

Solid-state electrochemical thermal transistors with $SrCoO_x$ films (80 nm) deposited on 10-nm-thick GDC-buffered YSZ substrates (thickness: 0.1 mm, 0.2 mm, 0.5 mm, and 1.0 mm) were fabricated according to the previous reports[16, 17]. An electrochemical redox treatment was performed at 280 °C in air. Specifically, a constant current of ±50 μA was applied for a predetermined time using Faraday's law of electrolysis (~220 s). The electron density (Q) was controlled by the current application time as $Q = (I \cdot t)/(e \cdot V)$, where I is the flown current, t is the current application time, e is the electron

charge, and V is the volume of the $SrCoO_x$ film (5 mm × 5 mm × 80 nm). The electrochemical oxidation/reduction reaction is given as:

Oxidation: $SrCoO_2 + O^{2-} \rightarrow SrCoO_3 + 2e^-$, $Q \sim 3.4 \times 10^{22}$ cm^{-3}

Reduction: $SrCoO_3 + 2e^- \rightarrow SrCoO_2 + O^{2-}$, $Q \sim 3.4 \times 10^{22}$ cm^{-3}

During the oxidation or reduction treatment, we monitored the change in the required voltage and time. Afterwards, the sample was immediately cooled to room temperature.

The out-of-plane XRD patterns of the resultant thermal transistors (**Fig. S2**) reveal that the crystal structure of $SrCoO_x$ is controlled in defect perovskite (DP, fully reduced, x = 2), brownmillerite (BM, as-grown, x = 2.5), and perovskite (P, fully oxidized, x = 3). We calculated the out-of-plane lattice parameter of the $SrCoO_x$ using the diffraction peaks of 008_{BM}, 002_P, and 002_{DP}. **Figure 1b** plots the lattice parameters of the $SrCoO_x$ films as a function of the YSZ thickness. The obtained values agree well with the previous reports[16, 17] (solid lines). Detail of the crystal structure and the optoelectronic properties of the $SrCoO_x$ have been reported elsewhere[16].

Next, we measured the cross-plane κ of the $SrCoO_x$ films by the TDTR method at room temperature (**Figs. 1c** and **S2**). The observed κ values for each oxidized and reduced state are independent of the YSZ thickness. The average κ of the oxidized $SrCoO_3$ films is 3.86 W m^{-1} K^{-1} while that of the reduced $SrCoO_2$ is 0.97 W m^{-1} K^{-1}. Consequently, the crystal structure and the thermal conductivity of the $SrCoO_x$ films are independent of the YSZ thickness.

We then measured the ac impedance of the thermal transistors with different YSZ

thicknesses at 280 °C in air. To minimize the electrical resistance of the $SrCoO_x$ films, the thermal transistors were fully oxidized before the impedance measurements. The resultant Cole-Cole plots show two semicircles (**Figs. 2a−d**). The larger semicircle obtained from the higher frequency indicates the resistance of bulk YSZ ($R_{\text{YSZ bulk}}$). The observed $R_{\text{YSZ bulk}}$ values agree well with the ones calculated from the Arrhenius plot (**Fig. S1**), except in the case of YSZ thickness = 1.0 mm (**Fig. 2e**). Since the thermal transistor was placed on the heater stage (280 °C), but the surrounding environment was kept at room temperature (25 °C), the temperature at the top surface of the thicker thermal transistor may be less than 280 °C.

The other semicircle in each plot indicates the resistance of the YSZ interface ($R_{\text{YSZ interface}}$) that correspond to small angle grain boundaries in the YSZ crystals. Since oxidized $SrCoO_3$ is a good electrical conductor with electrical conductivity of ~1.4×10^3 S cm^{-1}, it does not affect the size of the semicircle. $R_{\text{YSZ interface}}$ depends on the YSZ thickness, indicating small angle grain boundaries are homogeneously distributed in the YSZ single crystals. For a YSZ thickness of 0.1 mm, $R_{\text{Interface}}$ is only ~10 kΩ, but it exceeds 150 kΩ when the YSZ thickness is 1.0 mm (**Fig. 2e**). Hence, decreasing the YSZ thickness can reduce the overall resistance of the thermal transistor.

We then analyzed the change in the dc resistance of the thermal transistor during oxidation/reduction treatment. **Figure 3** summarizes the change in the required voltage as a function of the applied electron density (Q) to the thermal transistors at 280 °C. The required voltage systematically decreases as the YSZ thickness decreases due to the smaller $R_{\text{YSZ bulk}}$ and $R_{\text{YSZ interface}}$ values. In both the oxidation from fully reduced

$SrCoO_2$ to fully oxidized $SrCoO_3$ (**Fig. 3a**) and reduction from fully oxidized $SrCoO_2$ to fully reduced $SrCoO_3$ (**Fig. 3b**) cases, two stepwise voltage changes were observed, possibly due to the crystallographic phase change, around Q ~0.5×10^{22} cm^{-3} and ~2×10^{22} cm^{-3}.

To visualize the voltage change, we plotted dV/dQ as a function of Q (**Fig. 4**). In the case of oxidation (**Fig. 4a**), three dV/dQ peaks are detected at 2.8×10^{21} cm^{-3}, 6.0×10^{21} cm^{-3}, and 1.9×10^{22} cm^{-3}. In the case of reduction (**Fig. 4b**), two dV/dQ peaks are detected at 5.8×10^{21} cm^{-3} and 2.1×10^{22} cm^{-3}. These peaks should correspond to the change in the crystal structure of $SrCoO_x$ films among DP, BM, and P. Since there is a superstructure phase between DP and BM phases, the dV/dQ peak located at 2.8×10^{21} cm^{-3} may be related to the superstructure phase formation[16].

Next, we measured the Cole-Cole plots of the thermal transistor with 0.1-mm-thick YSZ substrate after the oxidation (**Fig. 5a**) and reduction treatments (**Fig. 5b**). The electrical resistance of the YSZ substrate ($R_{YSZ\ bulk}$) did not change after the oxidation and reduction treatments (~23 kΩ). The interfacial electrical resistance ($R_{YSZ\ interface}$) after the oxidation is ~10 kΩ. After the reduction treatment, the shape of semicircle became flatten, indicating resistance of the DP phase (R_{DP} ~10 kΩ) is superimposed. These observations suggest that oxide ion conductivity of the DP phase is ~3×10^{-9} S cm^{-1}.

Finally, we increased the applied current to reduce the switching time. **Figures 6a** and **6b** plot the changes in the required voltage in the current application during oxidation and reduction, respectively. Although the required voltage is increased, applying 1 mA

for ~10 s oxidizes and reduces the $SrCoO_x$ films. These results clearly indicate that use of thinner YSZ single crystal significantly reduces the switching time of the $SrCoO_x$/GDC/YSZ-based solid-state electrochemical thermal transistors.

Is there minimum thickness of YSZ single crystal that can be used for the thermal transistors? As the technical issue, when the thickness of YSZ single crystal is thinner than 0.1 mm, the single crystal is easily broken into pieces due to mechanical stress during the grinding. Use of YSZ epitaxial films might be a good solution to reduce the thickness. Probably, the limitation is related to the breakdown field of YSZ. That is, when an electrical breakdown occurs, electron flows according to the electric field. Therefore, the solid electrolyte does not play as the ion conductor. Currently, we are considering ways how to reduce the thickness of YSZ as well as the use of another oxide ion conducting solid electrolyte exhibiting higher oxide ion conductivity ($\sigma \sim 10^{-3}$ S cm^{-3} at 280 °C) than that of YSZ ($\sigma \sim 10^{-6}$ S cm^{-1} at 280 °C).

CONCLUSION

Simply reducing the thickness of the solid electrolyte drastically reduces the switching time in $SrCoO_x$-based solid-state thermal transistors on YSZ substrates. In all samples, the x in $SrCoO_x$ was between 2 and 3, and the κ was switched between 0.97 and 3.86 W m^{-1} K^{-1}. Because the overall electrical resistance decreases upon reducing the YSZ thickness, the applied current is increased to 1 mA, which is 20 times larger than that in the previous reports (50 μA)[16, 17]. A 0.1-mm-thick YSZ substrate significantly reduces the switching time from 3 minutes to ~10 seconds.

Reduction of the YSZ thickness improves the thermal transistor characteristics. However, use of thinner YSZ single crystals (thickness < 0.1 mm) are not appropriate for the thermal transistor application because they are easily broken into pieces due to mechanical stress during the grinding. Use of YSZ epitaxial films might be a good solution to reduce the thickness. Currently, we are considering ways how to reduce the thickness of YSZ as well as the use of oxide ion conducting solid electrolyte exhibiting higher oxide ion conductivity ($\sigma \sim 10^{-3}$ S cm^{-3} at 280 °C) than that of YSZ ($\sigma \sim 10^{-6}$ S cm^{-1} at 280 °C).

EXPERIMENTAL

Fabrication of $SrCoO_x$-based solid-state electrochemical thermal transistors. 80-nm-thick $SrCoO_{2.5}$ films were heteroepitaxially grown on 10% Gd-doped CeO_2 (GDC) buffered (001)-oriented YSZ substrates via the pulsed laser deposition (PLD) technique[16, 22]. First, ~10-nm-thick GDC was heteroepitaxially grown on a YSZ (10 mm × 10 mm × z mm, where z = 0.1 mm, 0.2 mm, 0.5 mm, or 1.0 mm, double-sided polished, Crystal Base) substrate at 750 °C in an oxygen atmosphere (10 Pa). Focused KrF excimer laser pulses (λ = 248 nm, fluence ~2 J cm^{-2} pulse^{-1}, repetition rate = 10 Hz) were irradiated onto the ceramic target of GDC followed by the ceramic target of $SrCoO_x$. Then a ~40-nm-thick Pt film was sputtered on the top surface of the $SrCoO_{2.5}$ epitaxial film followed by low density Pt film sputtering on the backside of the YSZ substrate. Pt sputtering occurred at room temperature. Finally, the sample was cut into four squares (5 mm × 5 mm).

Electrochemical redox treatments. A thermal transistor (5 mm × 5 mm) was placed on

a Pt-coated glass substrate, which was heated to 280 °C in air. Then an electrochemical redox treatment was performed by applying a constant current of ±50 μA, ±0.2 mA, ±0.5 mA, or ±1 mA while, we monitored the change in the required voltage and time. Afterwards, the sample was immediately cooled to room temperature.

Crystallographic analyses. The crystalline phase, orientation, and lattice parameters of the resultant films were analyzed by high-resolution XRD (Cu $K\alpha_1$, λ = 1.54059 Å, ATX-G, Rigaku). The out-of-plane Bragg diffraction patterns were measured at room temperature to clarify the changes in the crystalline phase of $SrCoO_x$ ($2 \leq x \leq 3$). The lattice parameters were calculated from the diffraction peaks.

Measurements of κ. κ of the $SrCoO_x$ films perpendicular to the substrate surface was measured by time-domain thermoreflectance (TDTR, PicoTR, PicoTherm). The top Pt film served as the transducer, and the decay curves of the TDTR signals were simulated to obtain κ. The specific heat capacities of the layers used for the TDTR simulation were 132 J kg^{-1} K^{-1} for Pt, 485 J kg^{-1} K^{-1} for $SrCoO_x$, and 460 J kg^{-1} K^{-1} for YSZ. The TDTR method is described elsewhere[16, 23-25]. Regarding the treatment of the thermal conductivity values, since there are several uncertainties such as position of the baseline, position of the time zero, and noise of the signal, we used the error bars of ±10% of the obtained values.

AC impedance measurements. AC impedance measurements of the thermal transistors were performed using the same setup as that for the electrochemical redox treatments (280 °C, in air). We used a potentio-galvano stat (VersaSTAT) to measure the impedance

ranging from 100 kHz to 0.1 Hz.

ASSOCIATED CONTENT

Supporting Information is available free of charge via the Internet at https://pubs.acs.org/doi/10.1021/acsaem.XXXXXXX.

Arrhenius plot of the electrical conductivity of YSZ single crystal substrate; Changes in the out-of-plane XRD patterns of the solid-state electrochemical thermal transistors; Decay curves of the thermoreflectance phase signal for the thermal transistors with various YSZ thicknesses

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Author Contributions

M.Y., Q.Y., and Z.B. fabricated the samples and measured the thermal transistor characteristics. H.O. planned and supervised the project. All authors discussed the results and commented on the manuscript.

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Notes

The authors declare no competing interest.

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REFERENCES

(1) Wehmeyer, G.; Yabuki, T.; Monachon, C.; Wu, J.; Dames, C. Thermal Diodes, Regulators, and Switches: Physical Mechanisms and Potential Applications. *Appl. Phys. Rev.* **2017,** 4.

(2) Swoboda, T.; Klinar, K.; Yalamarthy, A. S.; Kitanovski, A.; Rojo, M. M. Solid-State Thermal Control Devices. *Adv. Electron. Mater.* **2021,** 7, 2000625.

(3) Li, B.; Wang, L.; Casati, G. Negative Differential Thermal Resistance and Thermal Transistor. *Appl. Phys. Lett.* **2006,** 88, 143501.

(4) Wang, L.; Li, B. Thermal Logic Gates: Computation with Phonons. *Phys. Rev. Lett.* **2007,** 99, 177208.

(5) Ben-Abdallah, P.; Biehs, S. A. Near-Field Thermal Transistor. *Phys. Rev. Lett.* **2014,** 112, 044301.

(6) Castelli, L.; Zhu, Q.; Shimokusu, T. J.; Wehmeyer, G. A Three-Terminal Magnetic Thermal transistor. *Nat. Commun.* **2023,** 14, 393.

(7) Lee, S.; Hippalgaonkar, K.; Yang, F.; Hong, J. W.; Ko, C.; Suh, J.; Liu, K.; Wang, K.; Urban, J. J.; Zhang, X.; Dames, C.; Hartnoll, S. A.; Delaire, O.; Wu, J. Q. Anomalously Low Electronic Thermal Conductivity in Metallic Vanadium Dioxide. *Science* **2017,** 355, 371.

(8) Berglund, C. N.; Guggenheim, H. J. Electronic Properties of VO_2 near the

Semiconductor-Metal Transition. *Phys. Rev.* **1969,** 185, 1022-1033.

(9) Cho, J.; Losego, M. D.; Zhang, H. G.; Kim, H.; Zuo, J.; Petrov, I.; Cahill, D. G.; Braun, P. V. Electrochemically Tunable Thermal Conductivity of Lithium Cobalt Oxide. *Nat. Commun.* **2014,** 5, 4035.

(10) Kang, J. S.; Ke, M.; Hu, Y. J. Ionic Intercalation in Two-Dimensional van der Waals Materials: In Situ Characterization and Electrochemical Control of the Anisotropic Thermal Conductivity of Black Phosphorus. *Nano Lett.* **2017,** 17, 1431-1438.

(11) Sood, A.; Xiong, F.; Chen, S.; Wang, H.; Selli, D.; Zhang, J.; McClellan, C. J.; Sun, J.; Donadio, D.; Cui, Y.; Pop, E.; Goodson, K. E. An Electrochemical Thermal Transistor. *Nat. Commun.* **2018,** 9, 4510.

(12) Lu, Q.; Huberman, S.; Zhang, H.; Song, Q.; Wang, J.; Vardar, G.; Hunt, A.; Waluyo, I.; Chen, G.; Yildiz, B. Bi-directional Tuning of Thermal Transport in $SrCoO_x$ with Electrochemically Induced Phase Transitions. *Nature Mater.* **2020,** 19, 655-662.

(13) Terakado, N.; Nara, Y.; Machida, Y.; Takahashi, Y.; Fujiwara, T. Dynamic Control of Heat Flow using a Spin-Chain Ladder Cuprate Film and an Ionic liquid. *Sci. Rep.* **2020,** 10, 14468.

(14) Yang, X.; Wang, S. Z.; Wang, C. Y.; Lu, R.; Zheng, X. H.; Zhang, T.; Liu, M.; Zheng, J.; Chen, H. S. Thermal Rectifier and Thermal Transistor of 1T/2H MoS_2 for Heat Flow Management. *ACS Appl. Mater. Interfaces* **2022,** 14, 4434-4442.

(15) Zhou, J.; Wu, Y.; Kwon, H.; Li, Y.; Xiao, X.; Ye, Y.; Ma, Y.; Goodson, K. E.; Hwang, H. Y.; Cui, Y. Heat Conductor-Insulator Transition in Electrochemically Controlled Hybrid Superlattices. *Nano Lett.* **2022,** 22, 5443-5450.

(16) Yang, Q.; Cho, H. J.; Bian, Z.; Yoshimura, M.; Lee, J.; Jeen, H.; Lin, J.; Wei, J.;

Feng, B.; Ikuhara, Y.; Ohta, H. Solid-State Electrochemical Thermal Transistors. *Adv. Funct. Mater.* **2023,** 33, 2214939.

(17) Bian, Z.; Yang, Q.; Yoshimura, M.; Cho, H. J.; Lee, J.; Jeen, H.; Endo, T.; Matsuo, Y.; Ohta, H. Solid-State Electrochemical Thermal Transistors with Strontium Cobaltite-Strontium Ferrite Solid Solutions as the Active Layers. *ACS Appl. Mater. Interfaces* **2023,** 15, 23512-23517.

(18) Zhang, Y.; Postiglione, W. M.; Xie, R.; Zhang, C.; Zhou, H.; Chaturvedi, V.; Heltemes, K.; Zhou, H.; Feng, T.; Leighton, C.; Wang, X. Wide-Range Continuous Tuning of the Thermal Conductivity of $La_{0.5}Sr_{0.5}CoO_{3-\delta}$ Films via Room-Temperature Ion-Gel Gating. *Nat. Commun.* **2023,** 14, 2626.

(19) Ikeda, S.; Sakurai, O.; Uematsu, K.; Mizutani, N.; Kato, M. Electrical-Conductivity of Yttria-Stabilized Zirconia Single-Crystals. *J. Mater. Sci.* **1985,** 20, 4593-4600.

(20) Yahiro, H.; Eguchi, Y.; Eguchi, K.; Arai, H. Oxygen Ion Conductivity of the Ceria Samarium Oxide System with Fluorite Structure. *J. Appl. Electrochem.* **1988,** 18, 527-531.

(21) Yamaguchi, S.; Tasaki, Y.; Kobayashi, M.; Horiba, K.; Kumigashira, H.; Higuchi, T. Electronic Structure and Oxygen Ion Conductivity of As-Deposited $Ce_{0.90}Sm_{0.10}O_{2-\delta}$ Thin Film Prepared by RF Magnetron Sputtering. *Jpn. J. Appl. Phys.* **2015,** 54.

(22) Yang, Q.; Cho, H. J.; Jeen, H.; Ohta, H. Macroscopic Visualization of Fast Electrochemical Reaction of $SrCoO_x$ Oxygen Sponge. *Adv. Mater. Interfaces* **2019,** 6, 1901260.

(23) Cho, H. J.; Takashima, Y.; Nezu, Y.; Onozato, T.; Ohta, H. Anisotropic Heat Conduction in Ion-Substituted Layered Cobalt Oxides. *Adv. Mater. Interfaces* **2020,** 7, 1901816.

(24) Takashima, Y.; Zhang, Y.; Wei, J.; Feng, B.; Ikuhara, Y.; Cho, H. J.; Ohta, H. Layered Cobalt Oxide Epitaxial Films Exhibiting Thermoelectric $ZT = 0.11$ at Room Temperature. *J. Mater. Chem. A* **2021,** 9, 274-280.

(25) Cho, H. J.; Wu, Y. Z.; Zhang, Y. Q.; Feng, B.; Mikami, M.; Shin, W.; Ikuhara, Y.; Sheu, Y. M.; Saito, K.; Ohta, H. Anomalously Low Heat Conduction in Single-Crystal Superlattice Ceramics Lower Than Randomly Oriented Polycrystals. *Adv. Mater. Interfaces* **2021,** 8, 2001932.

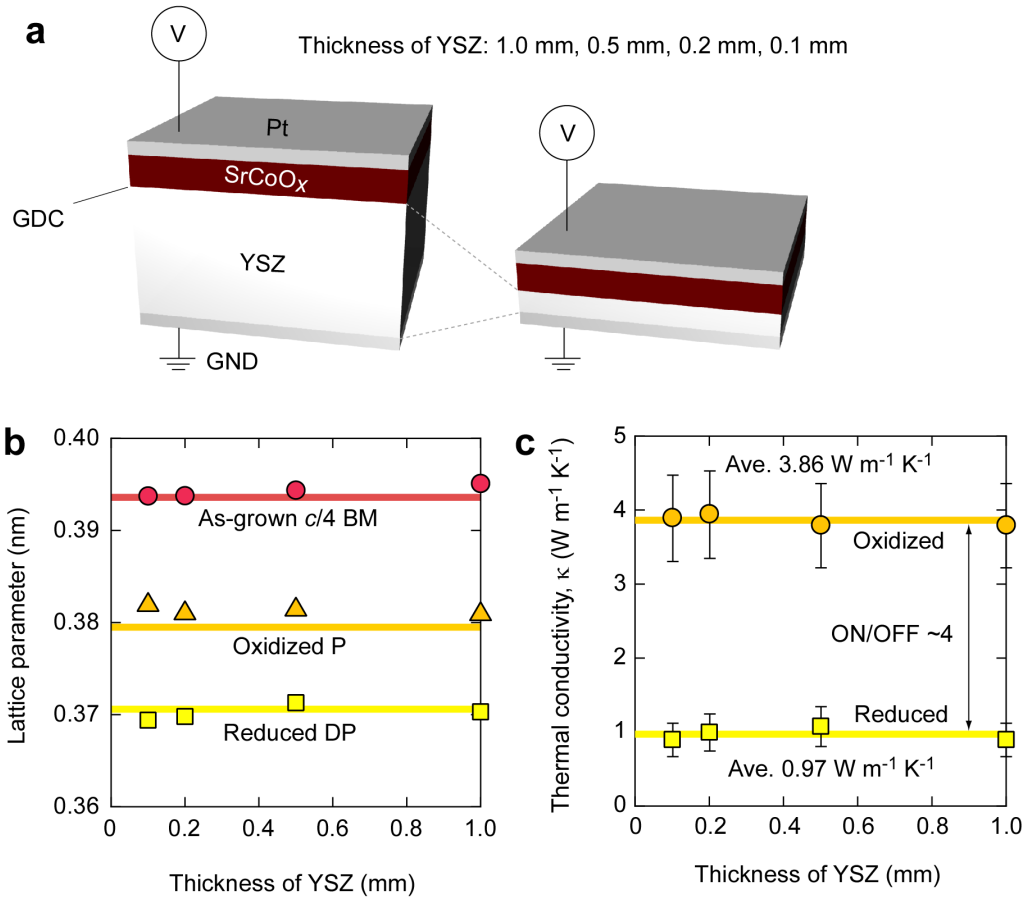


Figure 1. Solid-state electrochemical thermal transistors with various YSZ thicknesses. (a) Schematic of a $SrCoO_x$-based thermal transistor composed of a Pt top electrode, $SrCoO_x$ active layer, GDC layer, YSZ (solid electrolyte) substrate, and Pt bottom electrode. YSZ substrate thickness is 1.0 mm, 0.5 mm, 0.2 mm, or 0.1 mm. (b) Out-of-plane lattice parameter of $SrCoO_x$ layer as a function of YSZ thickness. (c) Change in the thermal conductivity of the $SrCoO_x$ layer as a function of YSZ thickness. For all samples, x in $SrCoO_x$ is between 2 and 3.

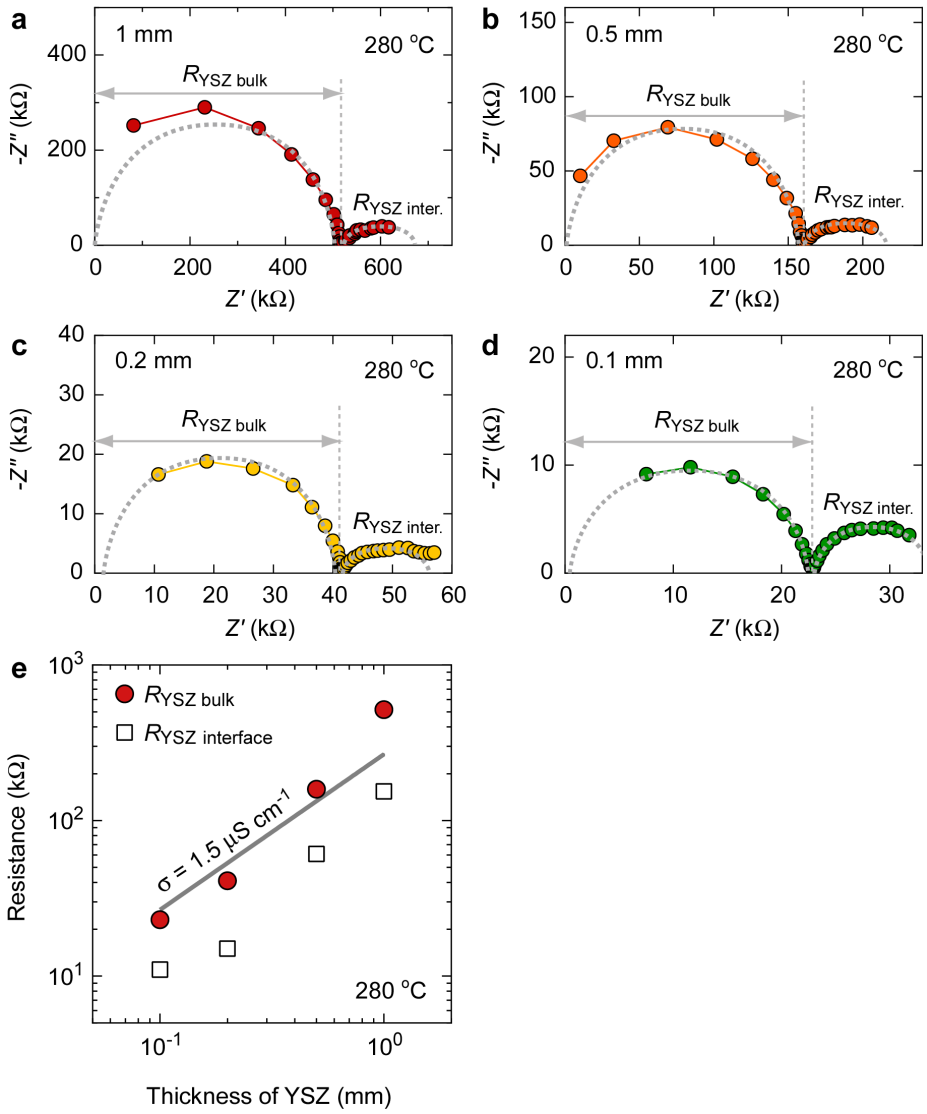


Figure 2. Electrical resistance of the YSZ single crystal substrates. (a−d) Cole-Cole plots of the thermal transistors with various YSZ thicknesses. (a) 1 mm, (b) 0.5 mm, (c) 0.2 mm, and (d) 0.1 mm. AC impedance measurements of thermal transistors in the fully oxidize states acquired at 280 °C in air. Two semicircles are clearly visible. Both $R_{YSZ\ bulk}$ and $R_{YSZ\ interface}$ increase as the YSZ thickness increases. (e) Change in the electrical resistance of the YSZ substrate (5 mm × 5 mm × z mm, z = 0.1, 0.2, 0.5, and 1) as a function of YSZ thickness. The solid line indicates the electrical conductivity σ = 1.5 μS cm^{-1}.

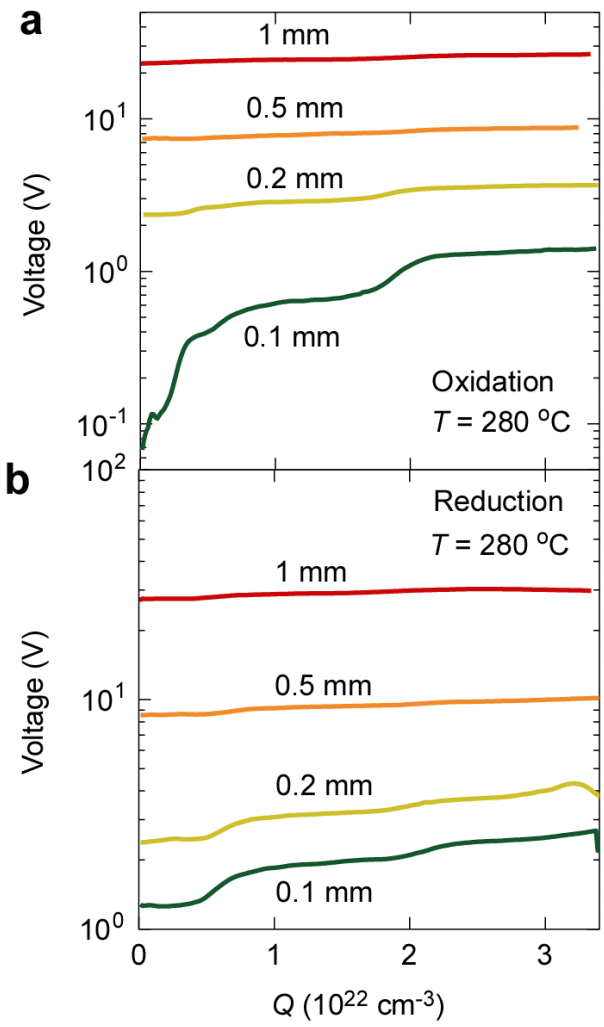


Figure 3. Changes in the applied voltage during the electrochemical redox treatment at 280 °C in air. (a) Oxidation, (b) Reduction. Stepwise increases in the applied voltage occur around $Q = 0.5 \times 10^{22}$ cm^{-3} and 2×10^{22} cm^{-3}.

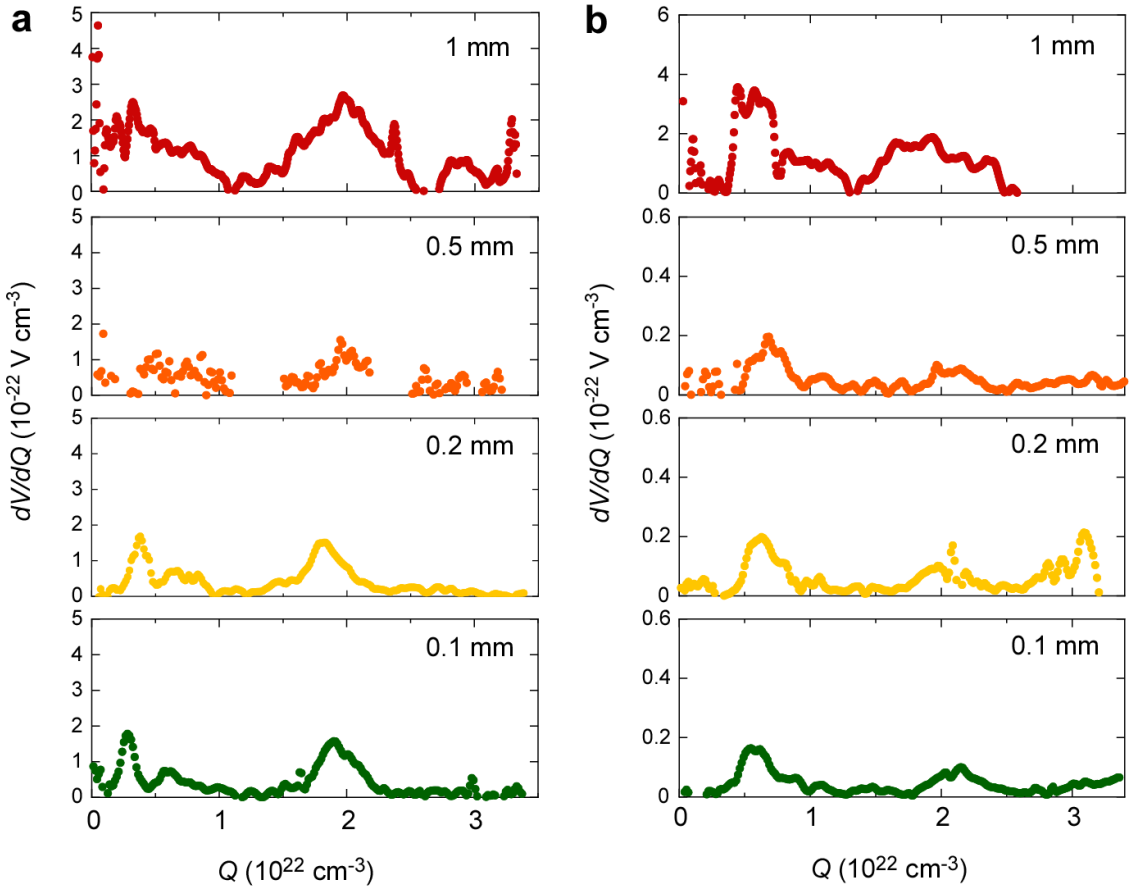


Figure 4. Changes in the *dV*/*dQ* during the electrochemical (c) oxidation and (d) reduction. During oxidation treatment, three peaks of *dV*/*dQ* are detected at 2.8×10^{21} cm^{-3}, 6.0×10^{21} cm^{-3}, and 1.9×10^{22} cm^{-3}. In the case of reduction, two peaks of *dV*/*dQ* are detected at 5.8×10^{21} cm^{-3} and 2.1×10^{22} cm^{-3}. These peaks correspond to the change in the crystal structure of $SrCoO_x$ films among DP, BM, and P.

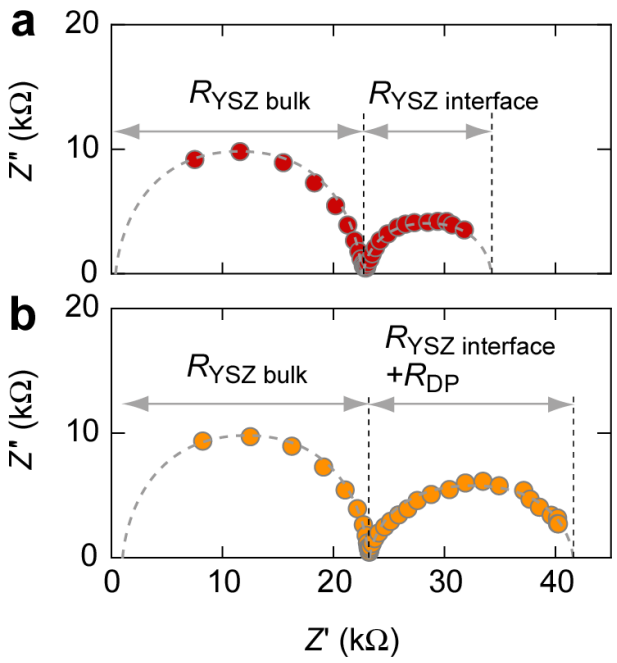


Figure 5. Cole-Cole plots of the thermal transistor with a 0.1-mm-thick YSZ substrate after (a) oxidation and (b) reduction. Electrical resistance of the YSZ substrate ($R_{\text{YSZ bulk}}$) is ~23 kΩ. Interfacial electrical resistance ($R_{\text{YSZ interface}}$) after the oxidation treatment is ~10 kΩ. After the reduction treatment, electrical resistance of the DP phase (R_{DP} ~10 kΩ) is superimposed.

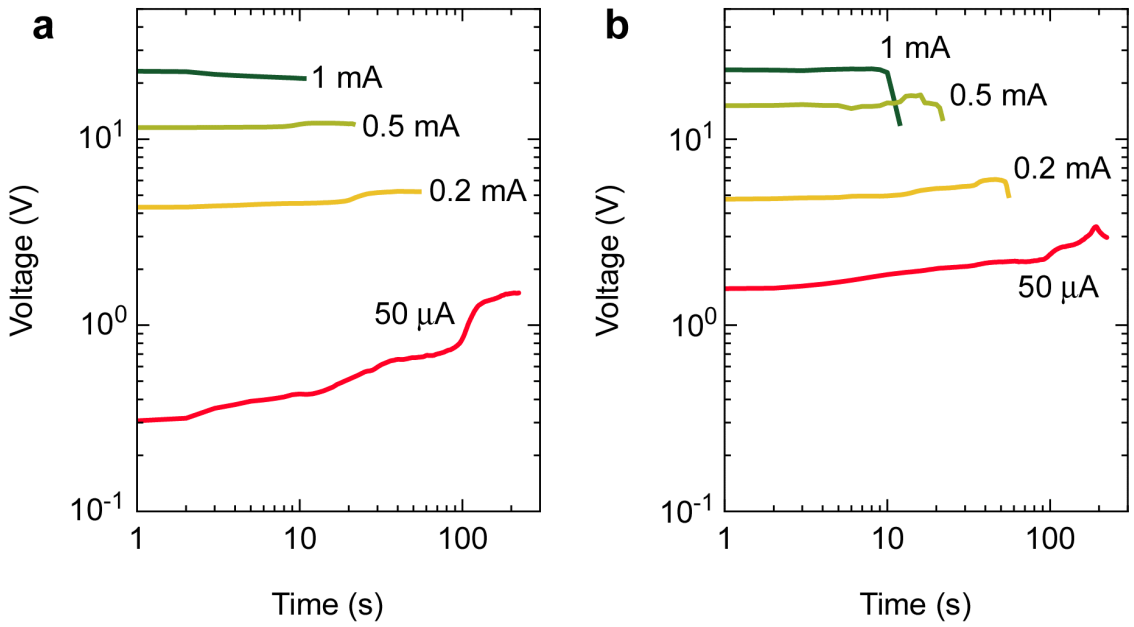
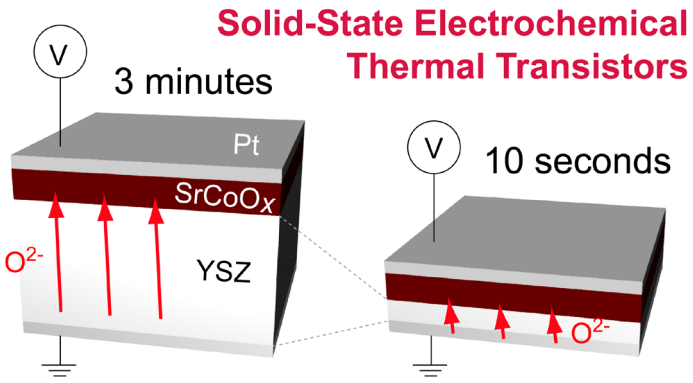


Figure 6. Changes in the voltage of the solid-state electrochemical thermal transistor with a 0.1-mm-thick YSZ substrate during electrochemical redox treatment. (a) Oxidation, (b) Reduction. Switching time is significantly reduced to ~10 seconds upon applying 1 mA current.

TOC graphic


Solid-State Electrochemical
Thermal Transistors
V
3 minutes
Pt
SrCoOx
O2-
YSZ
V
10 seconds
O2-

Supporting Information

Significant Reduction in the Switching Time of Solid-State Electrochemical Thermal Transistors

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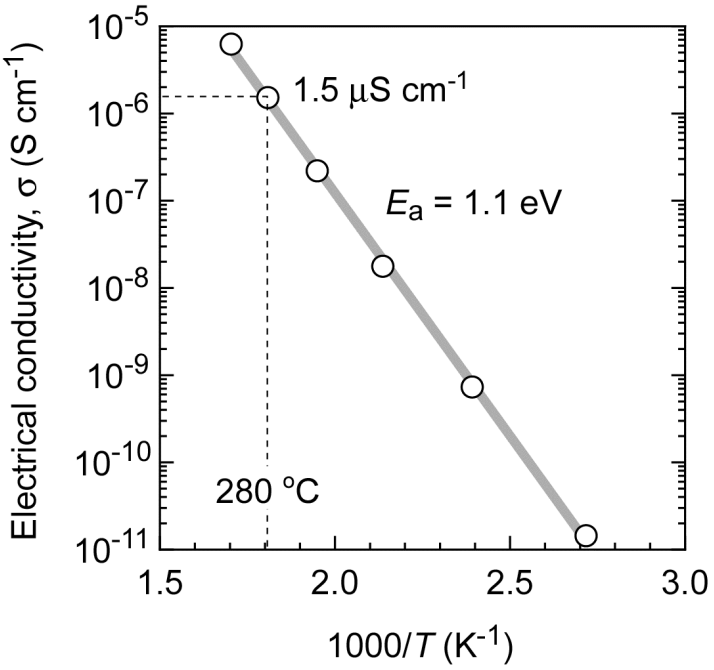

Figure S1. Arrhenius plot of the electrical conductivity of YSZ single crystal substrate (Bulk, thickness: 0.5 mm) that used in this study. The electrical conductivity at 280 °C is 1.5 μS cm^{-1}.

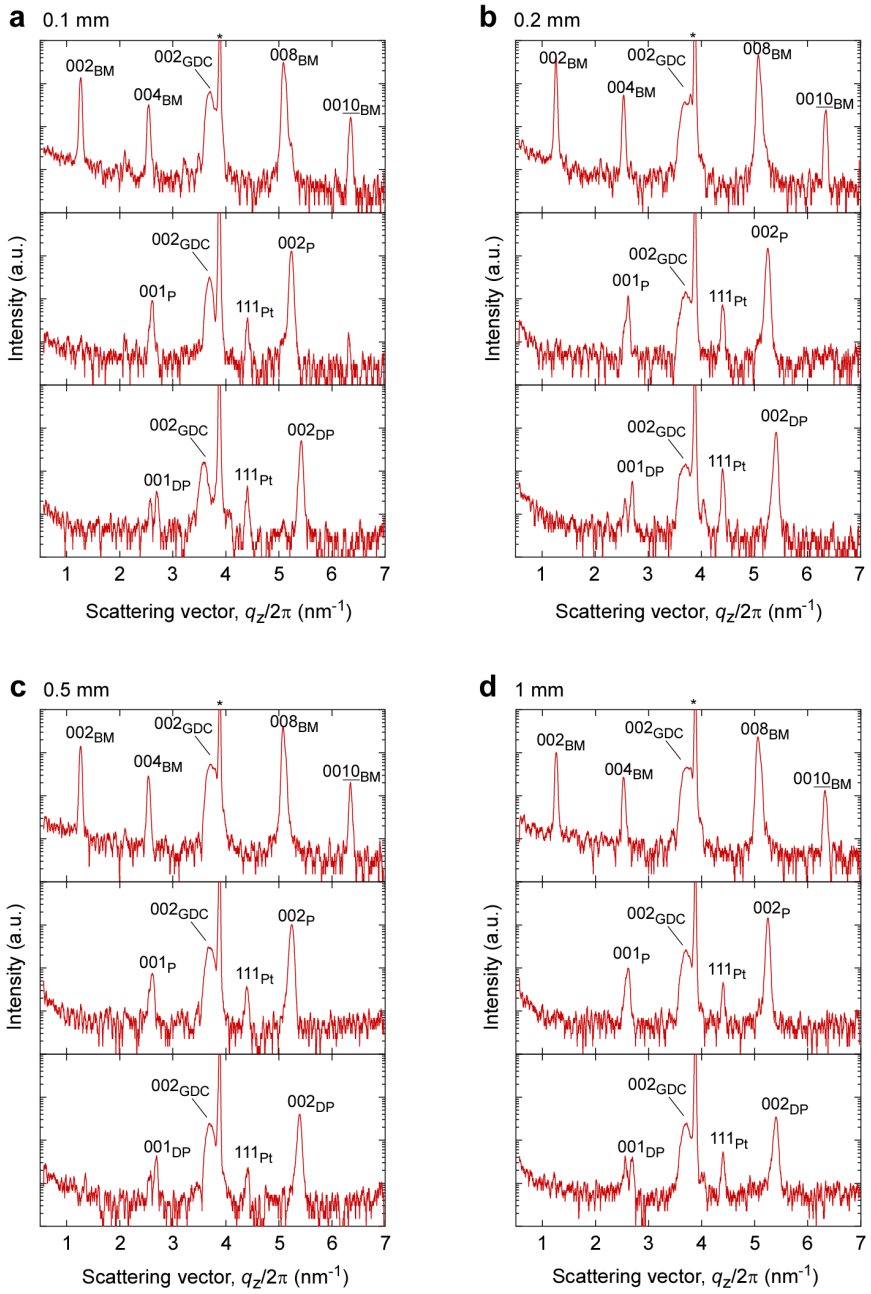

Figure S2. Changes in the out-of-plane XRD patterns of the solid-state electrochemical thermal transistors. YSZ thickness is (a) 0.1 mm, (b) 0.2 mm, (c) 0.5 mm, and (d) 1 mm. The top panel is the as-grown state, the middle panel is the oxidized state, and the bottom panel is the reduced state, respectively. BM: brownmillerite, P: perovskite, DP: defect perovskite. Regardless of the YSZ thickness, the crystal structure of $SrCoO_x$ changed between DP, BM, and P phases.

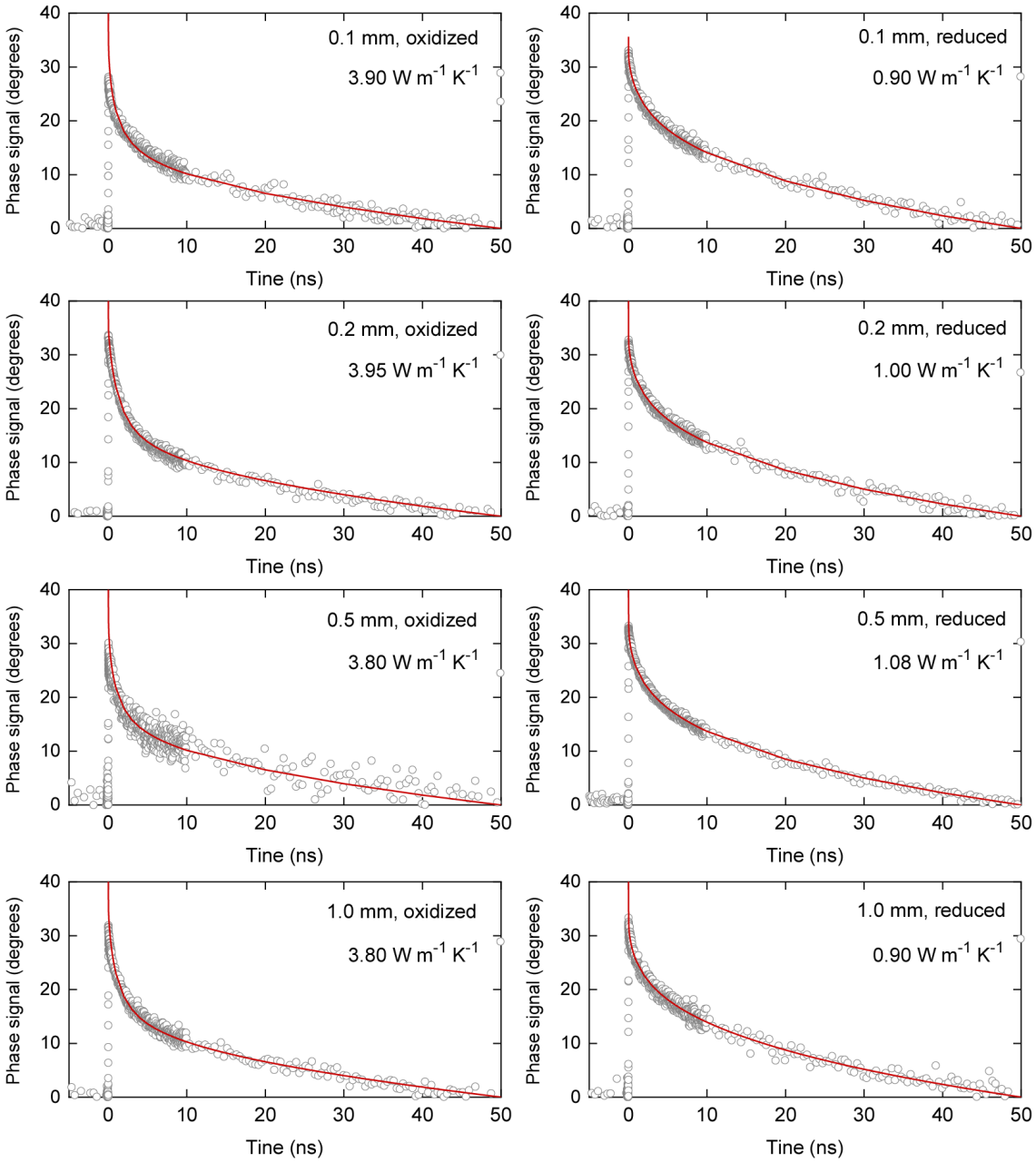

Figure S3. Decay curves of the thermoreflectance phase signal for the thermal transistors with varied YSZ thicknesses. Plots: observed data, red line: simulated curves.