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Novel Quantum Nanodevice-based Logic Circuits Utilizing Semiconductor Nanowire Networks and Hexagonal BDD Architecture

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Collaborators and Supports

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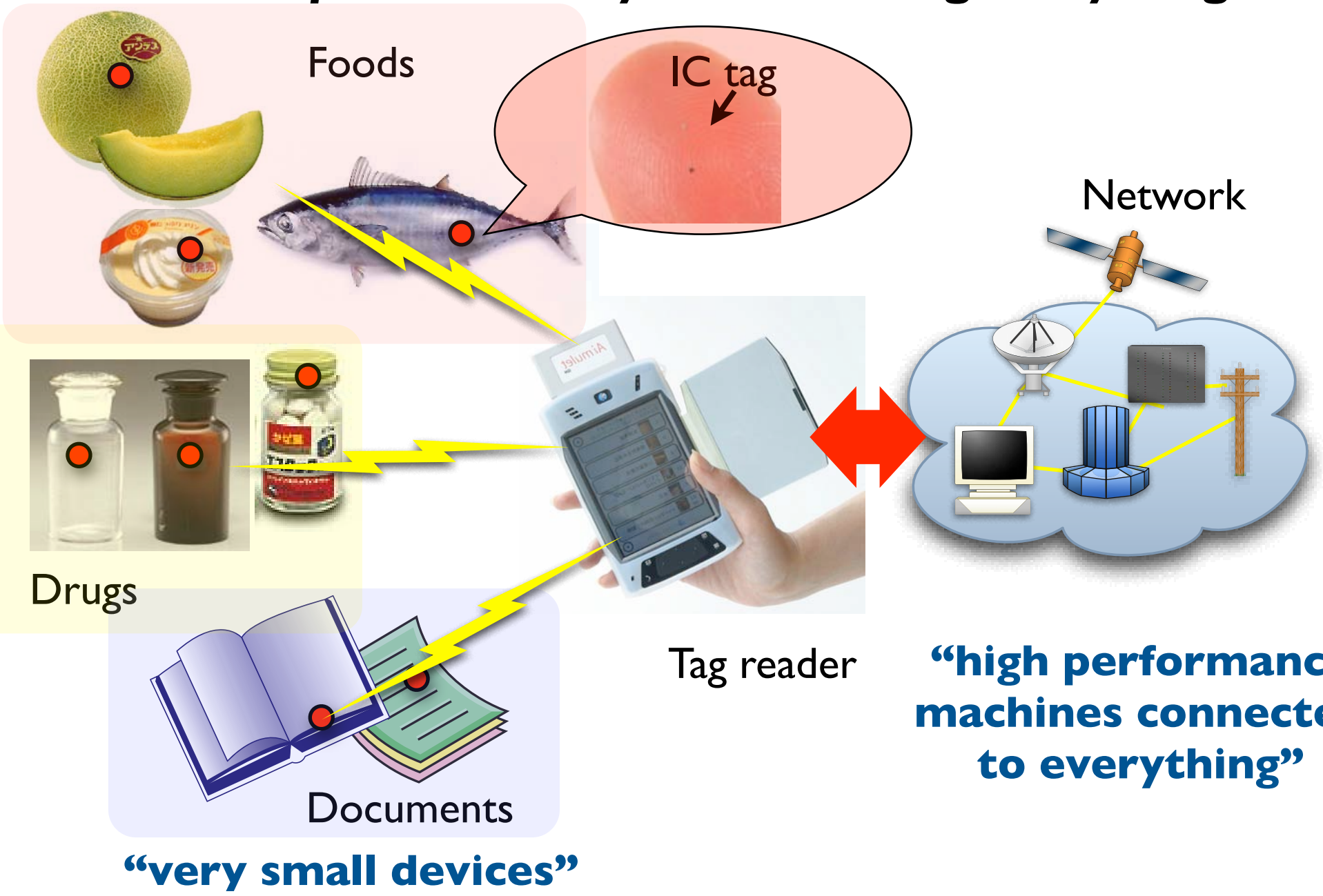
Outline

1. Introduction
2. Concept and Implementation of Hexagonal BDD Quantum Circuits
3. Devices, Elemental Circuits and Subsystems
4. Nanoprocessor
5. Summary

Introduction

Ubiquitous Society ~ Networking Everything



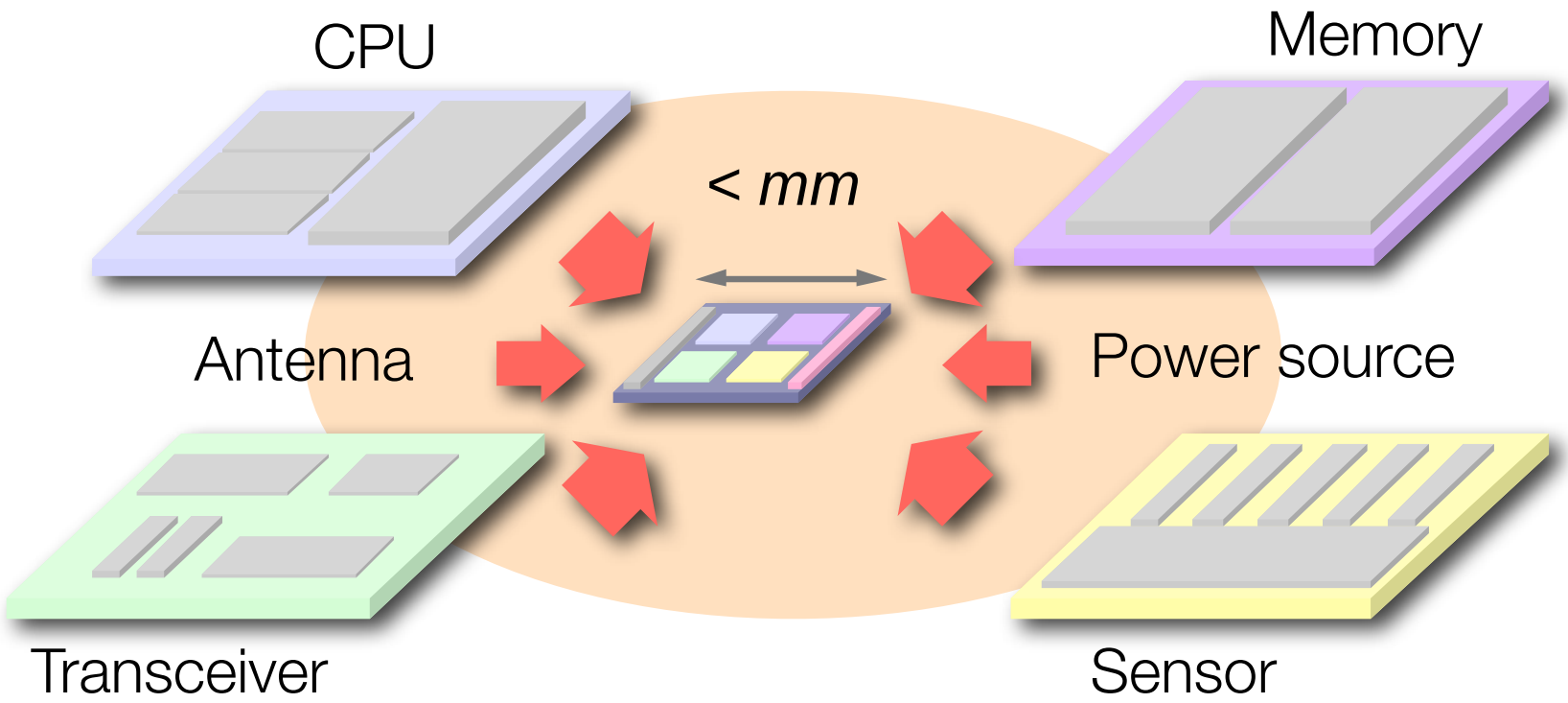
"high performance machines connected to everything"

"very small devices"

Ubiquitous Hardware for End Users/Objects

Small device : **Ultra-Small Knowledge Vehicle**

21st Century COE program, Hokkaido Univ.,
"Meme-media Technology Approach to the R&D of Next-generation ITs" from MEXT, Japan

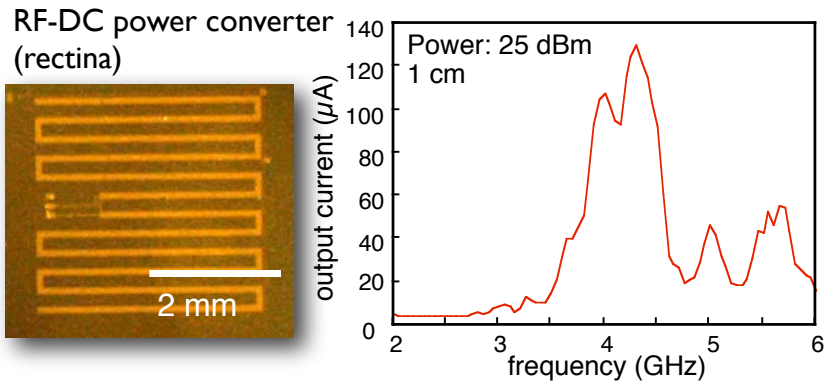


- **Extremely “Small Size” and “Low Power”**
- **More intelligent than RFID**

How Low Power?

Power source ~ mm² chip

- **Solar cell** : 100 nW Room
- **RF** : 100 μW d = 1 cm



Power consumption

- **Communication** : 10 nJ/bit by RF
- **Sensor** : 1 nJ/sample
- **CPU** : 1 nJ/instruction

http://robotics.eecs.berkeley.edu/~pister/SmartDust/in2010

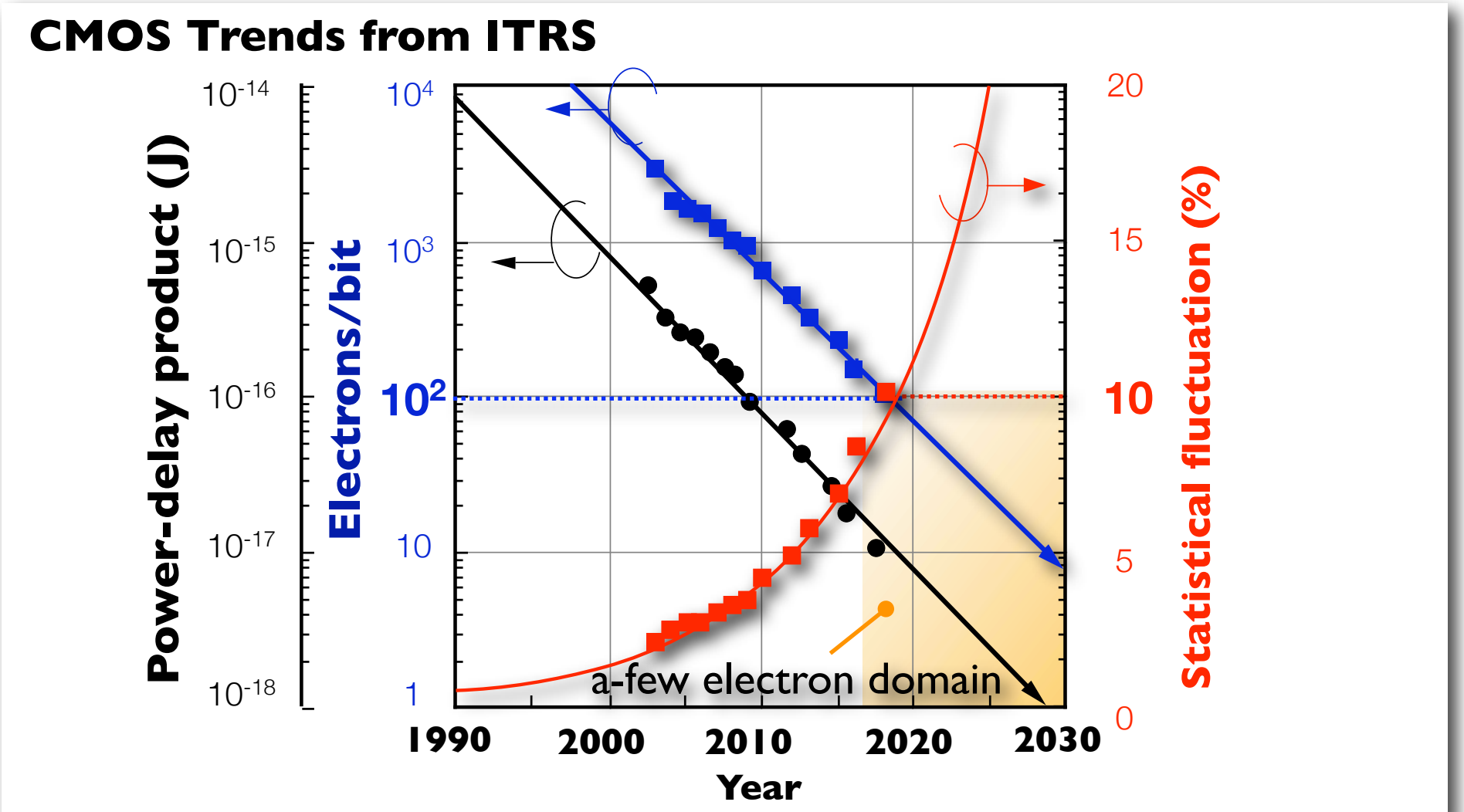
Possible tasks by RF power for 10 ms (= 1 μJ)

- 100-bit data transmission
  or
- 300 data sampling for 3 sensors
  or
- 300 data averaging

Only limited tasks

For Intelligent tasks, "Lower Power" is necessary

Out of Control, A-Few Electrons in CMOS



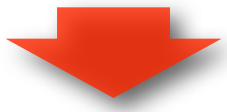
- **Reduction of power = Reducing electrons/bit**
- **Electrons < 100 causes serious bit error in CMOS**

Precise control of a-few electrons is possible by quantum nanodevices

Quantum Nanodevices

Advantage	Low power Small
Problem	Low temperature operation Poor current drivability, low gain Uniformity Integration

To keep CMOS compatible, we should **solve** problems in straight forward, but very difficult

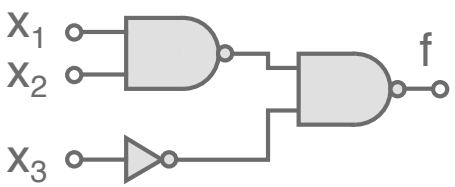


"**cover-up**" *by alternative logic architecture* = **hexagonal BDD**

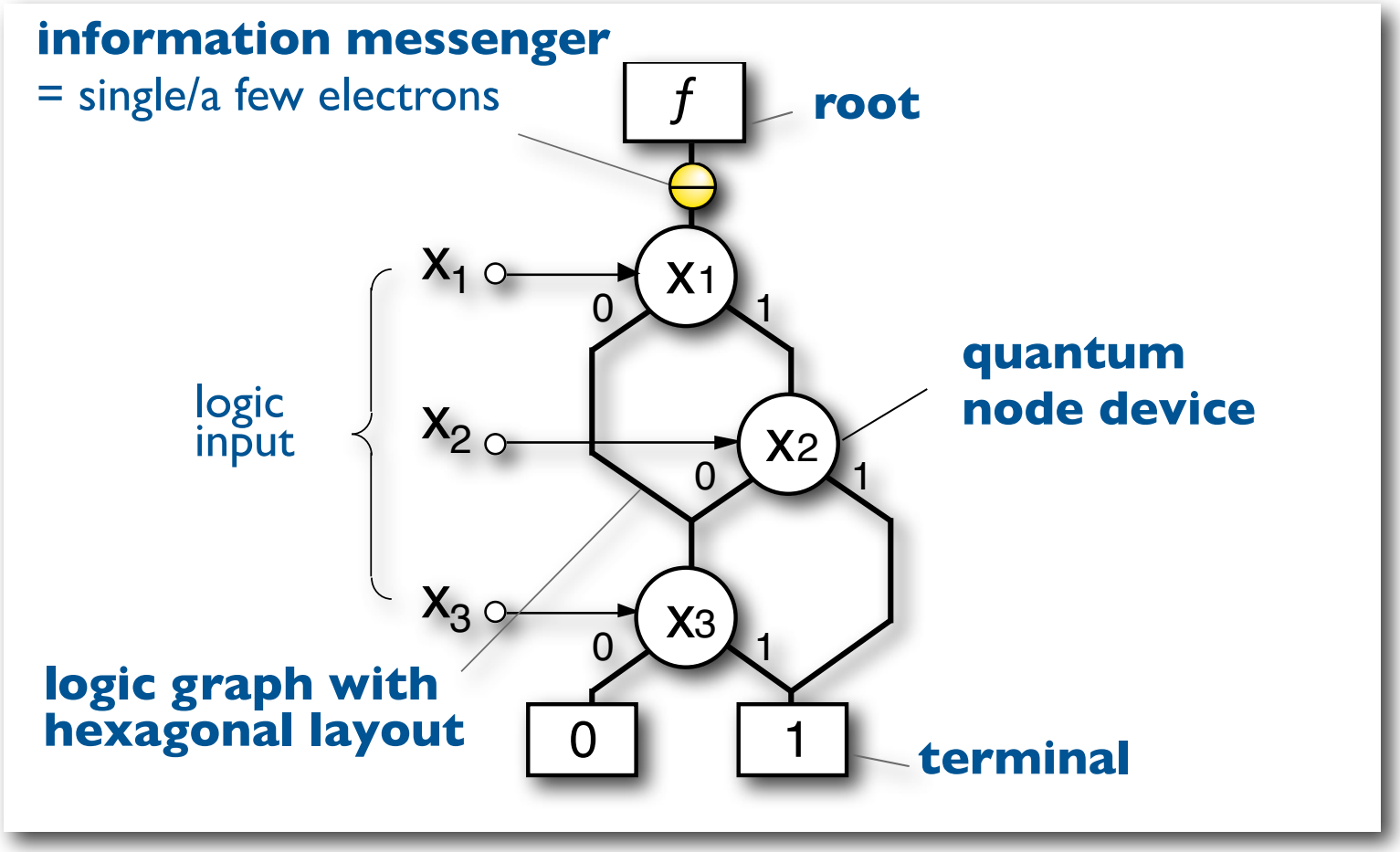
Concept of Hexagonal BDD Logic Quantum Circuits

Hexagonal Binary-Decision Diagram (BDD)

Kasai and Hasegawa, IEEE EDL, 23, 2002

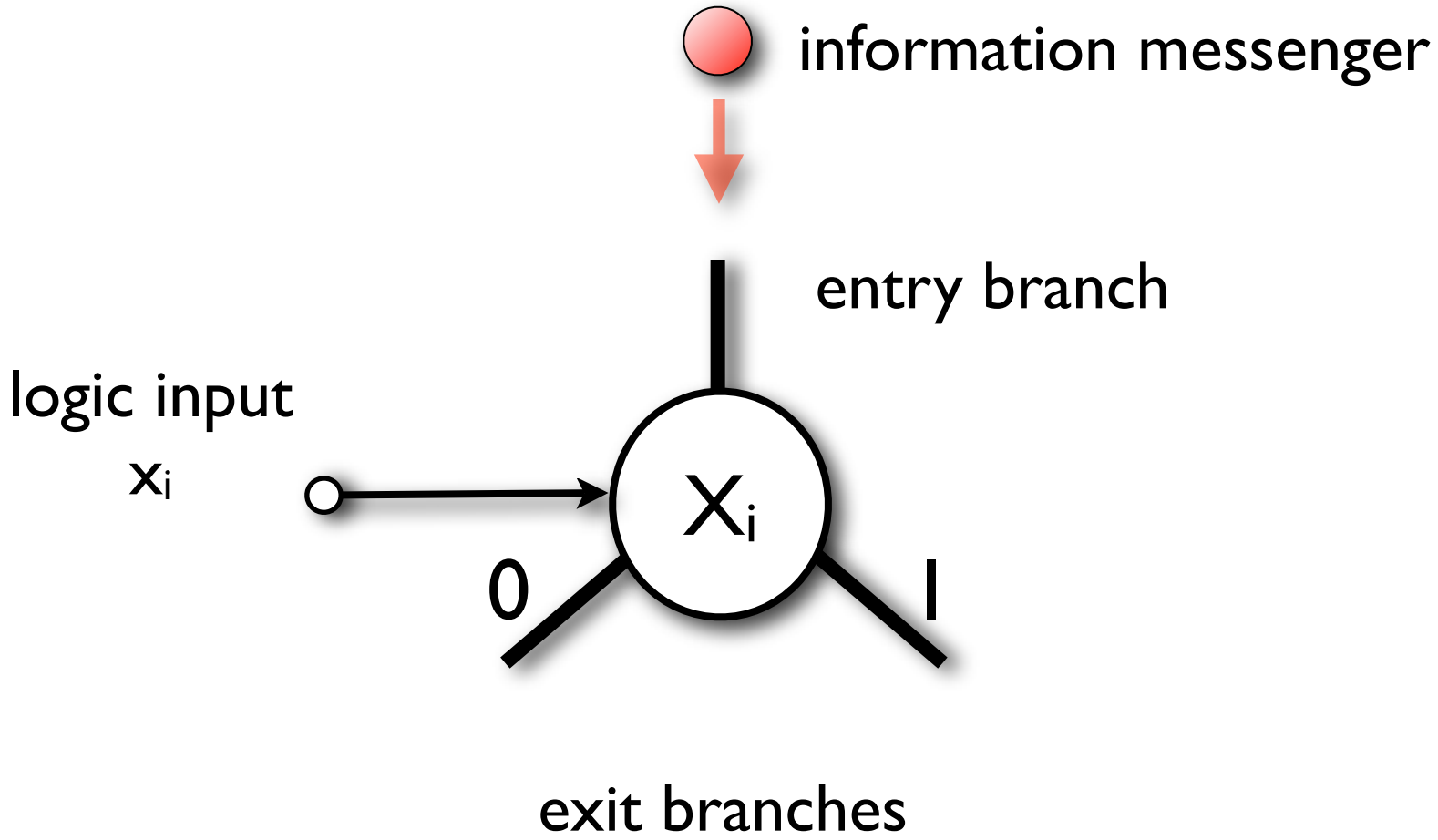


Logic gate architecture

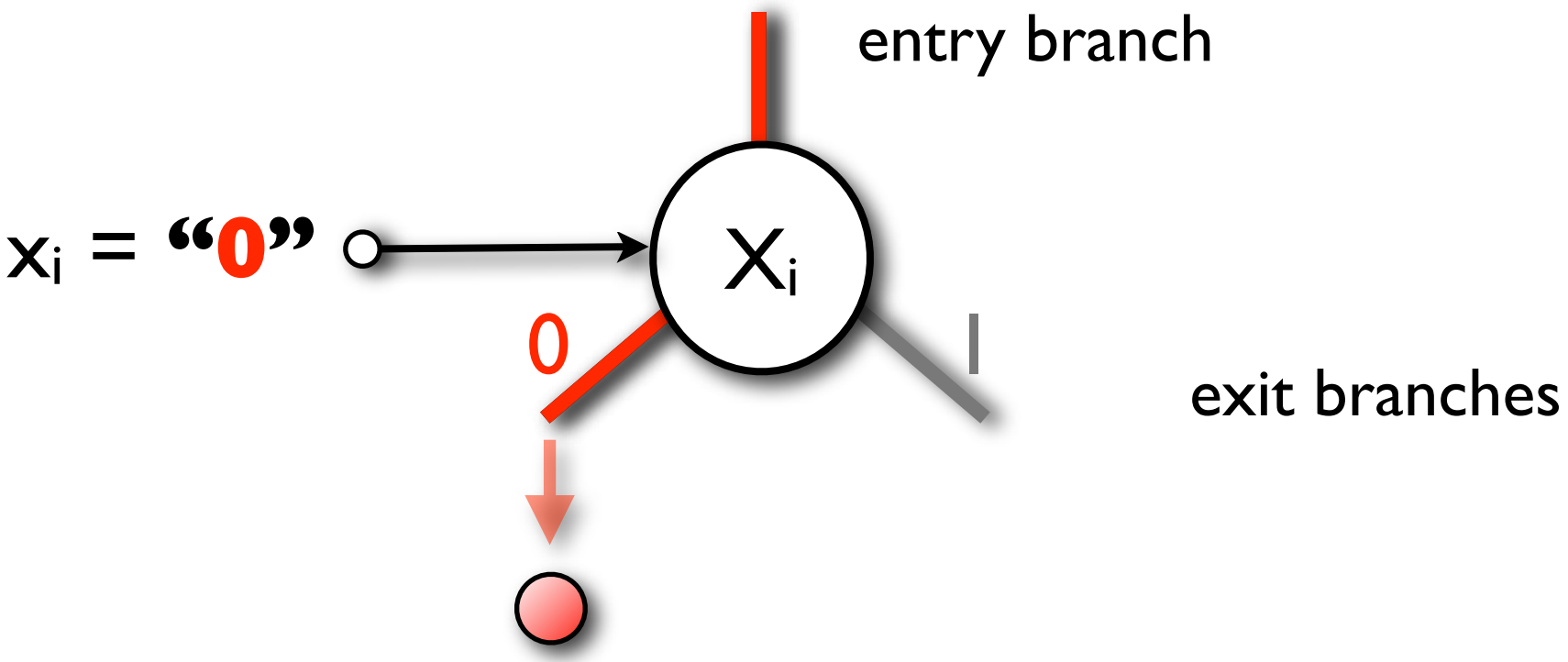


- Logic-function representation: **directed graph** with **hexagonal layout**
- Information messenger: **single or a few electrons**
- Device: **quantum node device** switching paths for messengers

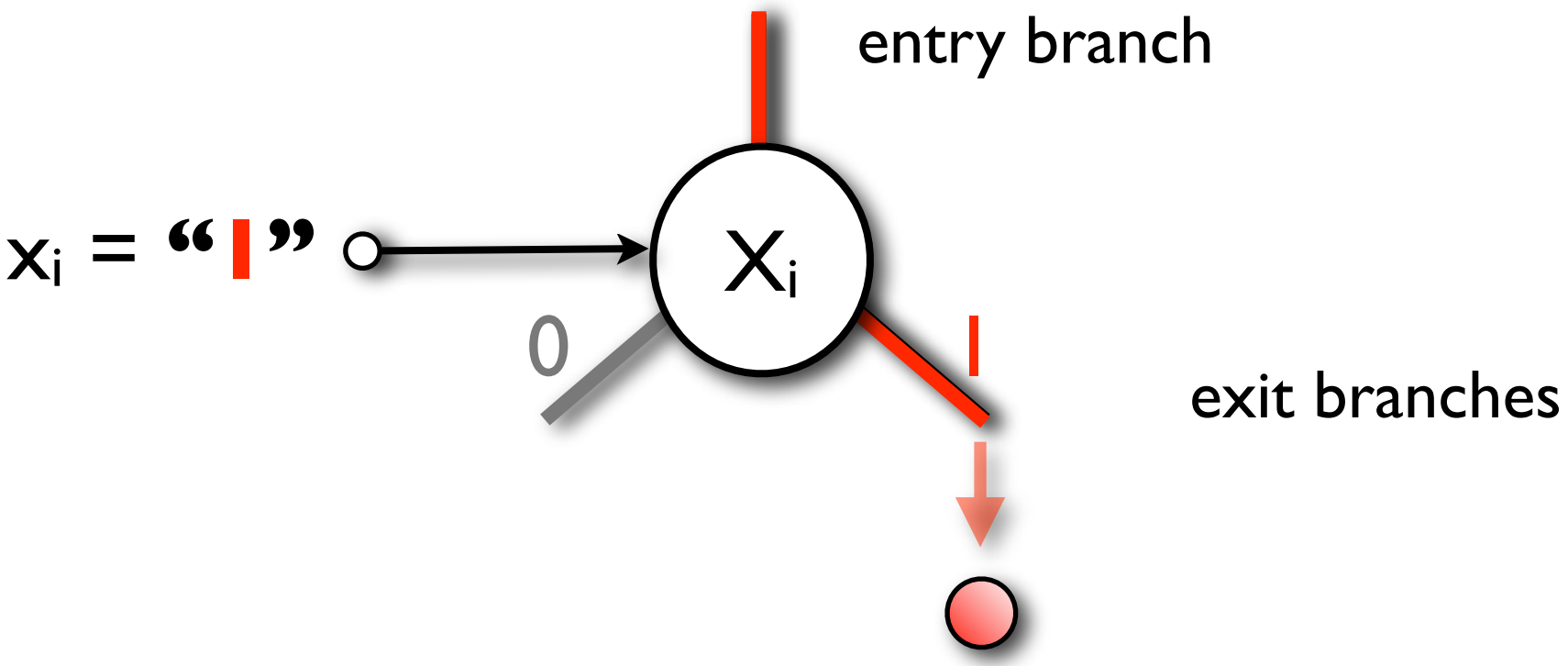
BDD Node Device



BDD Node Device

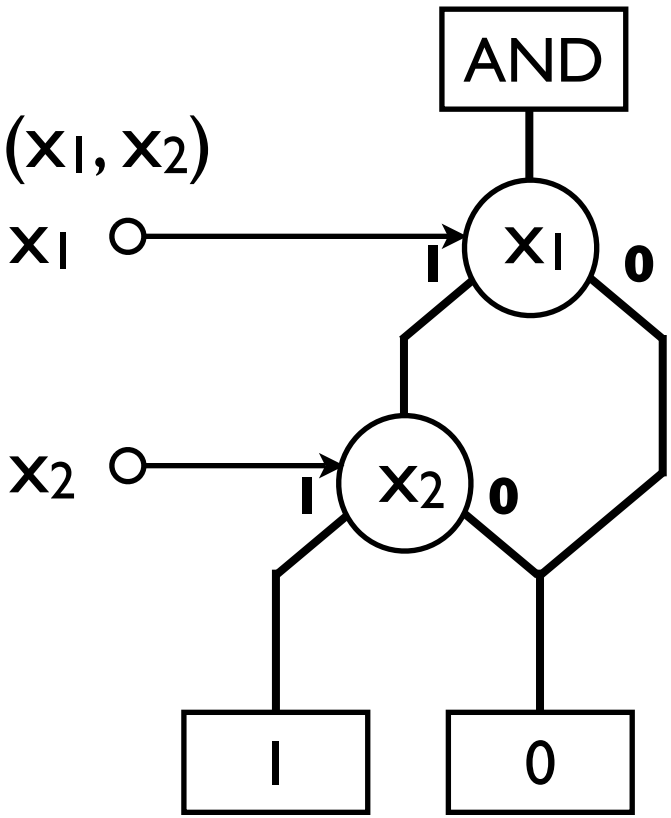


BDD Node Device



BDD Circuit Operation

ex. AND = $X_1 \bullet X_2$



x_1	x_2	AND
0	0	0
0	1	0
1	0	0
1	1	1

Main Features

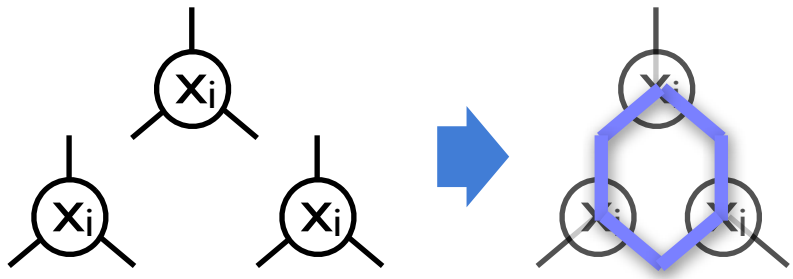
1. Ultra-low power operation

path switching function and passive transmission of messenger
don't require "transfer gain" and "current drivability"

single- or a-few-electron messengers controlled in quantum way
by ultra-low voltage results in low current and low power

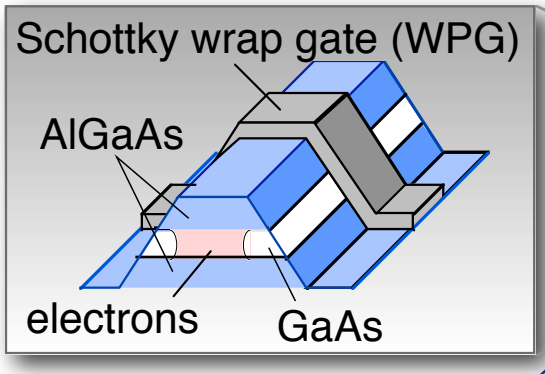
2. High-density and large-scale integration

hexagonal network realizes high-density integration of node devices
having 3-fold symmetric configuration

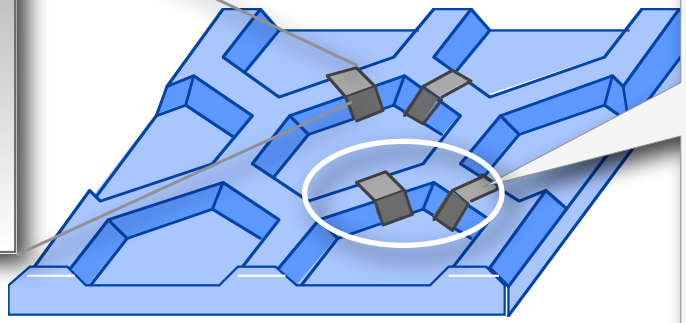


Hardware Implementation

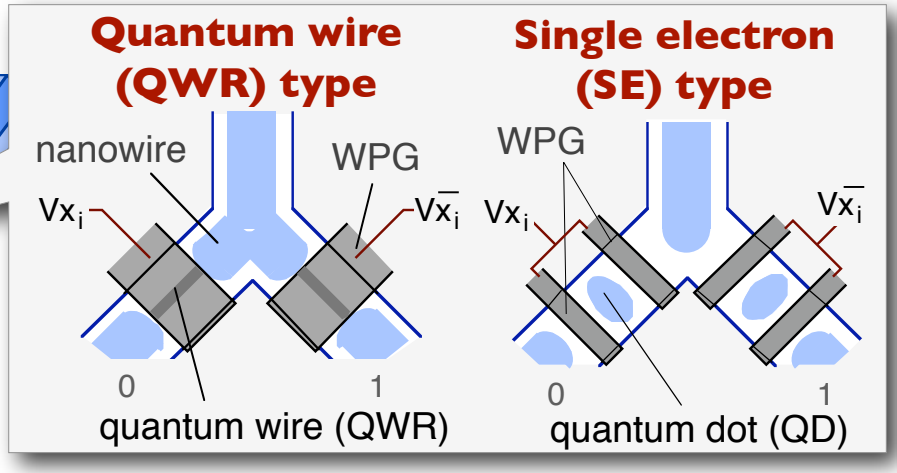
Compound Semiconductor Hexagonal Nanowire Network + Nano-scale Schottky Wrap Gate (WPG)



WPG structure



hexagonal etched nanowire network



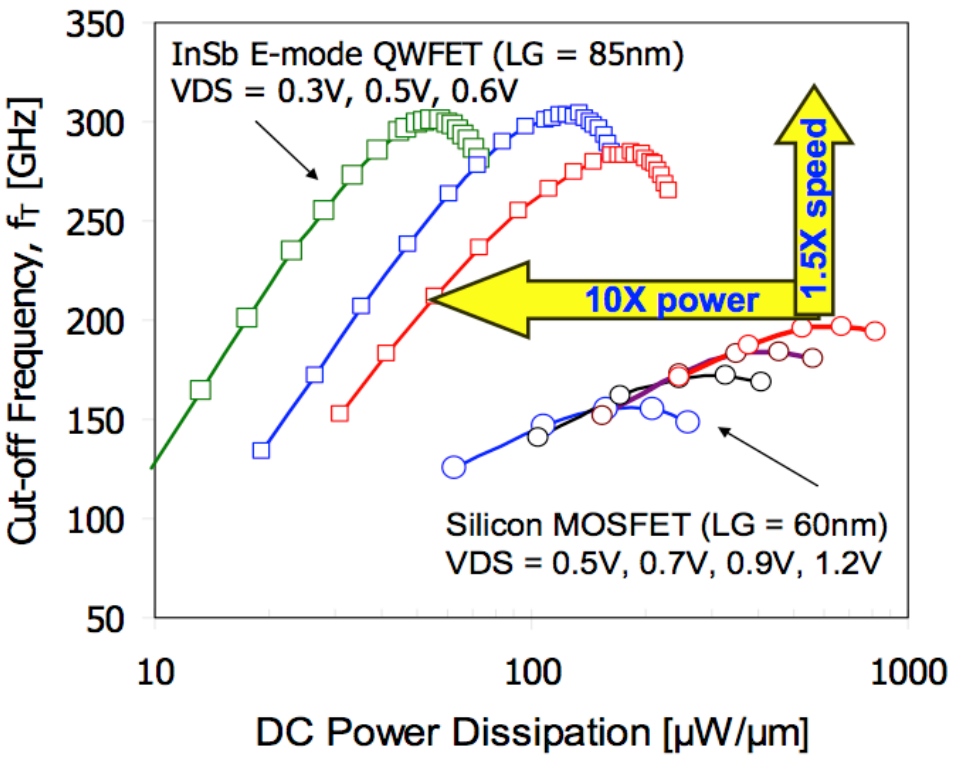
WPG quantum node devices

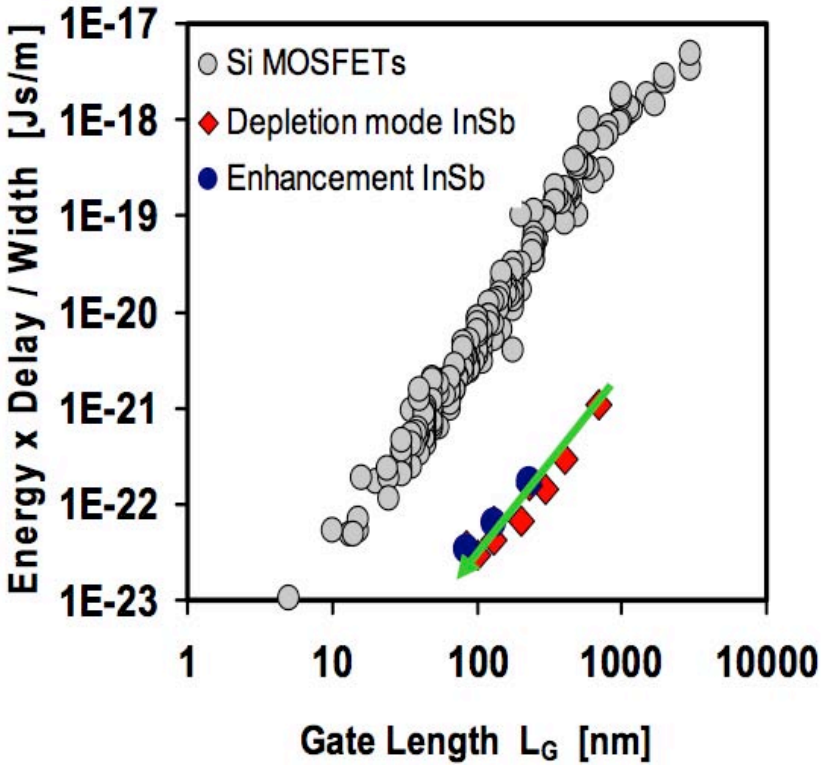
WPG structure:

- Simple planar structure: design flexibility, easy to integrate
- Tight gate control
- Operation as either "quantum nanodevices" or "normal FETs"

Compound Semiconductor Meets Hexagonal BDD

- High speed and low power
- Large quantized energy and long mean free path
- Mature nanostructure formation technology





source: Intel, IDF 2006

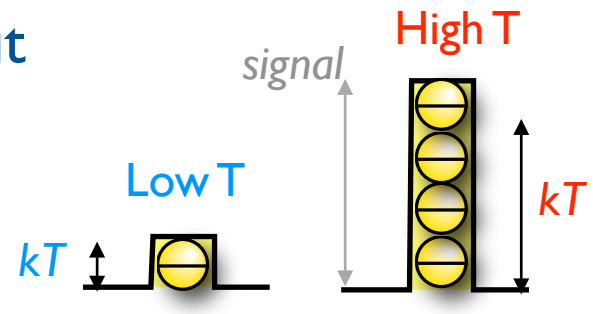
Main Features

1. Ultra-low power operation

2. Large-scale and high-density integration

3. Correct operation even at RT

WPG can control not only a-few-electrons but many electrons by trade-off with power

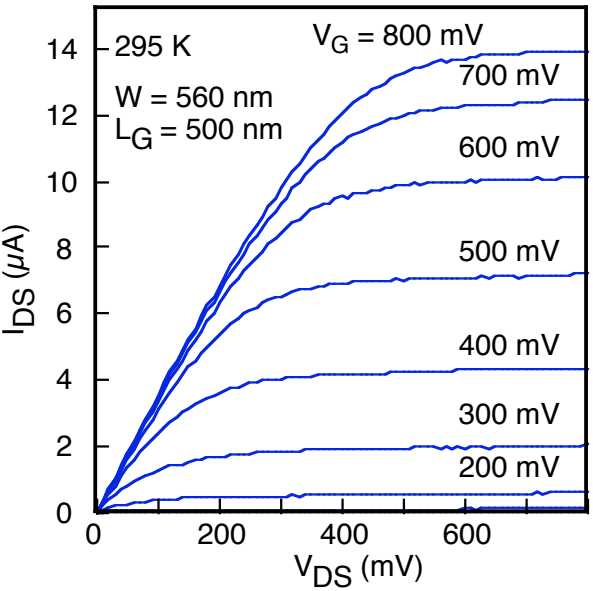


4. V_{th} fluctuation cover-up

cover-up by adjustment of input logic swing

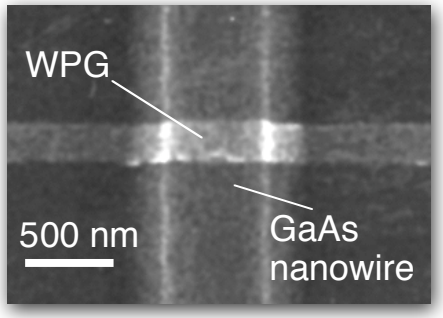
WPG-based Quantum Node Devices

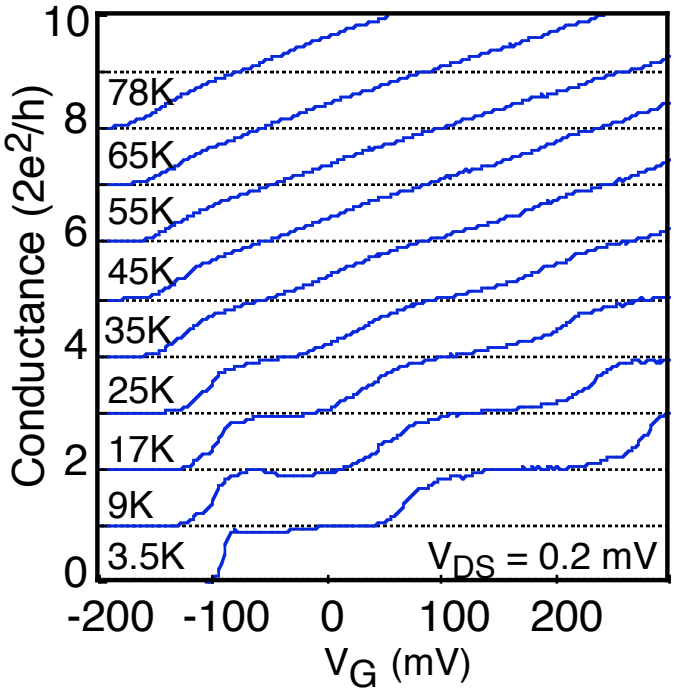
WPG device



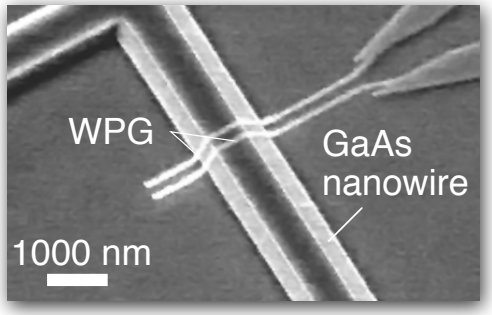
g_m = 60 mS/mm @ RT
230 mS/mm @ 80K

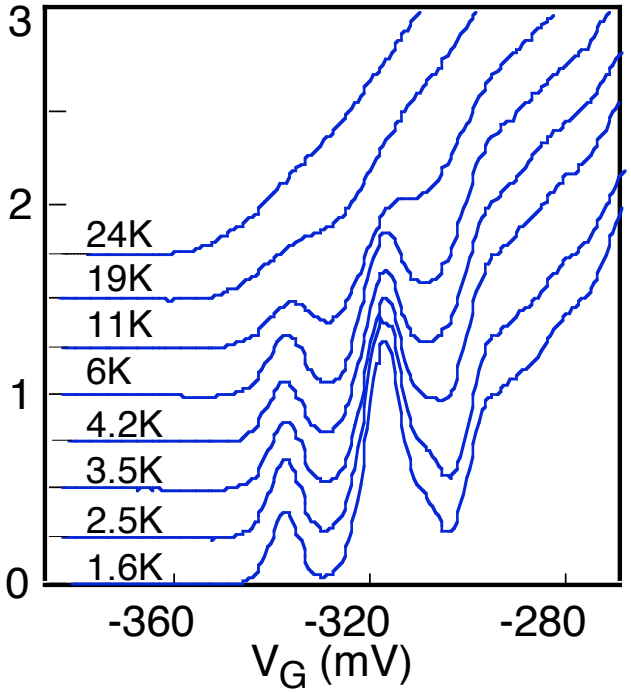
QWR device





Single electron device

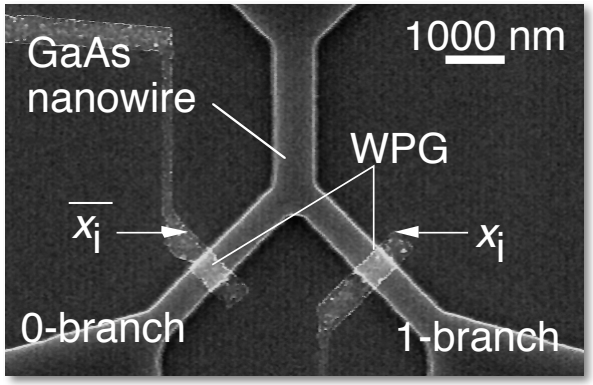


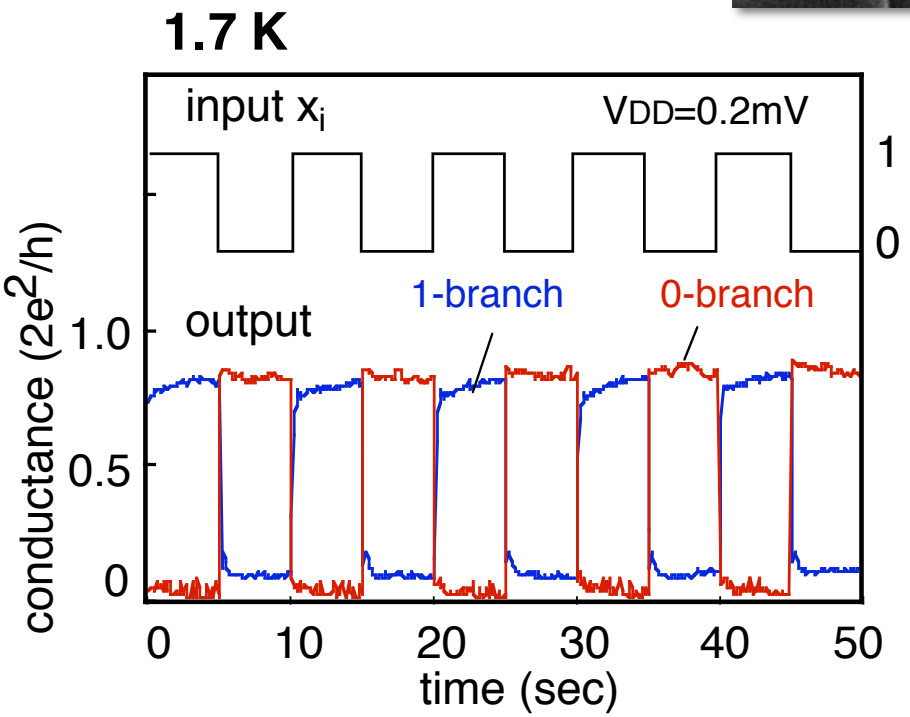


- **Fabricated devices can operate as QWR and SE devices**
  successfully control single or a-few-electrons

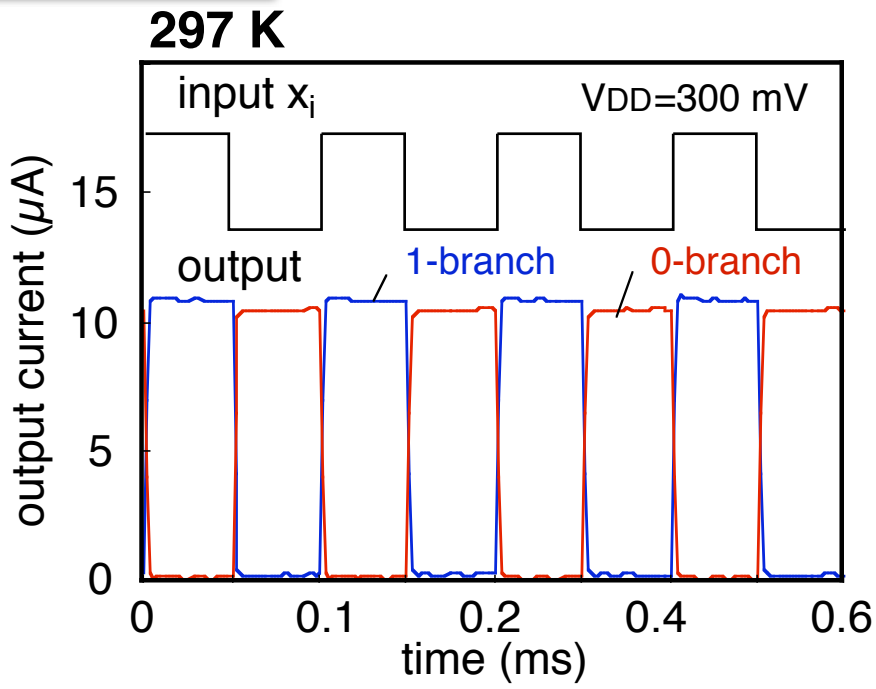
Path Switching Operation

QWR type node device





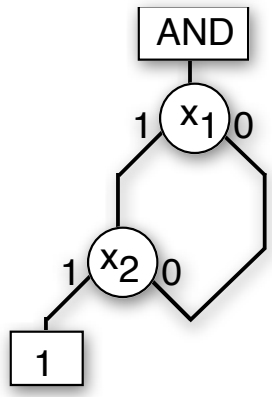
Path switching using quantized conductance



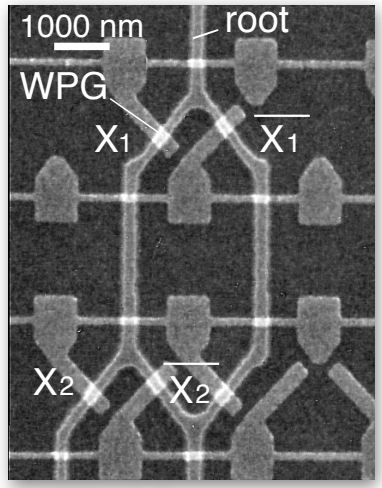
Path switching of many electrons in classical way

Logic Circuits

AND logic

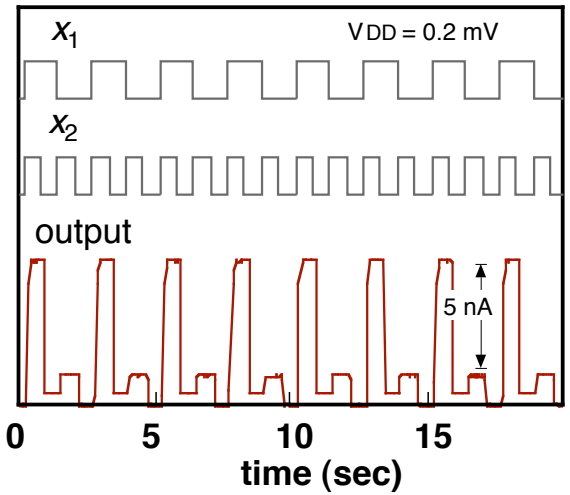


QWR-type

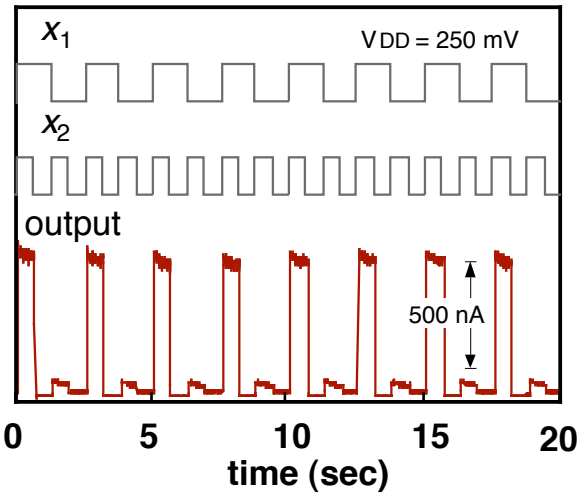


Logic operation

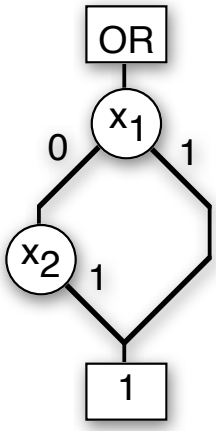
quantum regime (1.6 K)



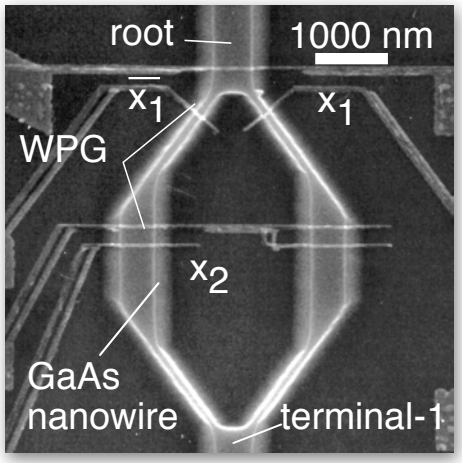
classical regime (300 K)



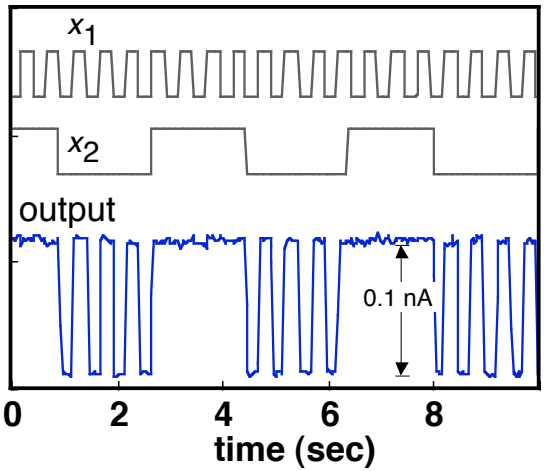
OR logic



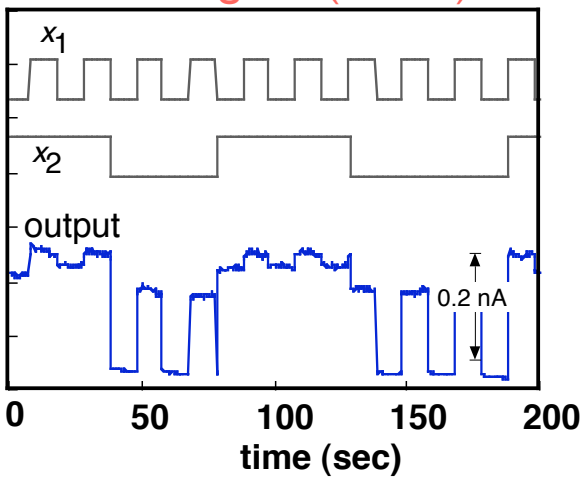
SE-type



quantum regime (1.6 K)

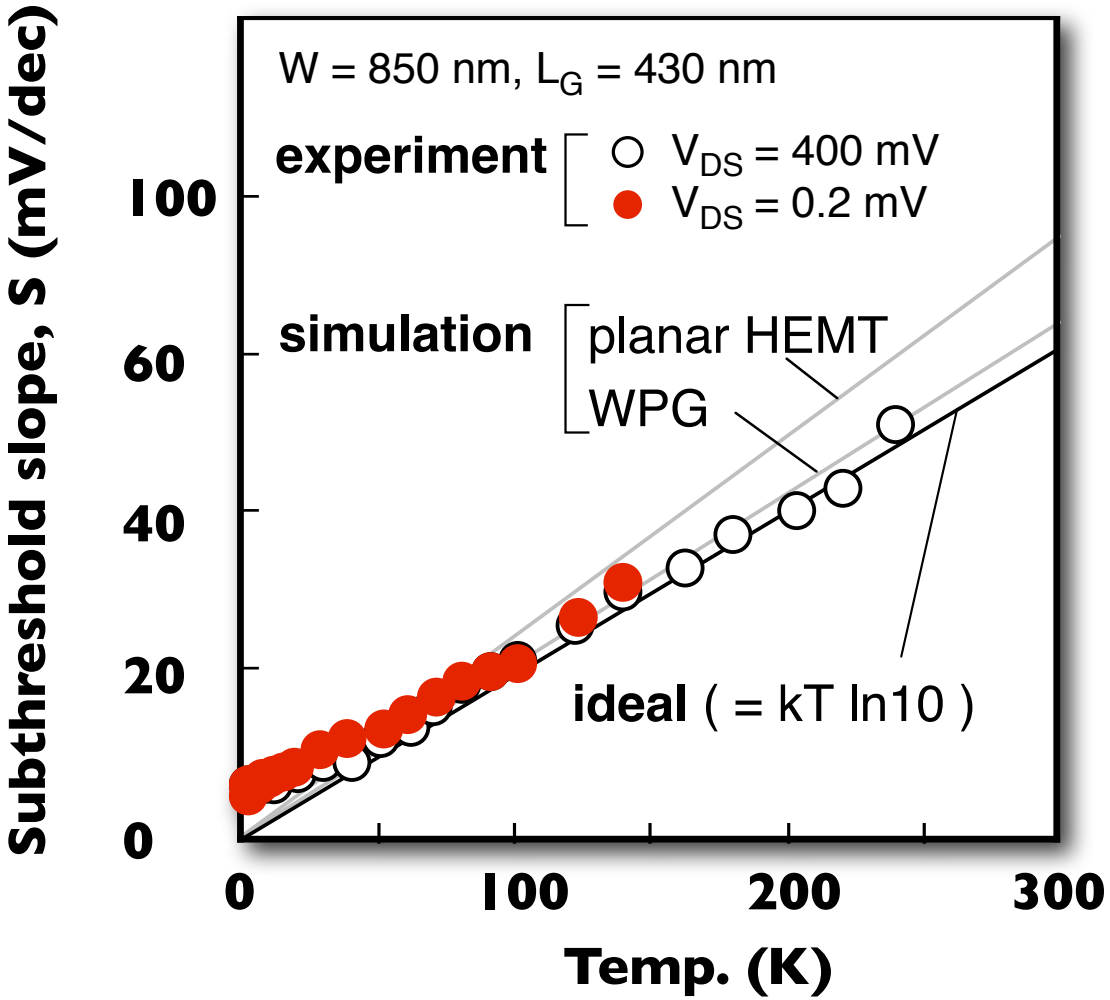


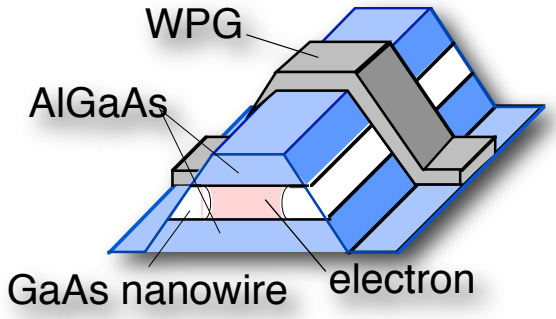
classical regime (120 K)



- **WPG BDD circuits can operate from LT to RT, changing transport mode**

Subthreshold Characteristics in WPG Devices

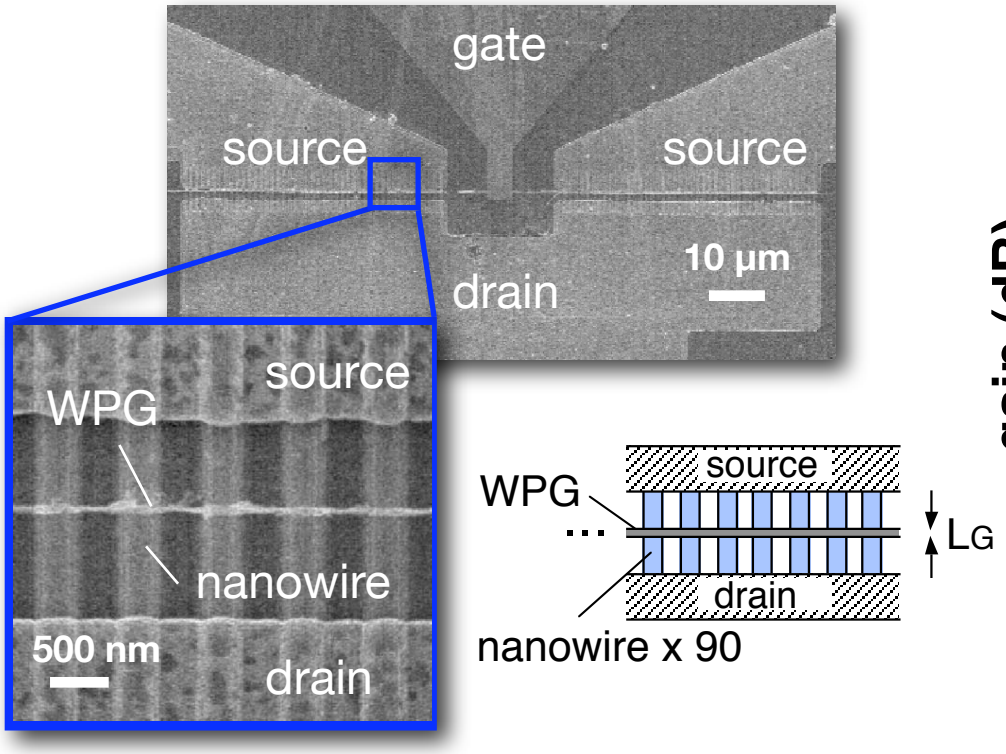


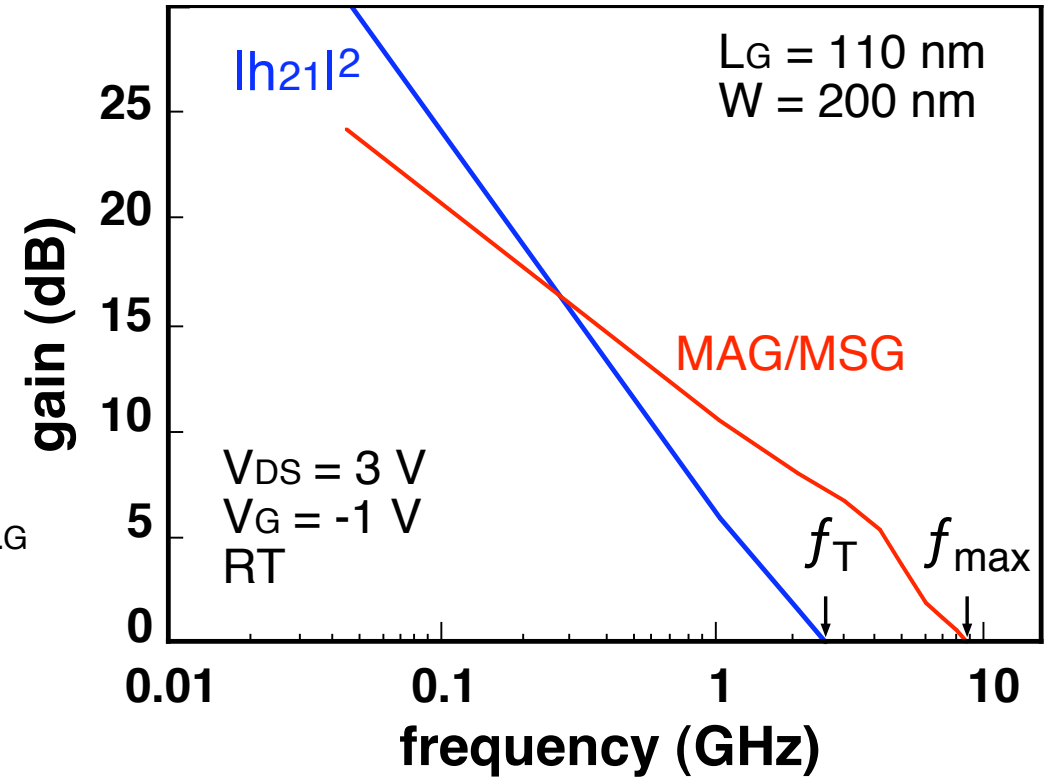


$$S = \frac{1}{\left.\frac{\partial \ln(I)}{\partial V_G}\right|_{max}} = \frac{kT}{\alpha} \ln(10)$$

- **Subthreshold slope is ideal in both quantum and classical domains**
- **Power-Temp. trade-off :** PDP ~ C {kT/e ln(10)}^{2} ~ T^2

High Speed Performance of WPG Devices

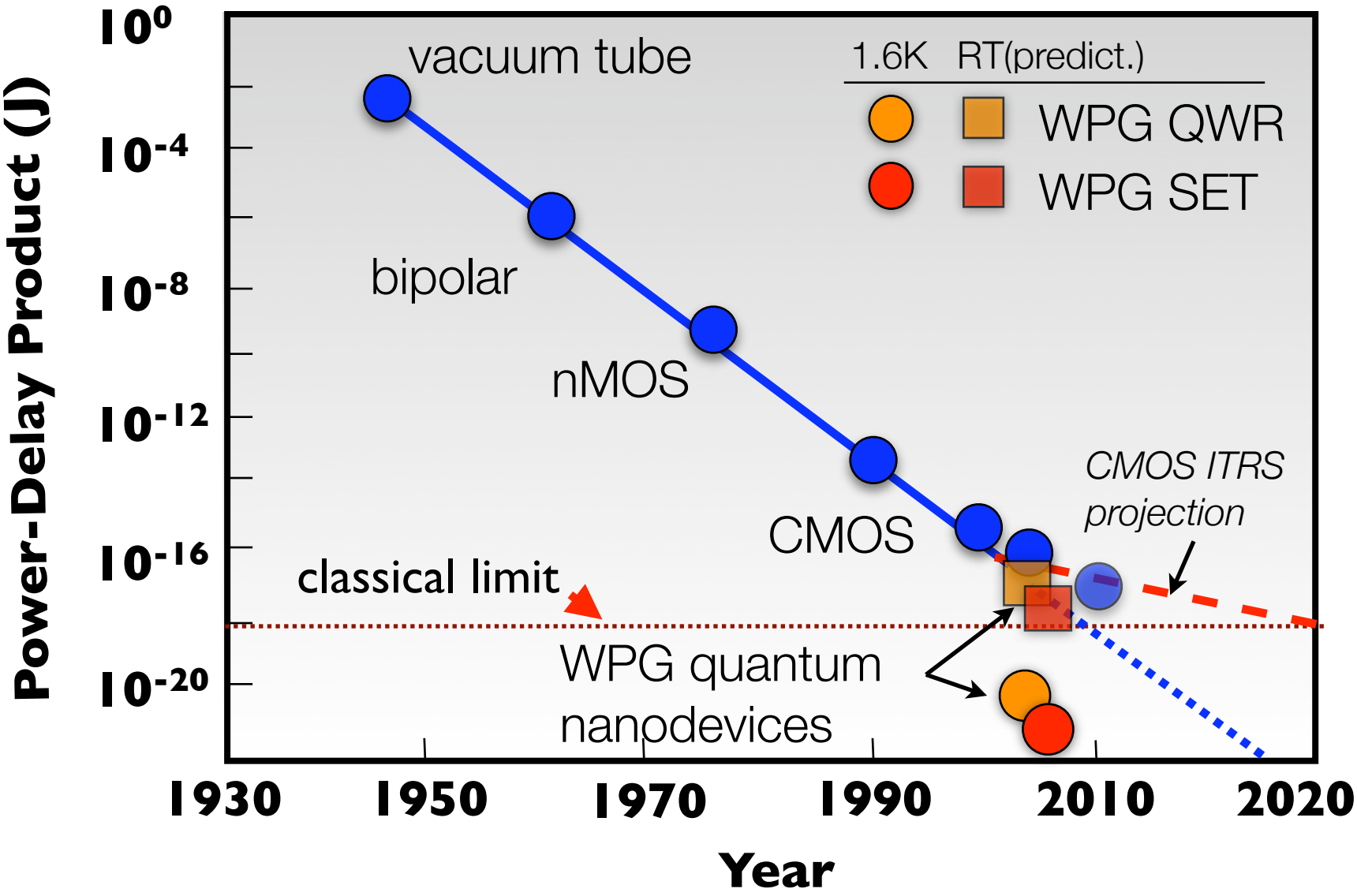




Gate Length, L_G	f_T	f_{max}
630 nm	1 GHz	5 GHz
110 nm	2.5 GHz	9 GHz

- **Confirmation of GHz switching capability**

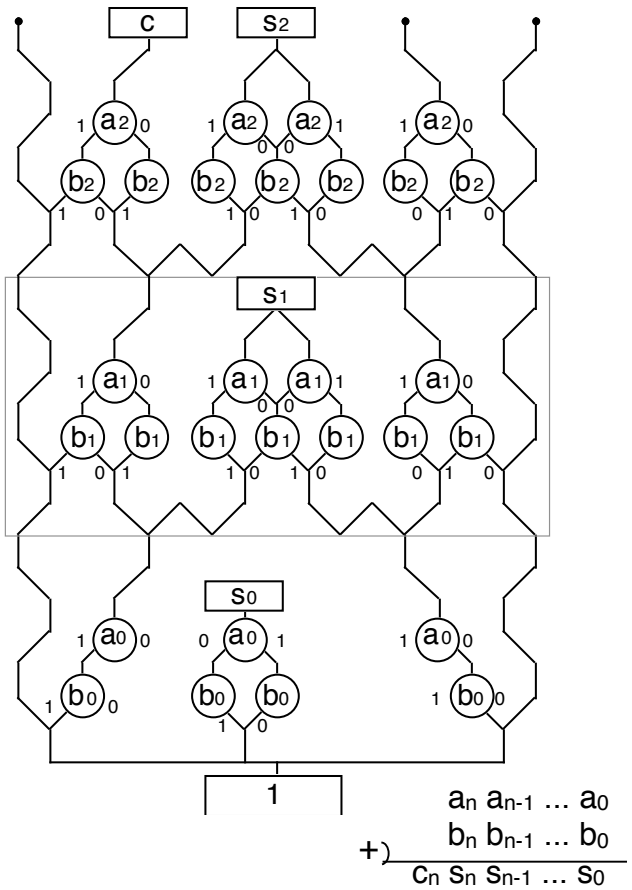
PDP Scaling



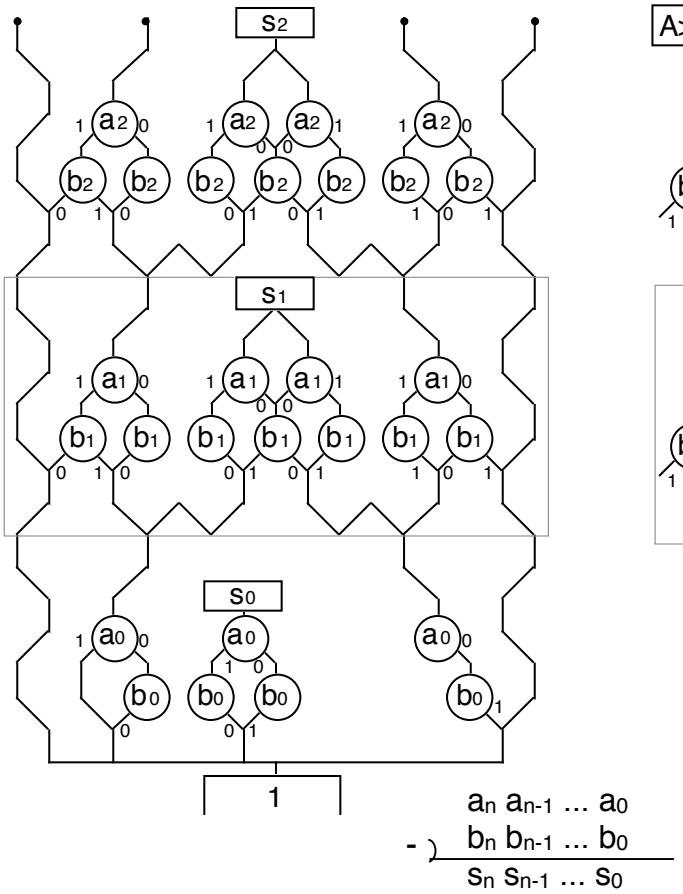
- **WPG quantum nanodevice can keep PDP scaling**

Design of Hexagonal BDD-based Subsystems

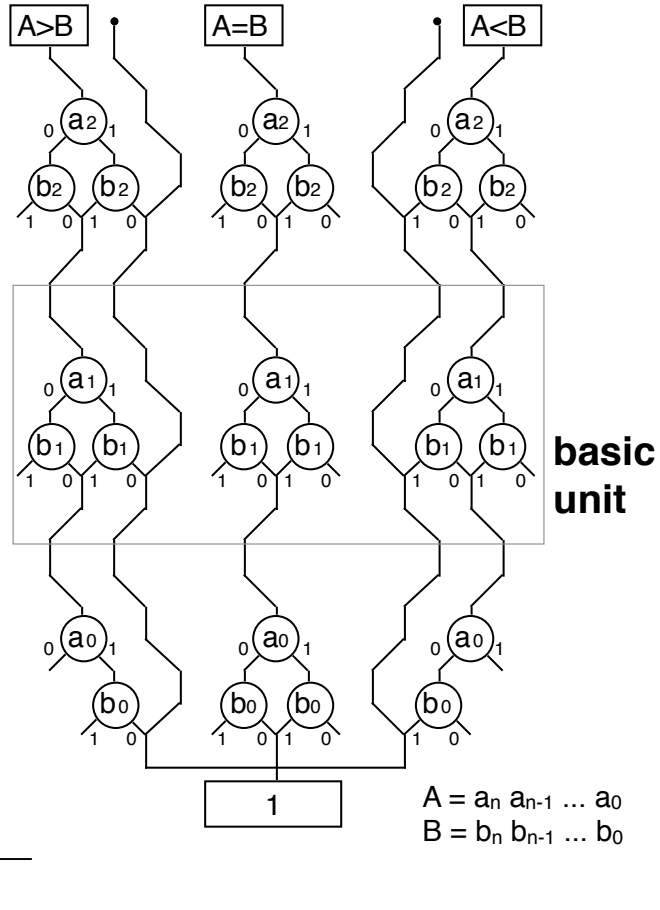
Adder



Substractor



Comparator



- **Any combinational circuits can be designed**

  Representation by principal disjunctive canonical form + Omitting terminal-0

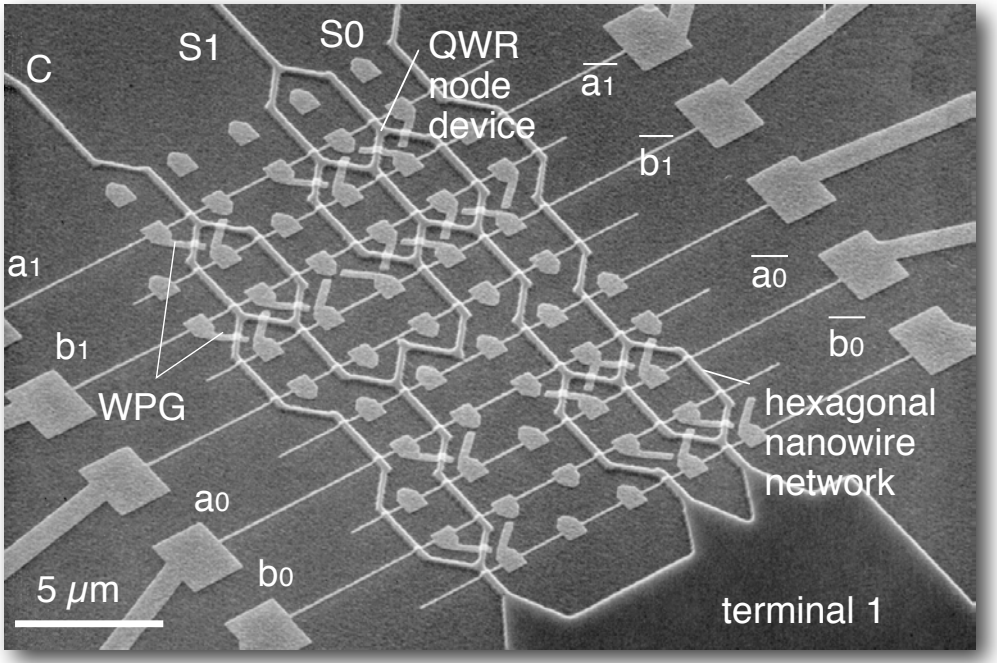
- **Smaller device count than that in CMOS logic**

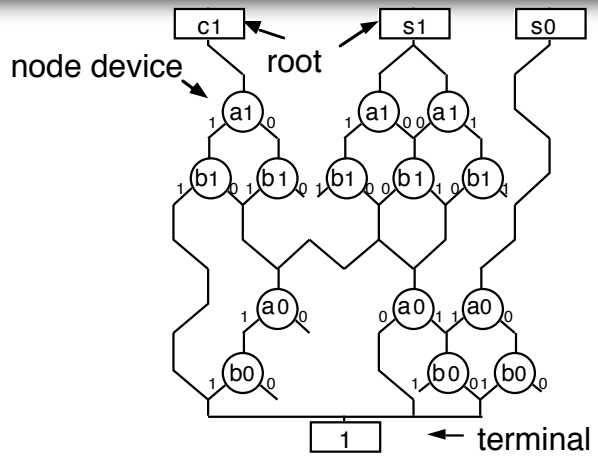
  *Ex. full adder unit Hexagonal BDD : **11** devices*

  *CMOS logic gate : **24** Trs*

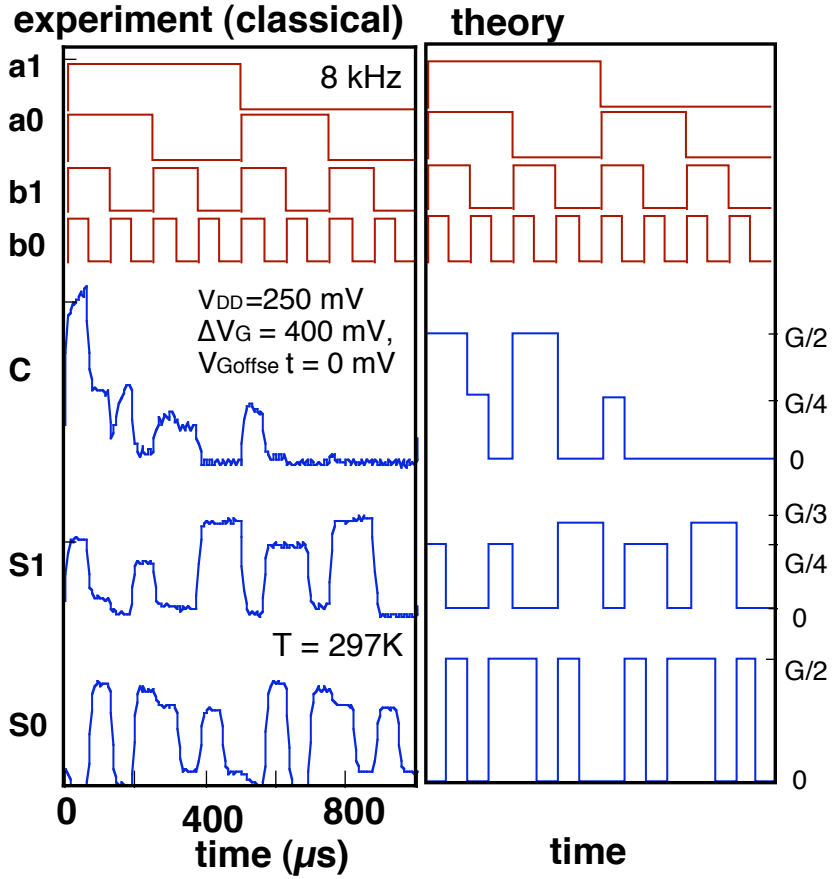
Fabrication and Characterization of Subsystems

QWR-type 2-bit adder





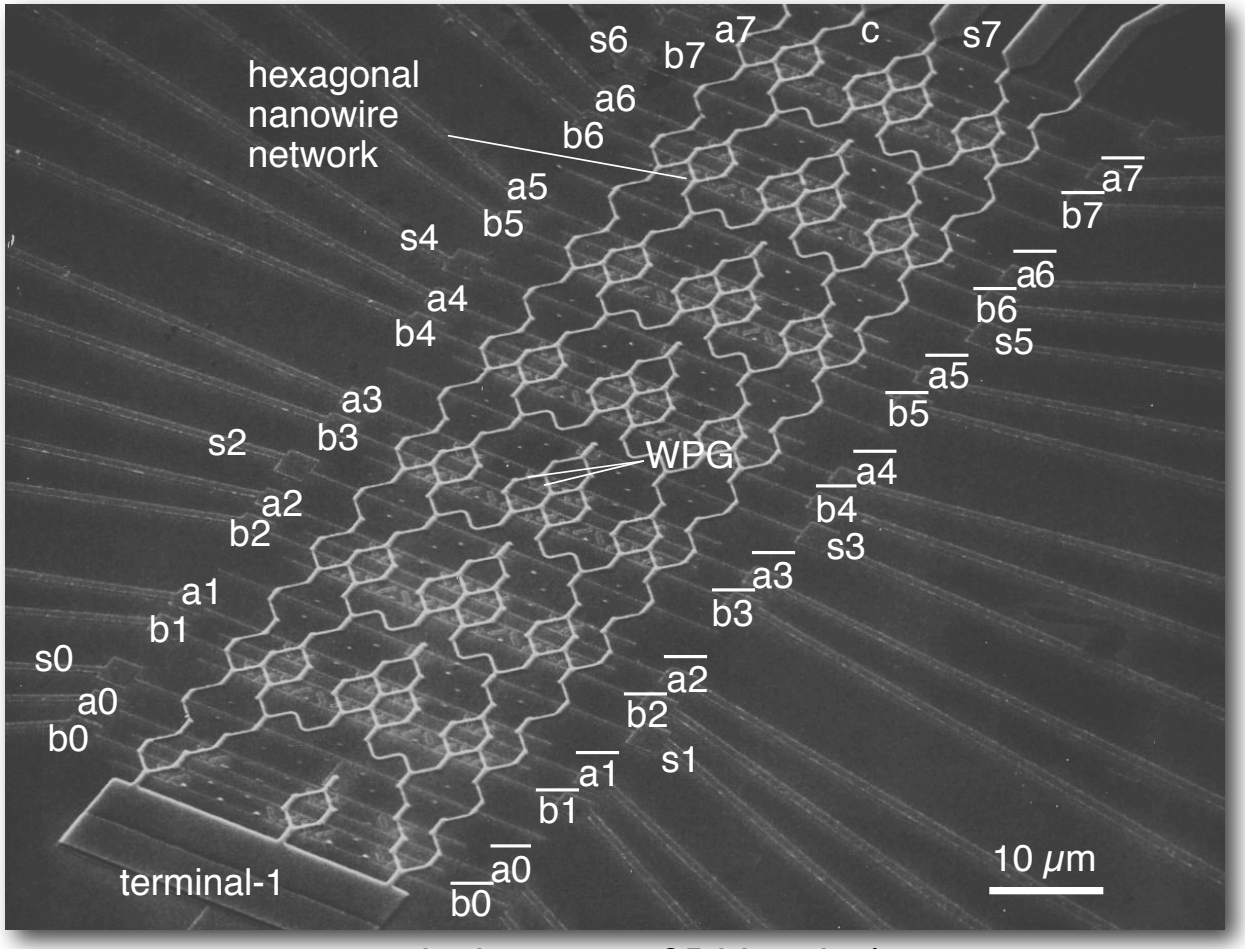
BDD 2-bit adder input-output waveforms

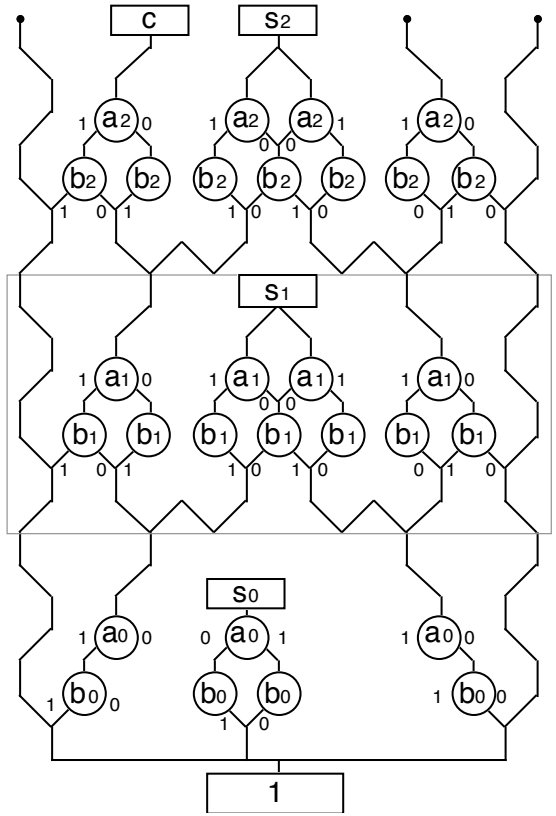


- **Fabricated 2-bit adder operated correctly at RT**
- **Fab. process for 45 M devices/cm^2 using etched nanowire is available**

Large-Scale Integration

QWR-type 8-bit adder





x 6

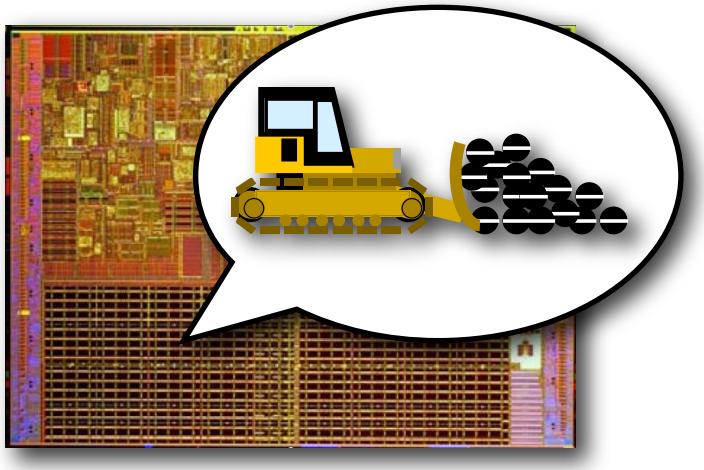
node density:	25 M nodes/cm2
circuit area:	74 μm x 19 μm
device counts:	84

- **Large number of devices can be integrated without nanowire crossover**
  84 QWR-based node devices could be integrated

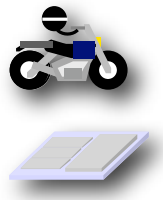
Nanoprocessor

- Feature: **"1/1000 x size and power consumption of MPU"**
- Target: core of ultra-small and ultra-low power digital systems for next-generation ubiquitous IT

But low power and small size are not compatible in CMOS



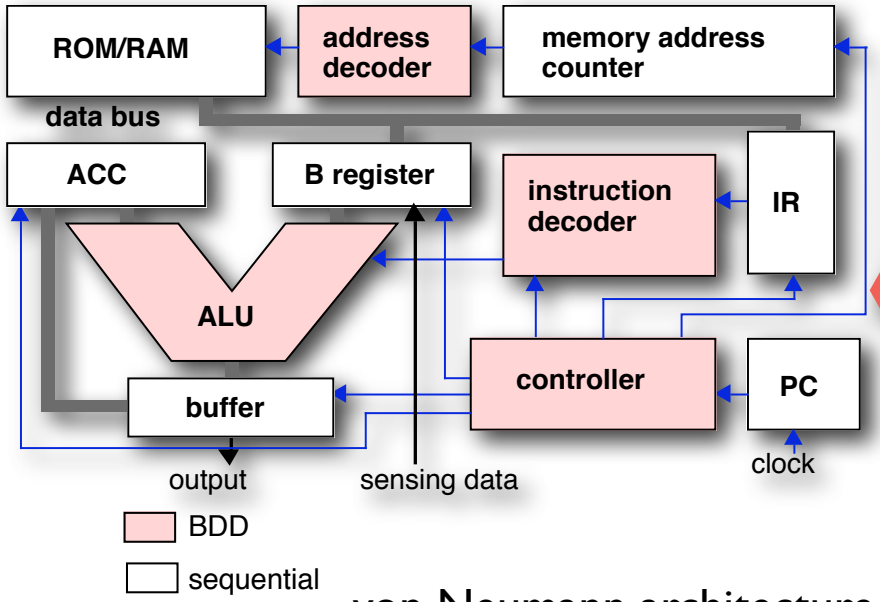
hexagonal BDD



NPU Implementation

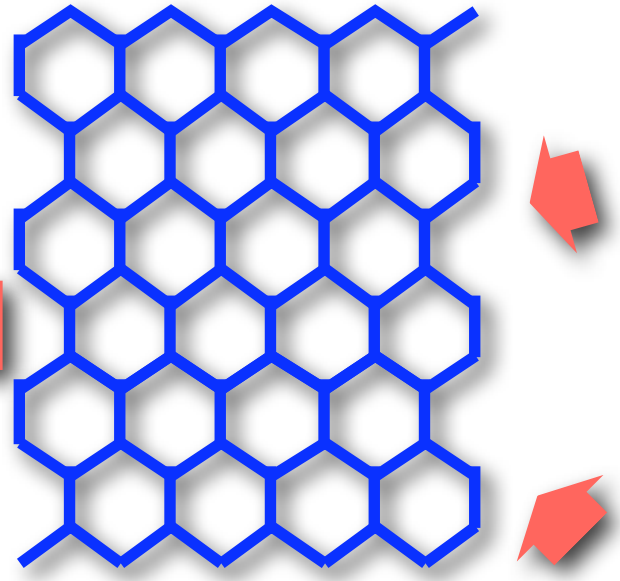
System can be implemented fully on a hexagonal nanowire network ?

Nanoprocessor system

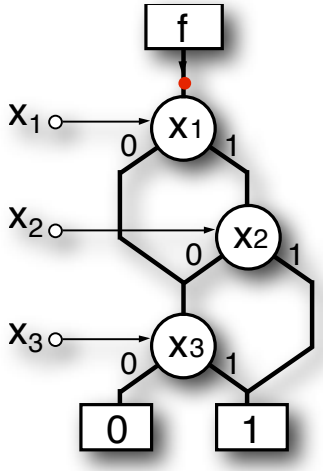


von Neumann architecture

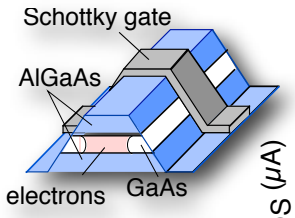
Hexagonal nanowire network

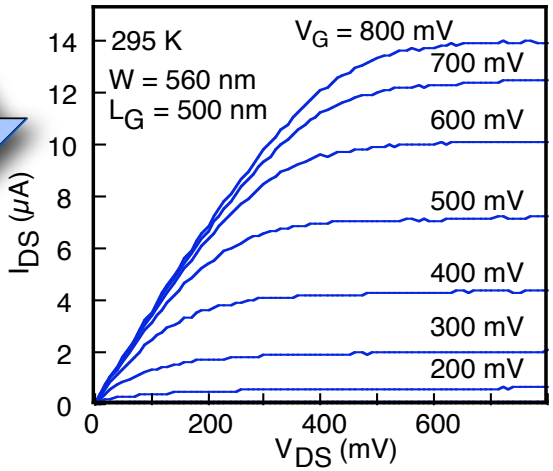


Hexagonal BDD



WPG nanowire FET

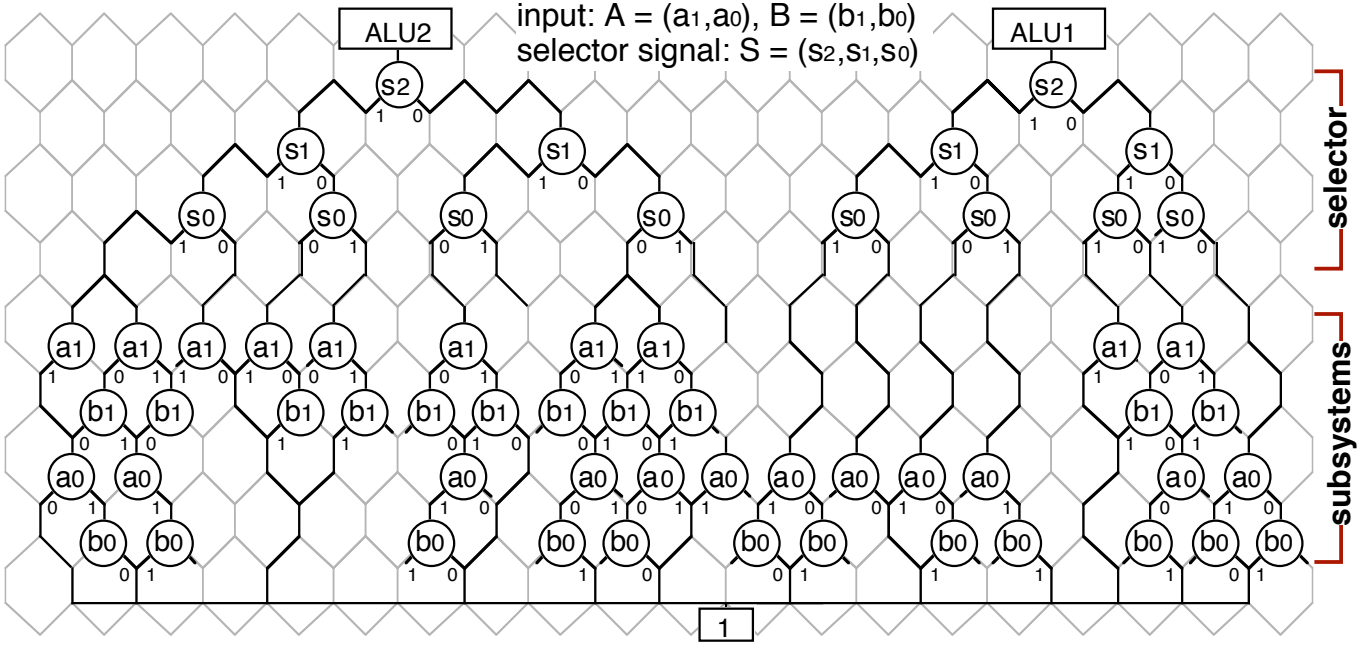




- Execution core : **Hexagonal BDD**
- Register, counter (sequential) : **WPG nanowire FET**

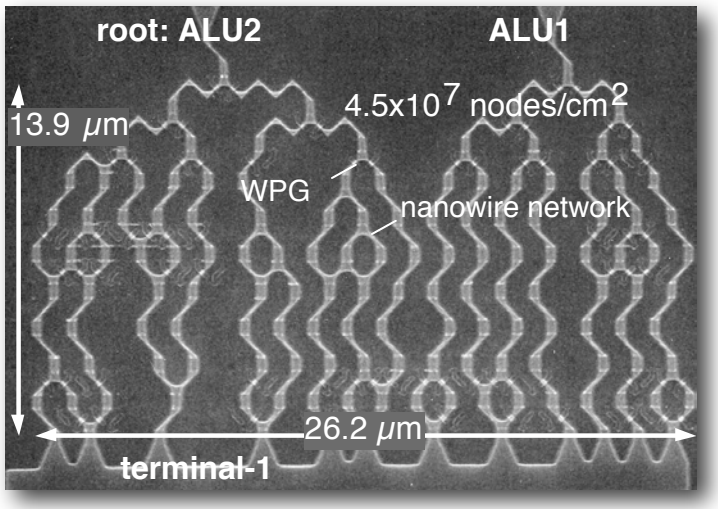
Hexagonal BDD-based ALU

8-instruction 2-bit ALU



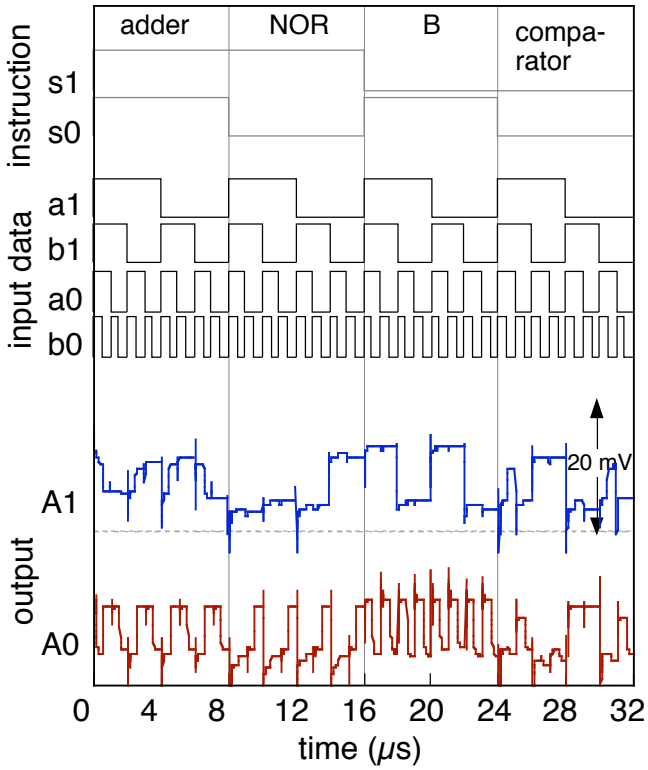
8 instructions:

S = 111: A+B, 100: AND, 110: NOT, 101: OR
010: bit left shift, 011: bit right shift, 000: comparator, 001: A-B



Input-output waveforms

(simulation)



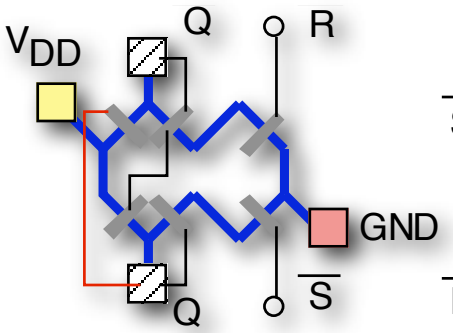
- **ALU can be designed using small number of devices**

  BDD 2-bit ALU (8-inst.) device count: **56**
  CMOS 2-bit ALU (7-inst.) Tr count: **144**

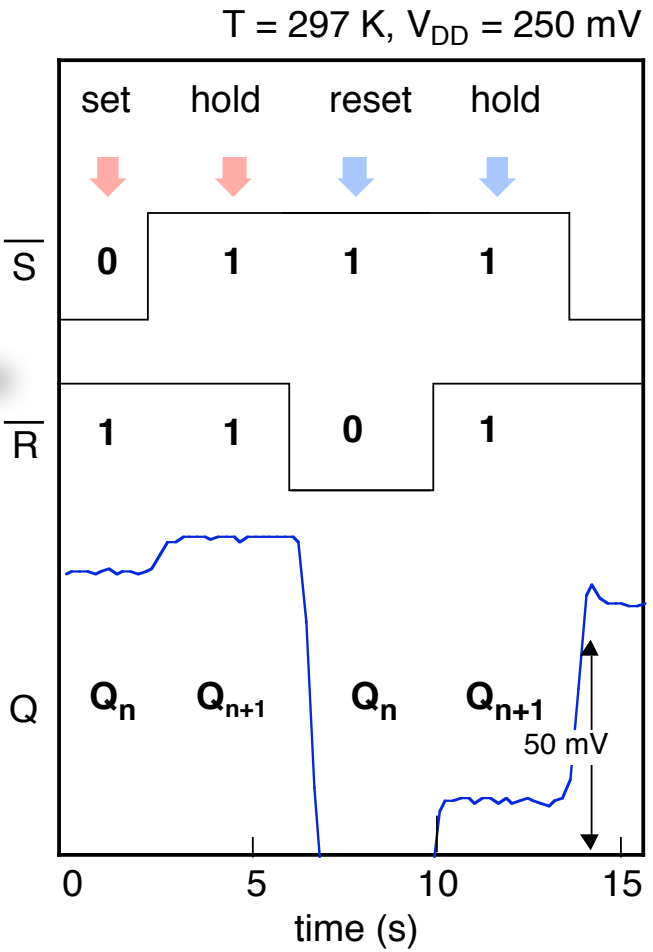
- **Fabrication of 2-bit ALU on etched nanowire network**

Implementation of Sequential Circuits

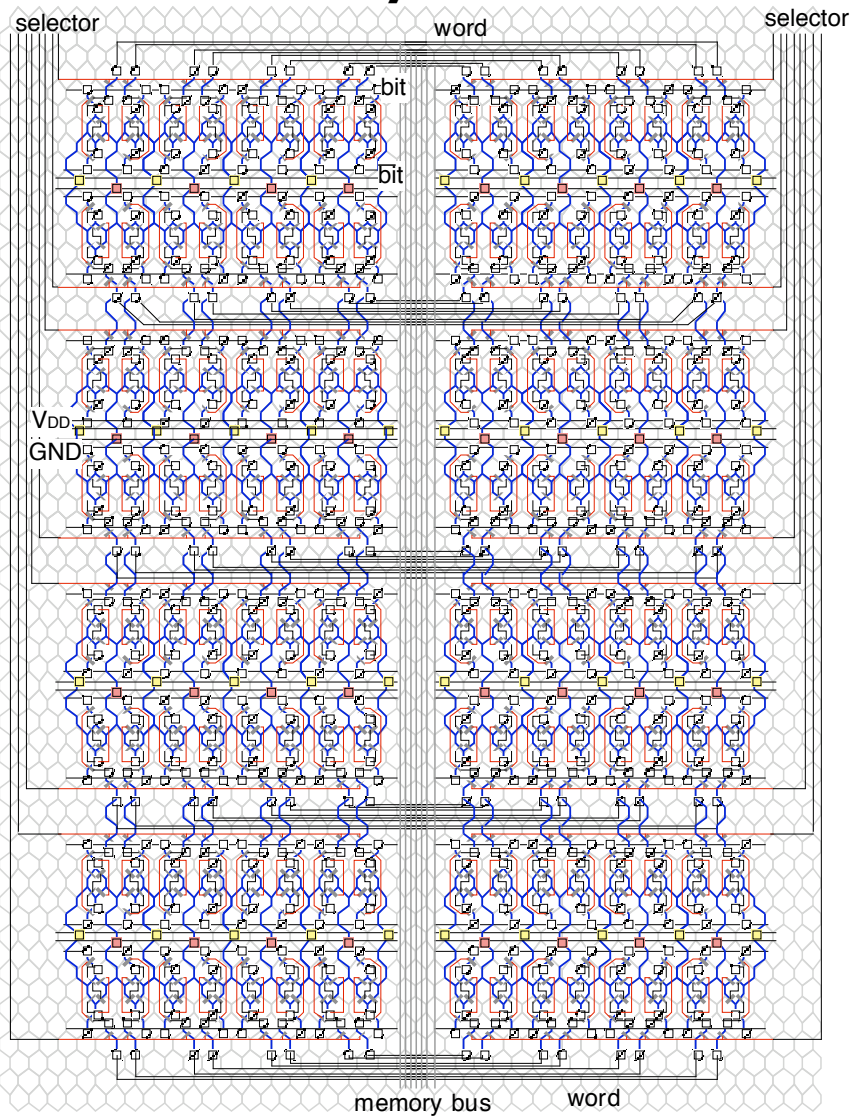
WPG FET-based RS Flip Flop



$\overline{S}$	$\overline{R}$	Q_{n+1}
1	1	Q_n
1	0	0
0	1	1
0	0	–



128-bit SRAM layout

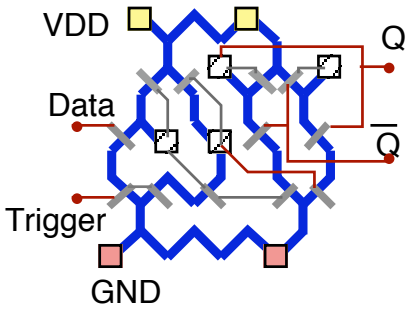


60 x 44 hexagons

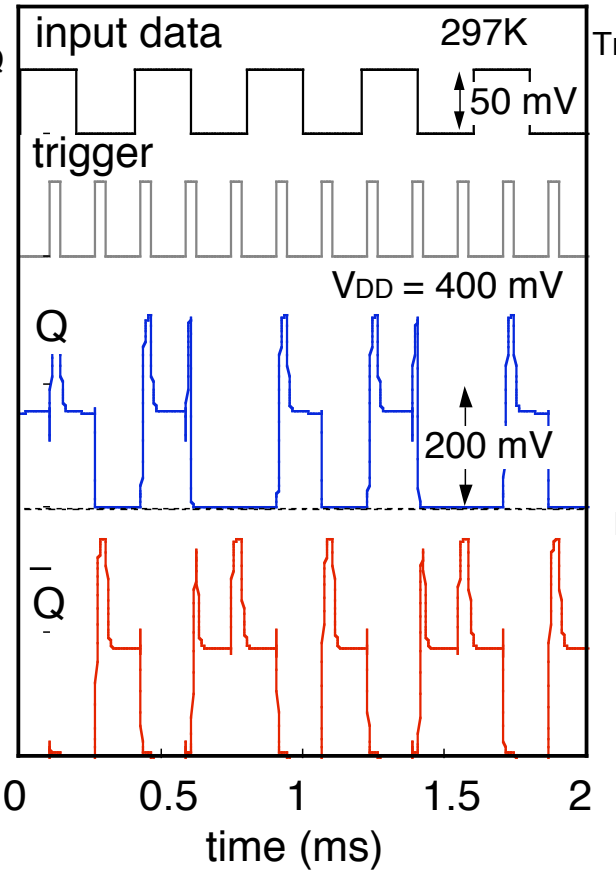
- **Experimental confirmation of correct operation of RS-FF at RT**
- **Successful design of SRAM unit**

Register and Counter

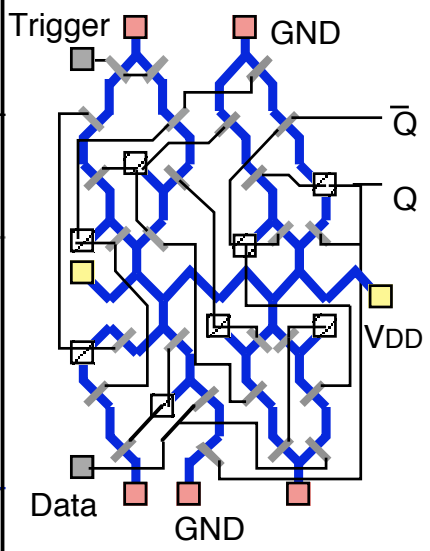
D-FF design



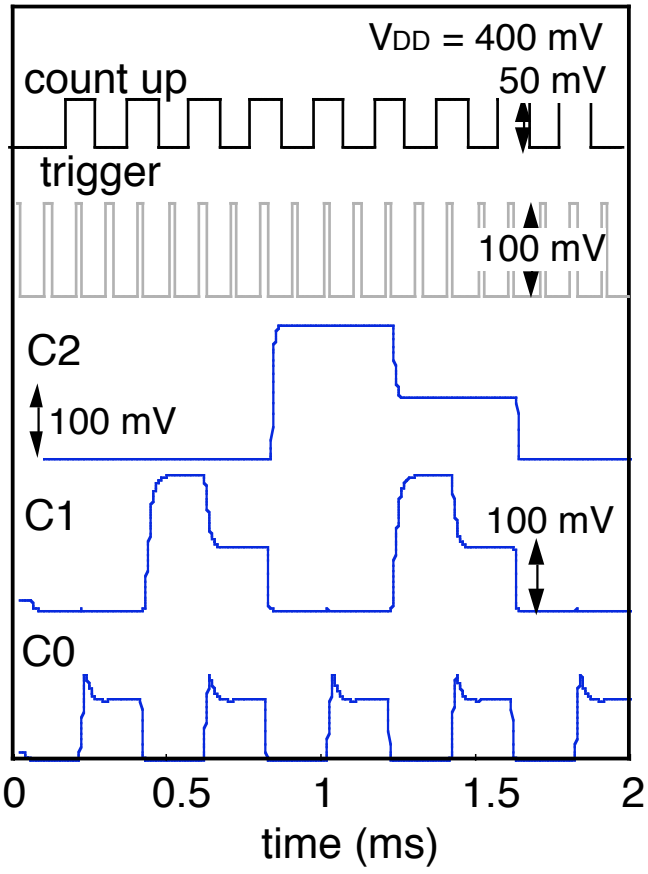
D-FF input-output waveform
(simulation)



T-FF design

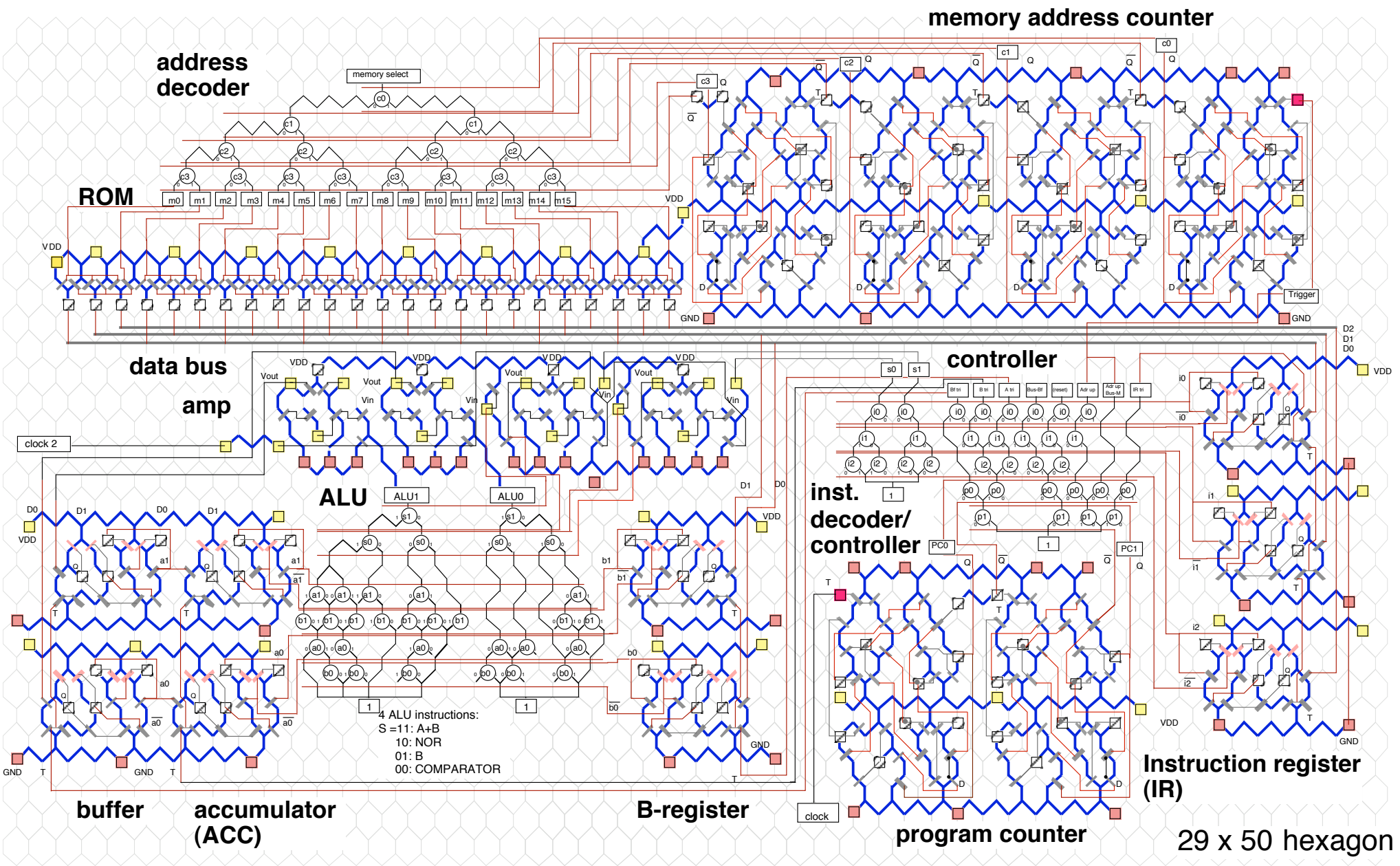


3-bit counter operation
(simulation)



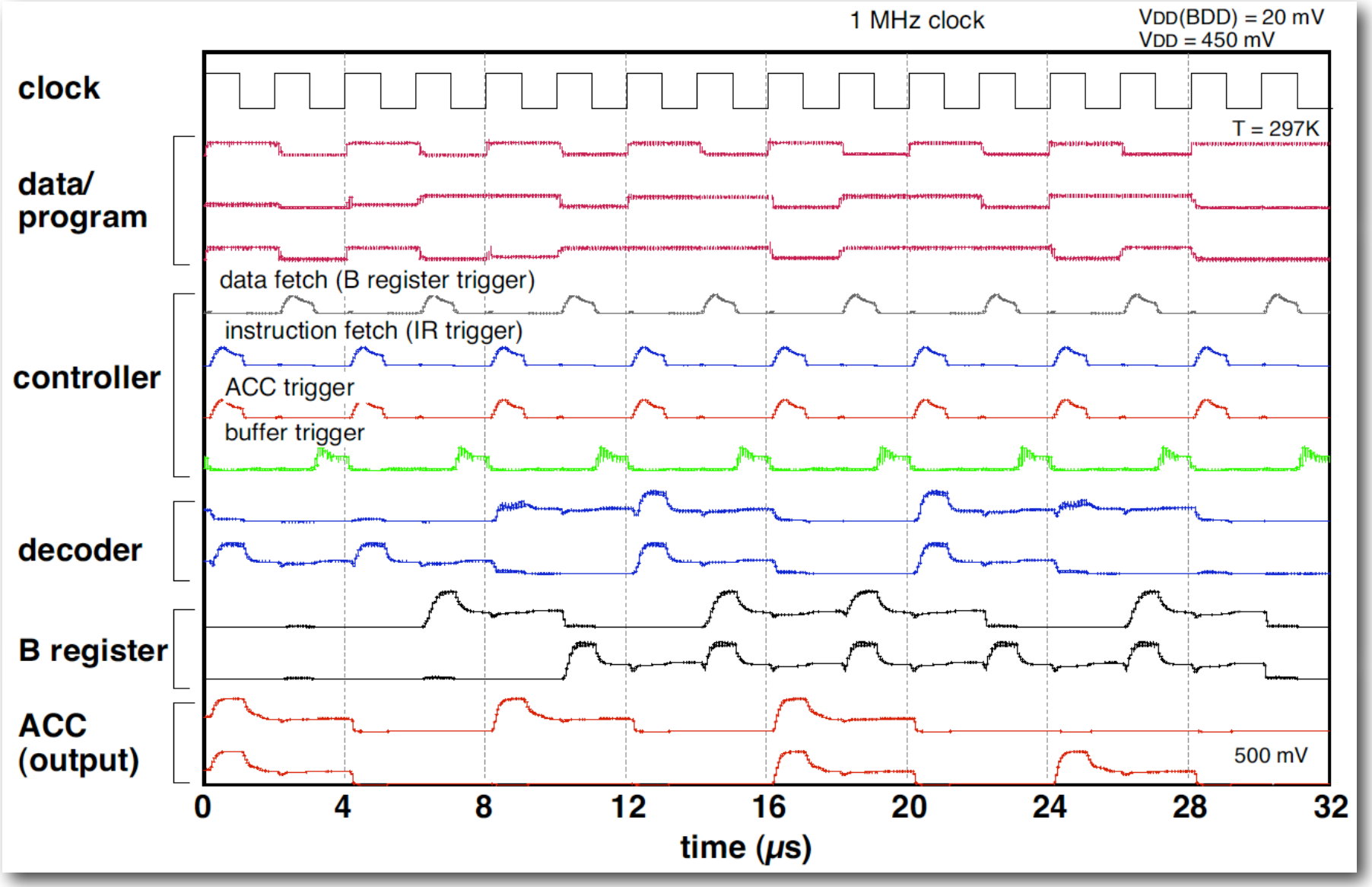
- **Correct operation of D-FF, T-FF and counter with small input voltage swing**

Hexagonal BDD-based 2 bit Nanoprocessor



- **Successful design of 2-bit NPU on 29 x 50-node network**

2 bit Nanoprocessor System Operation

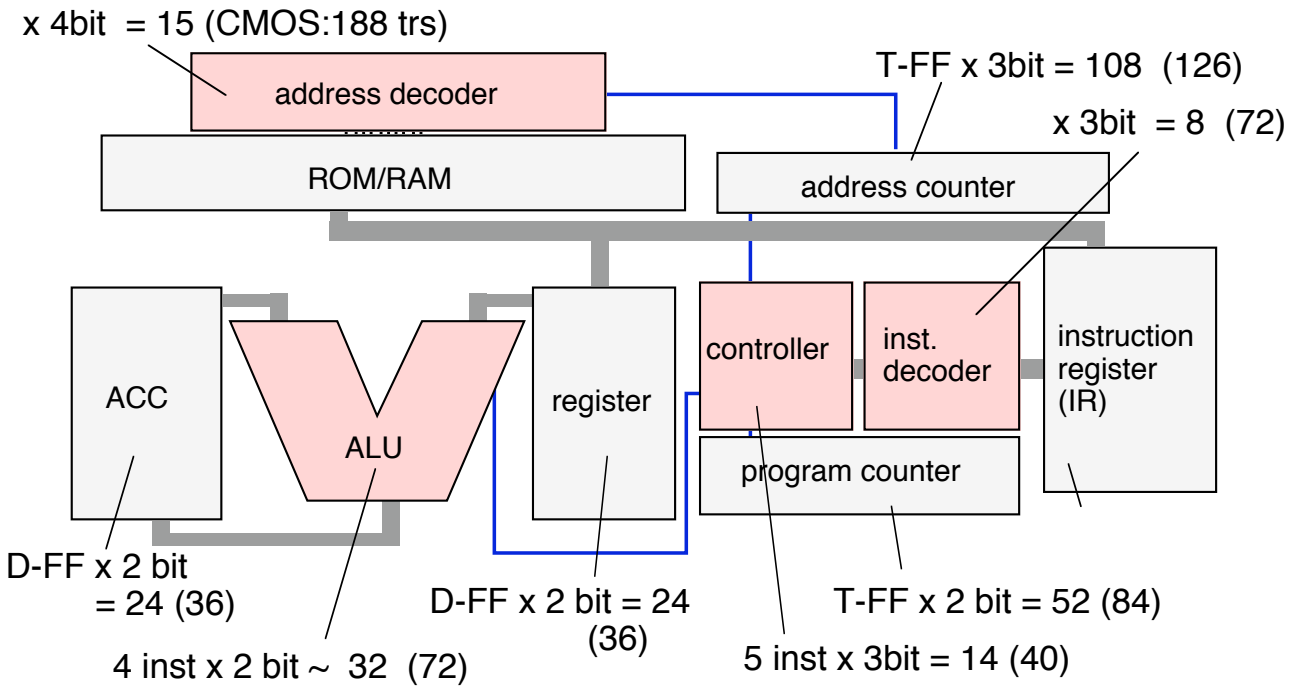


- **Correct operation of the system was confirmed by simulation**

Nanoprocessor Performance

Power consumption = activity factor x device count x PDP x clock

Device counts in system



Total 381 devices (CMOS: 740 Trs)

Activity factor

unit	activity factor
BDD	
address decoder	0.20
ALU	0.11
controller	0.14
inst. decoder	0.13
Sequential	
ACC	0.09
IR	0.09
register	0.09
add. counter	0.15
prog. counter	0.31
average	0.2

- **Power consumptions** at 10MHz operation

SE-type BDD: PDP = 10^{-22} J (sequential:10^{-20} J) → **0.01 nW**

65 nm CMOS: PDP = 10^{-16} J → **15 nW**

x 0.001

Chip Size

Hexagonal BDD-based 2-bit NPU

Node density	System area	
45 M/cm^2	3,200 μm^2	fab. process available
1 G/cm^2	145 μm^2	nanowire network
1.5 G/cm^2	**85 μm^2**	**nanowire network hp 65**
13 G/cm^2	11 μm^2	hp 22

area = 29 x 50 hexagons

node density ~ 1/(4 hp)^2

CMOS-based 2-bit MPU

Tech. node	System area	
130 nm	2,100 μm^2	
65 nm	**530 μm^2**	on the market
45 nm	260 μm^2	
22 nm	62 μm^2	end of CMOS

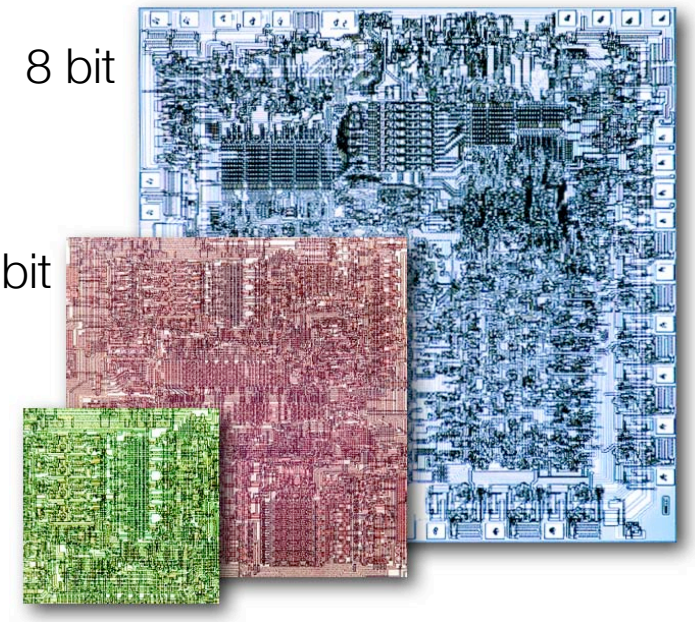
area = const. x Trs x hp^2
= 170 x 740 Trs x hp^2

- **Hexagonal BDD NPU chip size ~ 0.2 x CMOS MPU**

Nanoprocessor Specification

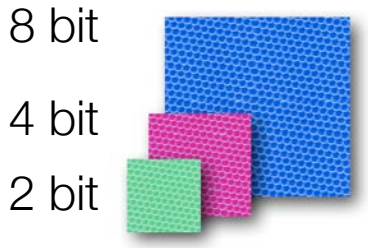
- **Size**

MPU

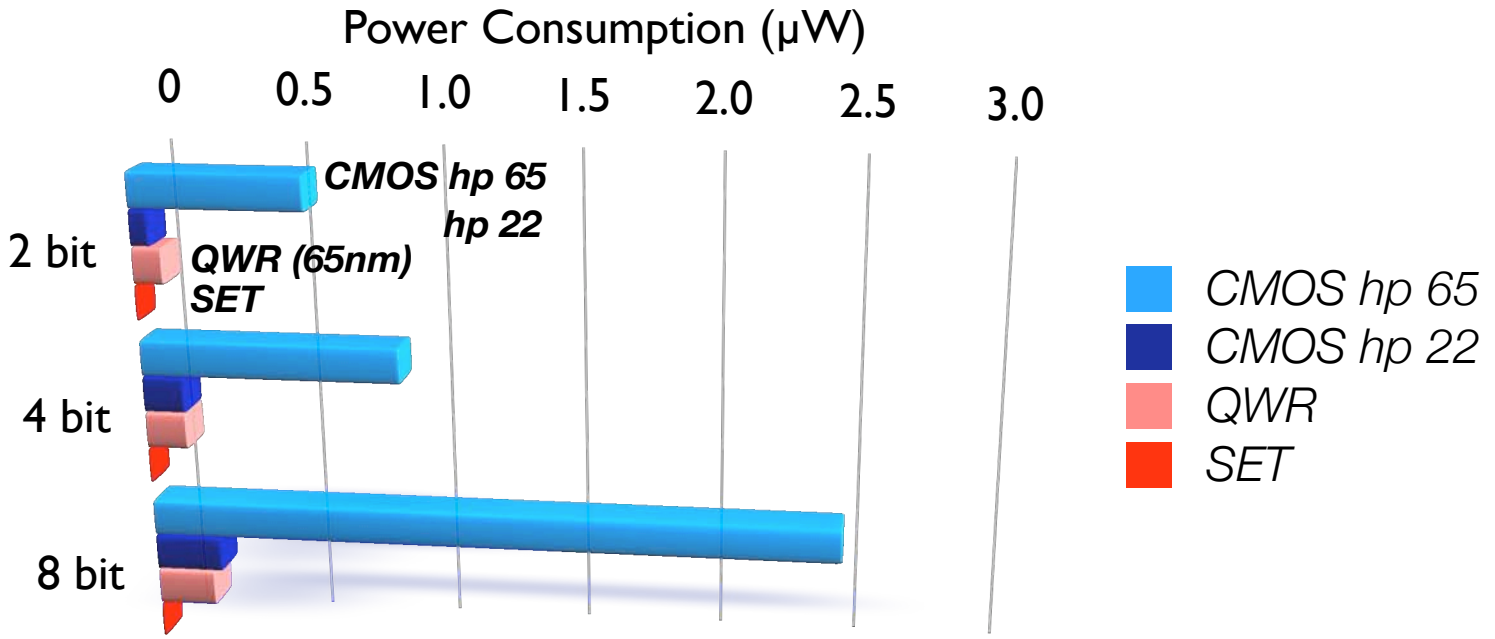


⟷ **10 μm @ hp65**

NPU



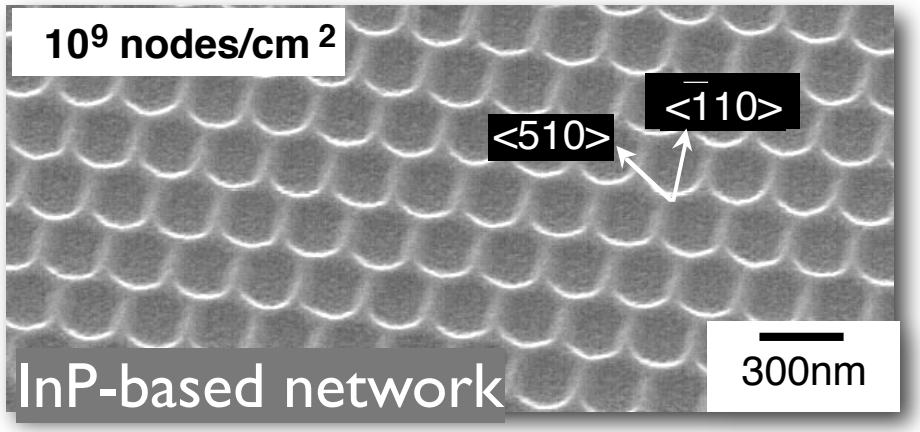
- **Power**



Future Options

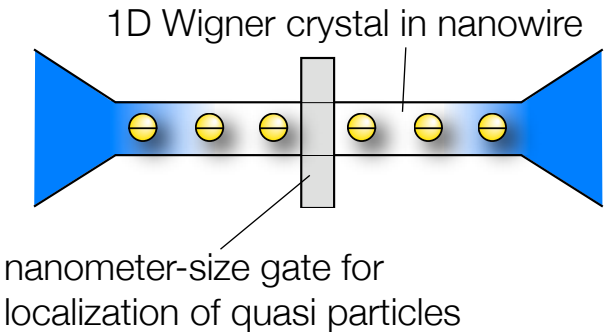
- **High-density integration**

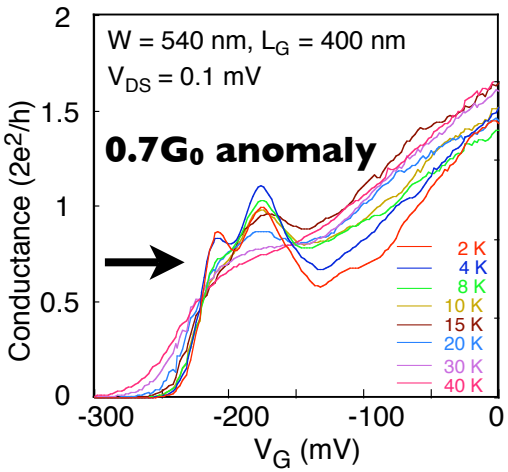
  high-density nanowire network formation utilizing various materials and processes

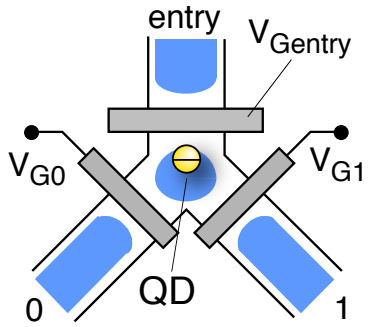


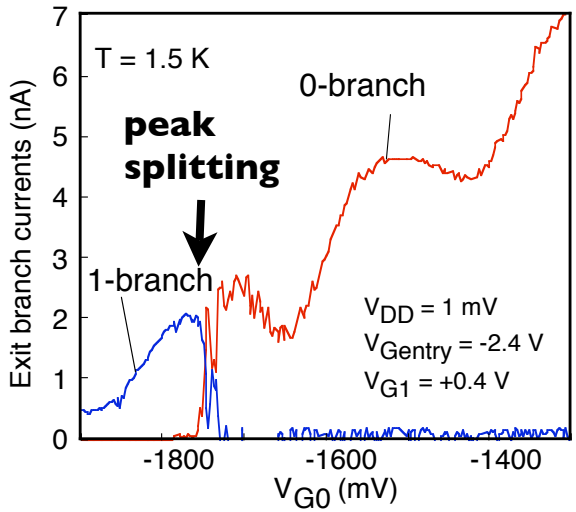
- **Low power consumption**

  low-density electron system and correlations in nanostructures
  - reduction of electrons/bit : *single electron control in 1D wire*
  - reduction of ΔV_G: *splitting a conductance peak in SE device*









Summary

- Novel quantum nanodevice-based logic circuits was presented.
  "Hexagonal BDD logic quantum circuit"
  = III-V semiconductor nanowire networks
  + hexagonal BDD logic architecture

- Hexagonal BDD quantum circuits have possibility to realize ultra-low power and ultra-small digital systems beyond the scaling limits of Si CMOS technology.

- Basic technologies of hexagonal BDD quantum circuit has been established successfully.

- Based on the hexagonal BDD, nanoprocessor (NPU) has been intensively investigated for an ultra-small knowledge vehicle in advanced ubiquitous society.