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Fabrication and Characterization of InGaAs/InAlAs Insulated Gate Pseudomorphic HEMTs Having a Silicon Interface Control Layer

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SUMMARY A novel InGaAs/InAlAs insulated gate (IG) pseudomorphic high electron mobility transistor (PHEMT) having a silicon interface control layer (Si ICL) is successfully fabricated and characterized. Systematic efforts to characterize and optimize the insulated gate structure and the PHEMT fabrication process were made by using *in-situ* X-ray photoelectron spectroscopy (XPS) and capacitance-voltage (*C-V*) techniques. This led to successful fabrication of a novel IG-PHEMT showing excellent stable DC characteristics with a good pinch off and a high transconductance (177 mS/mm), very small gate leakage currents, very high gate breakdown voltages (about 40 V) and respectable RF characteristics $f_T = 9$ GHz and $f_{max} = 38$ GHz.
key words: insulated gate, PHEMT, InGaAs, interface control, Fermi level pinning

1. Introduction

Realization of a good insulated gate (IG) structure with acceptably low interface state densities on III-V compound semiconductors has been a long standing issue due to strong Fermi level pinning which takes place at the insulator-III-V compound semiconductor interface due to high-density interface states [1], [2]. Previous III-V insulated gate field effect transistors (IGFETs) suffered from problems such as poor gate controllability, large drain current drift and poor reliability. Only very recently, a novel approach for GaAs using a $\text{Ga}_2\text{O}_3/\text{Gd}_2\text{O}_3$ [3]–[5] structure has realized a well behaved n-channel depletion mode GaAs metal-insulator-semiconductor field effect transistors (MIS-FETs) [5], although the performance of the enhancement mode device seems to be still poor. Thus, field effect transistors based on III-V semiconductors usually depend on Schottky gate structures in contrast to the case of silicon metal-oxide-semiconductor field effect transistors (MOSFETs). In fact, availability of stable Schottky barriers with high barrier heights have made GaAs-based metal-semiconductor field effect transistors (MESFETs) and high electron mobility transistor

(HEMT) devices commercially viable.

On the other hand, Schottky barriers in InP-based materials, in general, do not well behave as those of GaAs and related materials [6]. Thus, the InP-based InGaAs/InAlAs pseudomorphic HEMT (PHEMT) with the conventional Schottky gate structure is subject to various potential problems particularly in high power applications. Namely, the problems are large DC gate leakage current, low breakdown voltage, poor RF power handling capability, poor reproducibility and reliability. These are due to the low and unstable barrier height at the Schottky interface as well as due to forward conduction inherent in the Schottky gate structure. Since the InP-based PHEMT is a promising candidate for the key device in next generation ultra-high-speed wireless and optical communication systems due to its unsurpassed excellent high frequency performance [7], [8], solution of the above mentioned problems by employing a suitable IG structure is highly desirable.

As an effective surface passivation technology for III-V semiconductors, use of a silicon interface control layer (Si ICL) was proposed by Hasegawa et al. [9] for GaAs and InGaAs, and detailed structural and electronic characterization have been made [10], [11]. The effectiveness of this technology has been clarified in a macroscopic way by dramatic increase of photoluminescence from near-surface AlGaAs/GaAs quantum wells [12] and InAlAs/InGaAs quantum wires [13] as well as by realization of stable InGaAs MISFETs [14]. A preliminary attempt to realize an InP-based insulated gate (IG) HEMT was made which gave a promising DC result [15], and indicated necessity for a further systematic study. More recently, a scanning tunnel microscopy (STM)/scanning tunnel spectroscopy (STS) study also has been made on a clean MBE GaAs surface, showing the effectiveness of the Si ICL in a microscopic atomic scale [16].

The purpose of this paper is to systematically optimize the Si ICL-based insulated gate technology for the InGaAs/InAlAs structure and to fabricate an InP-based IG-PHEMT device based on this optimization. The first DC/RF results were briefly reported elsewhere [17]. In this paper, especially, the details of the design,

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fabrication and characterization of the IG structure and the IG-PHEMT device are presented. The optimized IG structure has led to successful fabrication of a novel IG-PHEMT showing excellent stable DC characteristics with a good pinch off and a high transconductance, very small gate leakage current, very high gate breakdown voltage and respectable RF characteristics ($f_T = 9$ GHz and $f_{max} = 38$ GHz).

2. Novel Gate Structure and Its Characterization

2.1 Gate Structure and Control of Quantum State

The structure of the novel insulated gate having a Si ICL applied to a standard InP-based PHEMT wafer structure is schematically shown in Fig. 1. In this structure, an ultrathin pseudomorphic Si layer grown by molecular beam epitaxy (MBE) is inserted between a Si-based insulator and the standard PHEMT wafer which usually has an InGaAs cap layer. It should be noted that the Si ICL is formed directly on the InGaAs cap layer. This is because the natural oxide layer of the InGaAs cap layer is easier to remove than that of the InAlAs layer which is inevitably formed by etching the InGaAs cap layer.

In Fig. 1, it is assumed that the thickness of the Si ICL is smaller than the critical layer thickness of Si on InGaAs so that the Si ICL maintains pseudomorphic lattice matching to the underlying InGaAs/InAlAs structure. It is also assumed that the Si ICL forms a high quality interface with the Si-based insulator with an acceptably low interface state density. When these two conditions are satisfied, ordered and coherent bonding transition from the III-V semiconductor to the Si-based insulator is achieved, and generation of interface gap states within the energy gap of the Si ICL should be suppressed according to the disorder induced gap state (DIGS) model for the Fermi level pinning [2].

Additionally, one has also to pay attention to the band states of the Si ICL, since a significant band gap

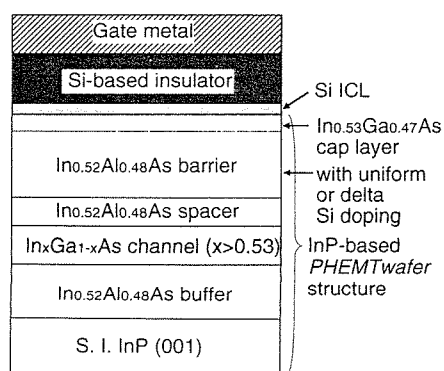


Fig. 1 A novel insulated gate (IG) structure for an InP-based PHEMT.

narrowing of the Si is expected due to tensile stress at the interface. The calculated band line-up in the new gate structure using the model solid theory [18] is shown in Fig. 2(a). The actual calculation procedure is fairly complicated and is described elsewhere [19]. It is anticipated in Fig. 2(a) that the Si conduction band states below the conduction band edge of the InGaAs cap layer will behave like interface states. This problem can be avoided by using a sufficiently thin Si ICL where the electron band states are pushed out from the ultra-narrow Si surface quantum well. A quantum mechanical calculation similar to that made for GaAs [11] and InP [20] gave a result shown in Fig. 2(b). According to this, the thickness of the Si ICL should be below 0.6 nm.

2.2 Fabrication of New Insulated Gate Structure

Fabrication, characterization, and optimization of the new insulated gate structure were done in an ultrahigh vacuum (UHV)-based growth/fabrication/characterization system where an MBE chamber, an electron cyclotron resonance (ECR) chemical vapor deposition (CVD) chamber, an X-ray photoelectron spectroscopy (XPS) chamber, a contactless capacitance-voltage ($C-V$) measurement chamber and other UHV-based chambers are connected by a common UHV transfer chamber. The base pressure of the system was 1×10^{-10} Torr.

As the first step of the gate structure fabrication, InGaAs/InAlAs PHEMT wafers with InGaAs cap layers were grown on both semi-insulating and n^+ semi-conducting (001) InP substrates in the MBE cham-

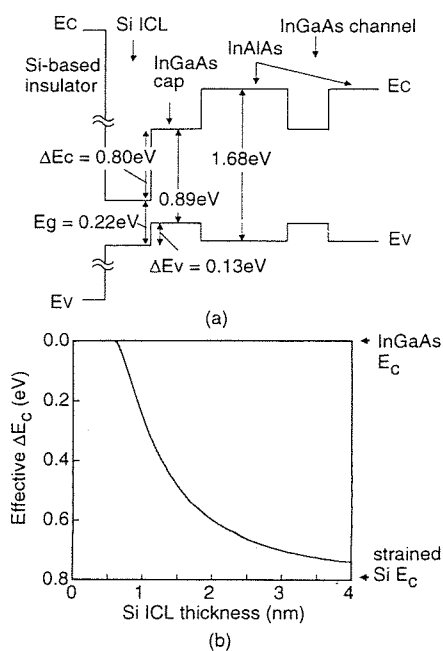


Fig. 2 Calculated band line-up in the novel gate structure.

ber with metallic Ga, In, Al and As sources. The pHEMT structure included from the bottom, a 200 nm-thick InAlAs buffer layer, a 10 nm-thick pseudomorphic $\text{In}_{0.7}\text{Ga}_{0.3}\text{As}$ channel layer, a 5 nm-thick InAlAs spacer layer, a 30 nm-thick InAlAs barrier layer and a top 10 nm-thick Si doped n^+ -InGaAs cap layer ($N_D = 5 \times 10^{18} \text{ cm}^{-3}$). Either uniform or delta Si doping was made into the InAlAs barrier layer. Typical values of the Hall mobility and sheet carrier density at 300 K were $7700 \text{ cm}^2/\text{Vs}$ and $1.9 \times 10^{12} \text{ cm}^{-2}$, respectively. After the growth, the wafers were taken out to air. This was intentionally done to develop an insulated gate fabrication process which is applicable to commercial PHEMT wafers with air exposed surfaces. For the purpose of investigating the electronic properties of the Si ICL-InGaAs interface directly by the C - V method, thick n -InGaAs layers were also grown directly on the n^+ -InP substrates.

Then, a systematic XPS study was made to optimize the surface preparation prior to the Si ICL formation. Since the n^+ -InGaAs cap layer was primarily important to obtain good source and drain ohmic contacts, a simplest idea was to completely remove the cap layer by recess-etching after ohmic contact formation. However, in this case, the InAlAs layer was exposed to the air and a native oxide layer was inevitably formed. It was found extremely difficult to remove the resultant Al oxide component and the IG FET devices with such an oxide layer did not work even when the Si ICL was inserted. On the other hand, we previously found that the native oxide layer on the InGaAs surface could be completely removed by the HF treatment [21]. This solution led to an As-rich surface after oxide removal, but stoichiometry of InGaAs was completely recovered after Si ICL deposition.

In the present device, we also found empirically that the optimum surface treatment was to leave a very thin InGaAs cap layer of 1 nm or so. With such a layer with 0.5 nm Si ICL, the Si donors in the InGaAs cap layer with a sheet carrier concentration below $5 \times 10^{11} \text{ cm}^{-2}$ are expected to remain neutral due to strong quantum confinement, giving no important contributions to surface conduction and to the threshold voltage control.

Therefore, after formation of ohmic contacts, the 10 nm-cap layer was recess-etched down to a few nm including a thin surface native oxide layer of about 1 nm or so by H_3PO_4 -based etchant and then, the native oxide layer was completely removed by the HF treatment. XPS study showed about 10 Å (1 nm)-thick cap layer remained after this process. To avoid unintentional oxidation, the pre-growth HF surface treatment was done in a N_2 ambient and the sample was quickly loaded into the MBE chamber keeping the sample in the N_2 ambient.

The growth of the Si ICL was done again in the MBE chamber, using the Si Knudsen cell as Si source.

The Si deposition rate was calibrated by the Si doping rate into GaAs. Typically, 1 nm-thick Si layer was grown at substrate temperatures of 250–290°C at which temperature inter-diffusion of Si into InGaAs is negligible. The thickness of the Si ICL was kept below the critical layer thickness of the Si on InGaAs which is 1.5 nm according to the well known formula by Matthews and Blakeslee [22]. Pseudomorphic growth of Si was confirmed by the streak patterns of the reflection high energy electron diffraction (RHEED) measurement.

Thickness adjustment of the Si ICL and formation of high quality interface between the Si ICL and the outer Si-based insulator are obviously critical factors for successful formation of the present new gate structure. Preliminary attempts of forming the Si ICL to the required thickness of 0.6 nm followed by direct ECR plasma CVD deposition of SiO_2 or Si_3N_4 gave very poor interface properties. This was due to uncontrollable inhomogeneous interface reactions. Particularly, excited oxygen radical species penetrated through the Si ICL and oxidized the InGaAs underneath in the case of deposition of SiO_2 . After various trials, the best procedure we found was to grow a thicker Si ICL of about 1 nm at first, and then to do partial surface nitridation of the Si ICL by irradiating the surface with the N_2 plasma in order to obtain an ultrathin SiN_x/Si structure with the optimum Si thickness. Detailed *in-situ* XPS measurements were made for *in-situ* process optimization of the ultrathin SiN_x/Si structure. Examples of angle resolved XPS data are given in Figs. 3(a) and 3(b), showing the presence of the ultrathin Si layer and the silicon nitride component. A quantitative analysis of these data using the photoelectron penetration depth data gave the thickness of the silicon nitride of 0.7 nm in this example.

Finally, a thicker SiO_2 or Si_3N_4 was deposited as the main gate dielectric by standard CVD procedure, followed by deposition of the gate metal. In this study, a 40 nm SiO_2 was deposited by the plasma CVD process, and vacuum deposited Cr/Au was used as the gate metal. Thus, the optimum insulated gate structure that we achieved and used in the device fabrication in the present study had the structure shown in Fig. 3(c).

2.3 Capacitance-Voltage Analysis

In order to assess the interface quality of the novel gate structure, three types of MIS capacitors shown in Figs. 4(a)–(c) were fabricated. The structure in Fig. 4(a) is a simple InGaAs MIS sample to directly obtain information on the Si ICL/InGaAs cap interface, and those in Figs. 4(b) and (c) are the vertical and lateral MIS capacitors having the complicated PHEMT wafer structure actually used in the device fabrication. It should be noted that the InGaAs cap layer was recess-etched to about 1 nm in Figs. 4(b) and 4(c) similarly to fabrication of the IG-PHEMT device. The

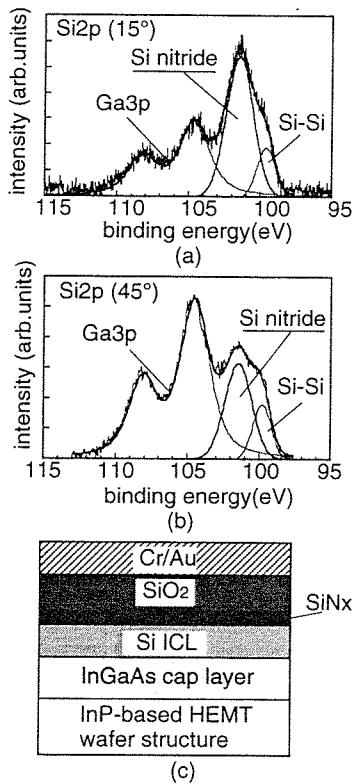


Fig. 3 (a) and (b) Angle resolved XPS data for SiNx/Si/InGaAs structure. (c) The optimum IG structure used for PHEMT fabrication.

C-V characteristics these samples were measured in detail within the temperature range of 50 K–300 K and for the frequency range of 1 kHz–10 MHz. Since the discussion of such detailed data are beyond the scope of the present paper, they will be presented elsewhere [19], and only a brief summary is given below.

The InGaAs MIS capacitor with a Si ICL shown in Fig. 4(a) showed an excellent interface property with a U-shaped interface state density distribution with its minimum in the range of $10^{10} \text{ cm}^{-2} \text{ eV}^{-1}$ in agreement with the previous result [21].

The important question is whether such a good interface quality is maintained in the actual PHEMT capacitors. It turned out rather unfortunately that the capacitors in Figs. 4(b) and 4(c) show strong frequency dispersion under accumulation bias which is similar to those of conventional GaAs MIS capacitors. Examples of observed frequency dispersion of capacitance measured at 300 K for the lateral capacitor structures in Fig. 4(c) are shown in Figs. 5(a) and 5(b) for the case of without and with Si ICL, respectively. Both show similar strong frequency dispersion of capacitance under accumulation bias, and presence of high density of interface states is suspected.

However, subsequent frequency-temperature analysis showed that two capacitors behave very differently as shown in Figs. 5(c) and 5(d). In the case of the sample without Si ICL, frequency dispersion showed strong

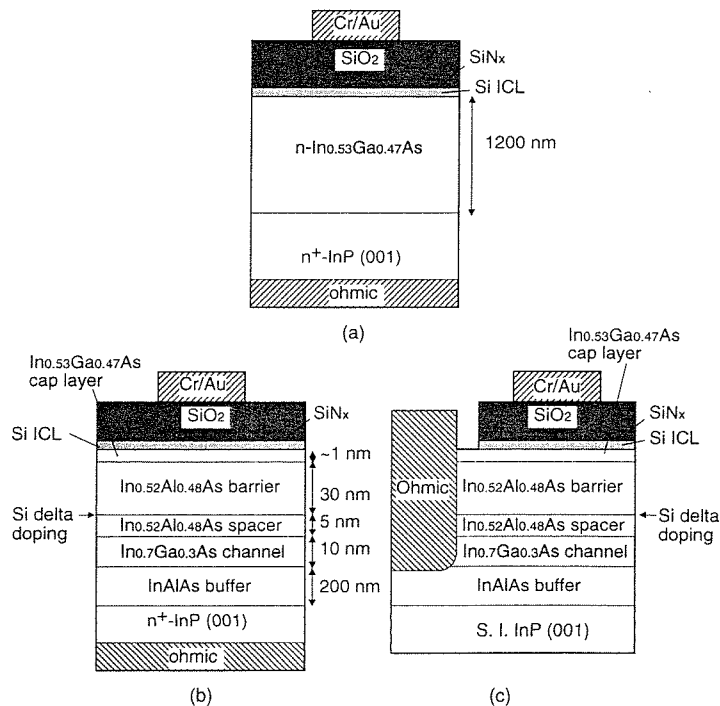


Fig. 4 MIS capacitor structures used for interface assessments. (a) InGaAs MIS capacitor, (b) vertical PHEMT MIS capacitor and (c) lateral PHEMT MIS capacitor.

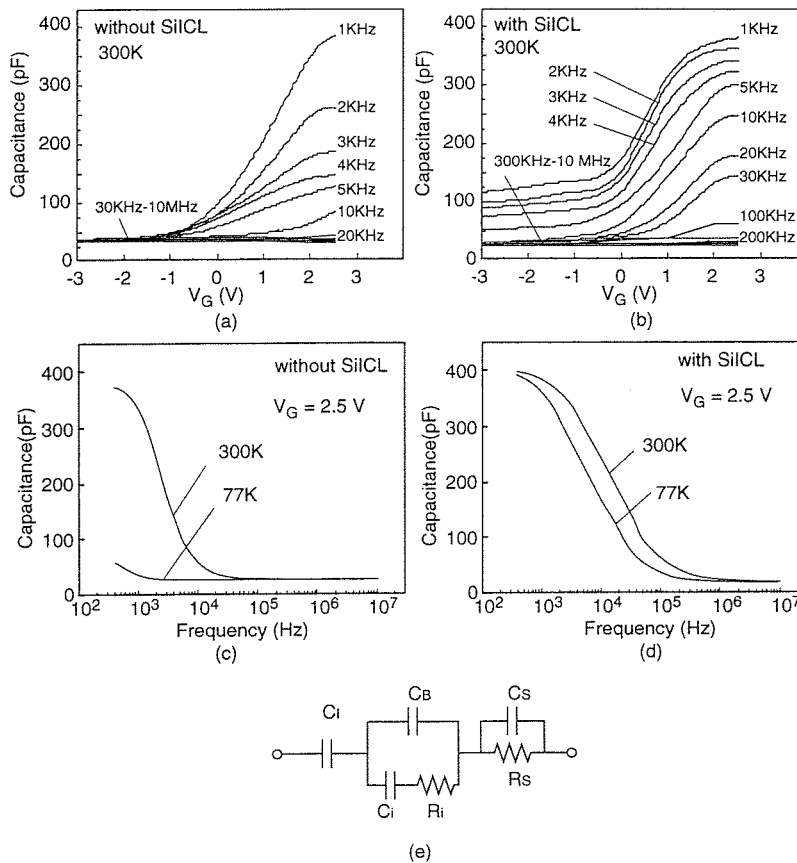


Fig. 5 Observed capacitance-voltage (C - V) and capacitance-frequency (C - f) data for lateral PHEMT MIS capacitors. (a) and (b) C - V curves without and with Si ICL. (c) and (d) C - f curves without and with Si ICL. (e) Equivalent circuit of the lateral diode.

temperature dependence as seen in Fig. 5(c). This indicates that the dispersion is indeed due to interface states that lie deep in the energy gap.

For further discussion, a simplified equivalent circuit of the present MIS structure including the effect of the interface states by a single time constant model [23] is shown in Fig. 5(e). Here, C_I is the insulator capacitance, C_i is the interface state capacitance, R_i is the carrier supply resistance of the interface state, C_B is the semiconductor depletion layer capacitance, and R_S and C_S are the lateral resistance and capacitance of the channel layer. C_i is proportional to the interface state density and R_i is inversely proportional to it, so that the product $R_i C_i$ corresponds to the emission time constant of the interface state at the Fermi level. At room temperature, the value of the time constant $R_i C_i$ was estimated to be 10^{-3} – 10^{-4} sec, explaining the observed dispersion. Since the emission time constant increases exponentially with temperature reduction, the behavior in Fig. 5(c) was also quantitatively consistent with the interface state model.

On the other hand, in the sample with Si ICL, the observed very weak temperature dependence shown in Fig. 5(d) cannot be explained by such an interface state model. A further careful analysis using the equivalent

circuit in Fig. 5(e) led to the conclusion that the dispersion is simply due to a much less temperature dependent series lateral resistance, R_S , that cannot be avoided in the lateral sample structure. Thus, a good interface without Fermi level pinning is maintained in the PHEMT MIS structure with Si ICL and accumulation is achieved in the sample.

To further check the validity of the present interpretation, the effective channel depth was estimated from the capacitance data in Fig. 5(b). The gate insulator capacitance, C_I , was estimated to be 400 pF from the measured low-frequency capacitance in the accumulation region, $V_G \gg 0$ V. The low frequency gate capacitance value in Fig. 5(b) under large negative gate voltages can be interpreted as a series connection of C_I and C_B , assuming $C_i = 0$. From this, C_B was found to be 160 pF. Then, the effective channel depth, d , is estimated to be 31 nm from the simple equation, $C_B = \epsilon_r \epsilon_0 S/d$, where ϵ_r is dielectric constant of the barrier layer and S is the electrode area (here, $S = 4.3 \times 10^{-4}$ cm²). This value reasonably agrees with the designed channel depth of 35 nm.

On the other hand, in the vertical PHEMT MIS structure shown in Fig. 4(b), presence of similar frequency dispersion was also seen for the case of with

and without Si ICL. However, a detailed analysis gave a similar conclusion with a different mechanism as discussed elsewhere [19], [24] and a good interface without Fermi level pinning was obtained for the sample with Si ICL.

3. Fabrication and Characterization of IG-PHEMTs

3.1 Device Structure and Fabrication Process

Using the optimized insulated gate structure, IG-PHEMT devices were fabricated. The cross-sectional structure of the device is shown in Fig. 6. The device has the optimized novel insulated gate structure shown in Fig. 4(a).

The sequence of the device fabrication process is shown in Fig. 7. The details are given below.

- (1) Device isolation by photolithography and wet chemical etching with a solution of $\text{H}_3\text{PO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O} = 1:1:38$.
- (2) Formation of Ge/Au/Ni source and drain electrodes in the air and alloying at 370°C , 5 min, in N_2 .
- (3) Pre-growth surface etching and treatment in

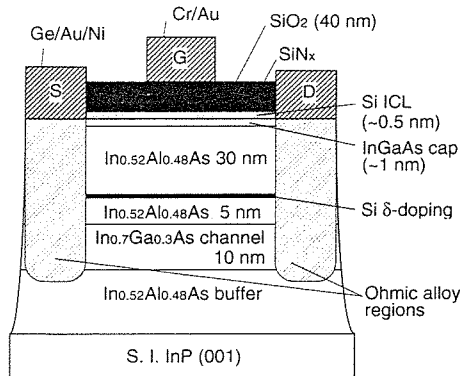


Fig. 6 Cross-sectional structure of InGaAs/InAlAs IG-PHEMT.

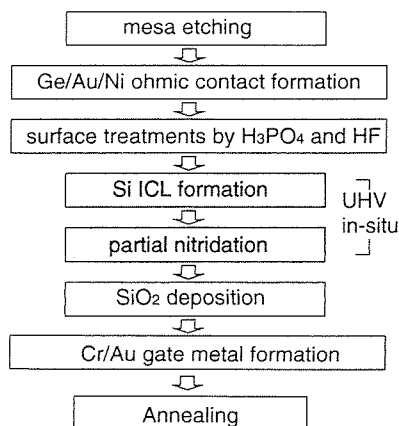


Fig. 7 Process sequence for fabrication of IG-PHEMT.

H_3PO_4 -based etchant and HF solution, respectively, under N_2 atmosphere.

(4) Formation of Si ICL by MBE at a substrate temperature of 280°C , its surface nitridation by irradiation of N_2 plasma in the ECR chamber and deposition of SiO_2 in the UHV system.

(5) Formation of a Cr/Au gate electrode by standard photolithography and lift-off process.

A micrograph of the fabricated device is given in Fig. 8. The device had two-finger channel and a gate length, L_G , of $1.6\ \mu\text{m}$ and the gate width in each channel, W_G , of $65\ \mu\text{m}$ (the effective channel width = $130\ \mu\text{m}$).

3.2 DC Characterization

$I_{DS}-V_{DS}$ characteristics of the fabricated IG-PHEMTs without and with Si ICL are shown in Figs. 9(a) and 9(b), respectively. It should be noted that voltage scales are different in these figures. Namely, it was found that the devices without Si ICL were very fragile and easily broke down. Therefore, they could be characterized at only small drain voltages. We found that high density interface states having U-shaped distribution including both donor and acceptor like states exist in insulator/InGaAs interfaces without Si ICL. Charging of these states tends to cause dielectric breakdown in the insulated gate, as well as lateral break-

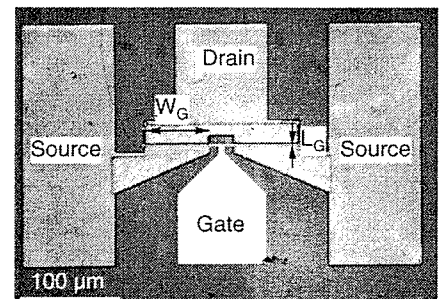


Fig. 8 A photograph of the fabricated IG-PHEMT.

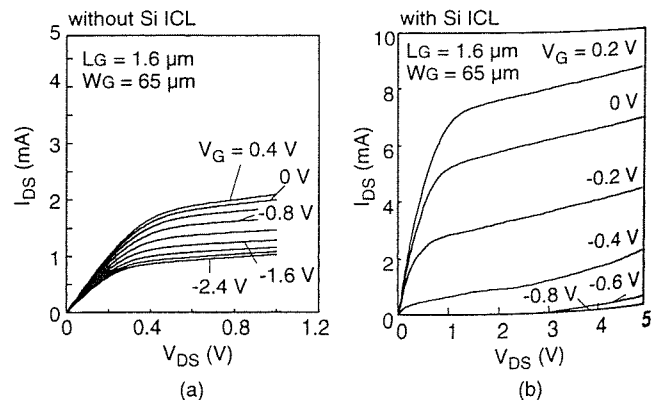


Fig. 9 $I_{DS}-V_{DS}$ characteristics of IG-PHEMTs (a) without Si ICL and (b) with Si ICL.

down due to complex surface electric field distribution along the channel, creating a local high-field region. As seen in Fig. 9(a), the IG-PHEMT without Si ICL showed poor gate controllability and small drain currents. The kink in drain currents was often seen, which was similar behavior to well-known kink in sub-micron-gate III-V semiconductor FETs. The observed kink in the present long-gate devices without Si ICL is strongly related to the surface states as discussed by Rocchi [25]. The channel could not be pinched off either. These are most likely due to presence of strong Fermi level pinning. The obtained maximum transconductance, g_m , of the device without Si ICL was 7 mS/mm for the device with $L_G = 1.6 \mu\text{m}$.

On the other hand, use of the Si ICL led to dramatic improvements of the DC characteristics of the device. An excellent gate control and complete channel pinch-off are seen in Fig. 9(b). The maximum drain currents became 4 times larger than those of the device without Si ICL. Source-drain currents could be well controlled up to $V_{DS} = 5 \text{ V}$ without any kink effects. A maximum g_m of 177 mS/mm was obtained at $V_G = 0 \text{ V}$ for $L_G = 1.6 \mu\text{m}$, being twenty times larger than the best g_m value of 7 mS/mm of the IG-PHEMT without Si ICL. The g_m of the conventional Schottky gate (SG)-HEMTs with $L_G = 1 \mu\text{m}$ was reported to be 210–377 mS/mm [26]. Taking account of a larger L_G of $1.6 \mu\text{m}$ in the fabricated IG-PHEMT, the obtained g_m value of 177 mS/mm is comparable to that of the SG-HEMTs. This shows that the fabricated IG-PHEMT realized good gate controllability. All of these improvements are due to the removal of the Fermi level pinning being consistent with the capacitance-voltage assessment. It seems that g_m values can be increased further to those of conventional sub-micron InP-based SG-PHEMTs by reducing the gate length.

As for the threshold voltage, V_{th} , the observed value was -0.6 V . A simple estimate of the threshold voltage was made using the following formula.

$$V_{th} = -qn_s(1/C_I + 1/C_B) + \phi_M/q - \chi_S - \Delta E_C/q \quad (1)$$

where ϕ_M is the work function of the gate metal, χ_S is the electron affinity of the semiconductor, ΔE_C is the conduction band offset in the InGaAs/InAlAs system. Assuming $\phi_M = 4.3 \text{ eV(Cr)}$, χ_S (InAlAs) = 3.2 V , $\Delta E_C = 0.55 \text{ eV}$, $n_s = 1.9 \times 10^{12} \text{ cm}^{-2}$, $(1/C_I + 1/C_B)^{-1} = 2.7 \times 10^{-7} \text{ F/cm}^2$ from the C - V measurements, then, V_{th} was estimated to be -0.58 V . This value agrees with the observed one.

Gate leakage currents of the IG-PHEMT with Si ICL and a SG-PHEMT are compared in Fig. 10. The reverse leakage current of the IG-PHEMT at $V_G = -0.5 \text{ V}$ was less than 0.01 nA . This was four orders of magnitude smaller than that of the SG-PHEMT. The forward gate current remained below 1 nA even at $V_G = +1 \text{ V}$. This value was 6 orders of magnitude smaller

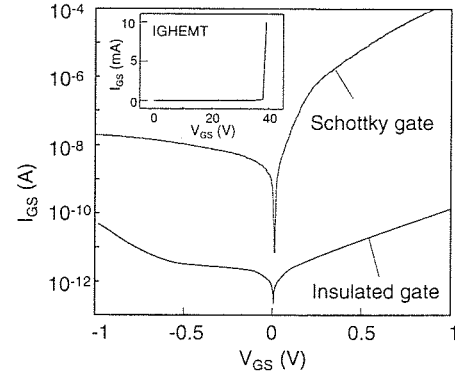


Fig. 10 Gate leakage current characteristics of the IG- and SG-PHEMTs.

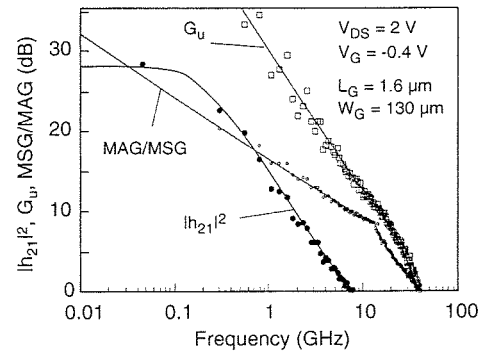


Fig. 11 On-wafer RF characteristics of the IG-PHEMT.

than that of the SG-PHEMT. Obtained low gate leakage current characteristics are useful not only for reduction of DC power consumption, but also for operations under large gate voltage swings. The off-state gate-source and gate-drain hard breakdown voltages were found to be as high as 38 V and 39 V , respectively, as shown in the inset of Fig. 10. These values were much larger than those of the SG-PHEMTs.

3.3 RF Characterization

The measured on-wafer RF characteristics of the IG-PHEMT with Si ICL are shown in Fig. 11. In spite of a long gate length of $L_G = 1.6 \mu\text{m}$, the device showed respectable RF characteristics. The 0 dB-frequency for the unilateral power gain, G_U , and that for the maximum available gain, MAG, were the same. The current gain cutoff frequency, f_T , was 9 GHz and the maximum oscillation frequency, f_{max} , was 38 GHz at $V_G = -0.4 \text{ V}$ and $V_{DS} = 2 \text{ V}$, respectively. These values of f_T and f_{max} were smaller than the reported values of a conventional SG-HEMT with $L_G = 1 \mu\text{m}$, which showed $f_T = 25\text{--}60 \text{ GHz}$ and $f_{max} = 120 \text{ GHz}$, respectively [27]. The reasons of this seems to be due to a longer gate length of $1.6 \mu\text{m}$, as well as unoptimized device design with respect to insulator thickness and parasitic elements. Use of a sub-micron gate length, optimization of the gate

insulator thickness and reduction of the parasitic resistance and capacitance will result in the improvement of the RF characteristics of the novel IG-PHEMT.

4. Conclusion

A novel InGaAs/InAlAs insulated gate (IG) PHEMT having a silicon interface control layer (Si ICL) was successfully fabricated and characterized. Systematic efforts to characterize and optimize the insulated gate structure and the PHEMT fabrication process were made using *in-situ* XPS and capacitance-voltage techniques.

This led to successful fabrication of a novel IG-PHEMT showing excellent stable DC characteristics with a good pinch off and a high transconductance ($g_m = 177 \text{ mS/mm}$), very small gate leakage currents, very high gate breakdown voltages respectable RF characteristics ($f_T = 9 \text{ GHz}$ and $f_{max} = 38 \text{ GHz}$).

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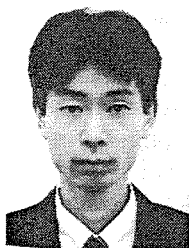
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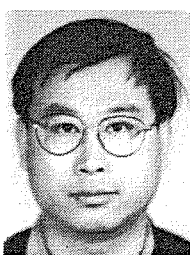
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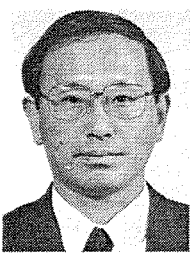
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