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Spiking neuron devices consisting of single-flux-quantum circuits (title)

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Abstract

Single-Flux-Quantum (SFQ) circuits can be used for making spiking neuron devices, which are useful elements for constructing intelligent, brain-like computers. The device we propose is based on the leaky integrate-and-fire neuron (IFN) model and uses a SFQ pulse as an action signal or a spike of neurons. The operation of the neuron device is confirmed by computer simulator. It can operate with a short delay of 100 ps or less and is the highest-speed neuron device ever reported.

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Keywords: Single-Flux-Quantum, spiking neuron device, integrate-and-fire model

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1. Introduction

The development of systems that imitate the function of biological neuron systems is one of the promising areas of research in single-flux-quantum (SFQ) electronics. At the beginning to proceed toward this goal, we propose a spiking neuron device consisting of SFQ circuits.

Brain-like computing --- the attempt to imitate human intelligence with electronic devices --- has attracted considerable attention in recent years. To embody brain-like computing, we must develop the way of constructing electrical analogs of biological neuron systems. For this purpose, several models to describe the dynamics of neurons have been proposed, though the study of neurons is still at an early stage and has yet to provide a complete picture of neurons. Among these models, the integrate-and-fire neuron (IFN) model is most used for its simplicity to analyze and simulate the behavior of neuron systems. With the IFN model, several electrical neuron systems have been produced experimentally using CMOS circuit technology [1].

In this paper, we propose a SFQ circuit that can implement the IFN model. Unlike CMOS circuits, a medium for signals in SFQ circuit is an impulse of the fluxoid quantum, so the SFQ circuit will be able to imitate the operation of neurons more precisely. In addition, SFQ circuits are superior in speed capability (three- or four-digit

faster) than CMOS circuit, so they will provide the highest-speed neuron devices ever reported. In the following sections, we first outline the IFN model (Section 2), then we propose the SFQ circuit that implement for the spiking neuron device (Section 3), and demonstrate the operation of the neuron device by means of computer simulation (Section 4).

2. IFN Model

A typical neuron can be divided into three functionally distinct parts, called dendrites, soma, and axon [2] as shown in Fig. 1. The dendrites play the role of the "input terminal" that collects signals from other neurons and transmits them to the soma. The soma is the "central processing unit" that performs an important nonlinear threshold processing step. If the total input exceeds a certain threshold, then the neuron "fires" and outputs a signal. The output signal is taken over by the "output terminal", the axon, which delivers the signal to other neurons. The signal is a short pulse of cell membrane potential called the action potential. It is called the spike, and the neuron is often called the spiking neuron. The dynamics of spiking neurons can be expressed by simultaneous differential equations such as Hodgkin-Huxley equations. However, these equations are intrinsically complex and therefore unsuitable for analyzing neuron network systems. For this reason, simple phenomenological models, especially the IFN

model, are popularly used for studies of network dynamics.

The IFN model is defined as follows. The neuron has a single variable *u(t)*, the membrane potential, given by

$$\frac{du(t)}{dt} = I(t) - \frac{u(t)}{\tau} \quad , \ldots (1)$$

I(t) is the sum of inputs for the neuron, τ is the time constant of the neuron, and *t* is time. The neuron outputs an impulse spike when *u(t)* exceeds a threshold value. After producing the output, the neuron resets *u(t)* to 0 to repeat the same operation. The next section, we propose a SFQ circuit that imitates the behavior of the IFN model.

3. Circuit Configuration

The spiking neuron device we propose uses a SFQ pulse as the impulse signal. It consists of three SFQ subcircuits, i.e., an input subcircuit, a leaky integrator subcircuit, and an output subcircuit. They correspond to dendrites, soma, and axon of biological neurons, respectively. The input subcircuit is a simple confluence buffer that collects SFQ pulses from other neuron devices and sends the pulses to the leaky integrator subcircuits. The leaky integrator subcircuit is the key component of our device. It accumulates or stores input fluxoid quanta and outputs an SFQ pulse when the number of stored fluxoid quanta exceeds a threshold. The output subcircuit sends the output SFQ pulse to other neurons and simultaneously produces resetting pulses for the leaky

integrator. In constructing our device, we used SFQ elementary circuits given in [3].

3.1. Leaky Integrator subcircuit

Figure 2 shows the leaky integrator subcircuit. The leaky integrator consists of Josephson memory loops from LA_1 to LA_N connected with a damping resistor R_1. Each Josephson junction from J_1 to J_N is biased with a dc bias current (denoted by idc). Junction J_0 is designed so that its critical current will be larger than that of other junctions, and is not biased. The circuit receives SFQ pulses from the input subcircuit and stores the flux quanta in its loops. The stored flux quanta in the right end loop (J_1-LA_1-R_1-J_0) fade away with a certain time constant because of the damping resistor R_1. In this circuit, we define the total current in the loops as an internal state of the neuron device that corresponds to "membrane potential" (the total current means current in LA_1 + current in LA_2 + … + current in LA_N). The number of the loops corresponds to the threshold for the firing. If many SFQ pulses arrive in a short time, the number of the stored flux quanta reaches the threshold, and the leaky integrator produces an output pulse through inductor LB_1 coupled with LA_N.

3.2. Output subcircuit

Figure 3 shows the output subcircuit consisting of ordinary Josephson transmission lines combined with SFQ pulse splitters and confluence buffers. The number of splitters

and confluence buffers are set at the same number of the memory loops in the integrator. The circuit receives a SFQ pulse from the leaky integrator and sends it to an output terminal. At the same time, with the output SFQ pulse, the circuit produces resetting SFQ pulses for the integrator. The resetting pulses are applied to the resetting terminal of the integrator. Then the current in the junction J_0 exceeds a critical current level, so the junction turns to normal conduction. In consequence, the stored pulses and the resetting pulses cancel each other and vanish. Because the number of the stored flux quanta and the resetting pulses are the same, the internal state of the integrator is initialized.

In the above discussion, the input pulses are assumed only as an excitatory input. However, a biological neuron has also an inhibitory input. In order to imitate the inhibitory property, we adopt the inhibitory input terminal in the output subcircuit as shown in Fig. 3. Using this terminal, a stored flux quantum and an inhibitory pulse cancel each other, and we can imitate the inhibitory property of the neuron.

4. Construction of the IFN Device and Simulation Results

The entire circuit of the SFQ neuron device is shown in Fig. 4. The number of the memory loops in the leaky integrator is 5 in this example. The input subcircuit collects SFQ pulses from other neuron devices and sends the pulses to the leaky integrator

subcircuit. The leaky integrator performs the threshold processing, and produces an output SFQ pulse when the total input exceeds a certain threshold for firing. We confirmed the operation of the circuit by computer simulation. The circuit parameters were: N = 5, LA_N = 8 pH (N = 1 ~ 5), idc = 0.1 mA, and R1 = 30 mΩ. The mutual induction coefficient between inductors LA_5 and LB_1 was assumed to be 0.7. For each Josephson junction, parallel resistance of 4 Ω and parallel capacitance of 0.1 pF were assumed. The critical current was 0.3 μA for junction J_0 and 0.13 μA for the other junctions.

The simulated operation is shown in Fig. 5. The waveforms for (i) input pulses, (ii) the internal state, and (iii) the output of the device are plotted. The input and the output waveforms represent the voltage of the corresponding nodes of the device circuit, and the internal state shows the amount of the total current in the memory loops of the leaky integrator. For a low density of input pulses (region (A) in the figure), the device produced no output pulse because the internal state of the device was unable to reach the threshold for firing. This is so because the stored flux quanta in the loops fade away with time by the damping resistor R_1. In contrast, for a high density of the input pulses (region (B) in the figure), the internal state increased to reach the threshold for firing. The neuron device produced an output SFQ pulse and then initialized its internal state

(region (C)).

5. Conclusion

A spiking neuron device consisting of Single-Flux-Quantum (SFQ) circuits has been presented. The circuit we propose is based on the integrate-and-fire neuron (IFN) model and uses a SFQ pulse as an action signal or a spiking pulse of neurons. The complete spiking neuron device was composed of an input subcircuit, a leaky integrator subcircuit, and an output subcircuit. It can imitate the operation of the neuron based on the IFN model, and operate with a short delay of 100 ps or less is the highest speed neuron device ever reported. The operation of spiking neuron device was confirmed through the SPICE simulation.

Reference

[1] Wolfgang Maass, Christopher M. Bishop (Eds.), Pulsed Neural Networks, MIT Press, Cambridge, 2001, pp. 133–236.

[2] Wulfram Gerstner, Werner Kistler (Eds.), Spiking Neuron Models, Cambridge University Press, Cambridge, 2005, pp. 93–102.

[3] Theodore Van Duzer, Charles W. Turner (Eds.), Principles of Superconductive Devices and Circuits second edition, Prentice Hall PTR., New Jersey, 1999, pp. 218–325.

Figure captions:

Figure 1. Schematic image of a neuron.

Figure 2. Leaky integrator subcircuit with N memory loops. “idc” represents a bias current for each Josephson junction. The critical current of the Josephson junction (J0) is set larger than that of other junctions. Inductors LA_N and LB_1 are coupled with each other.

Figure 3. Output subcircuit consisting of N splitters and confluence buffers.

Figure 4. Spiking neuron device consisting of SFQ circuits. The number of the loop memory is set at 5 loops.

Figure 5. Operation of the neuron devices. Simulated results of (i) input pulses, (ii) internal state, and (iii) output pulse.

Figure 1

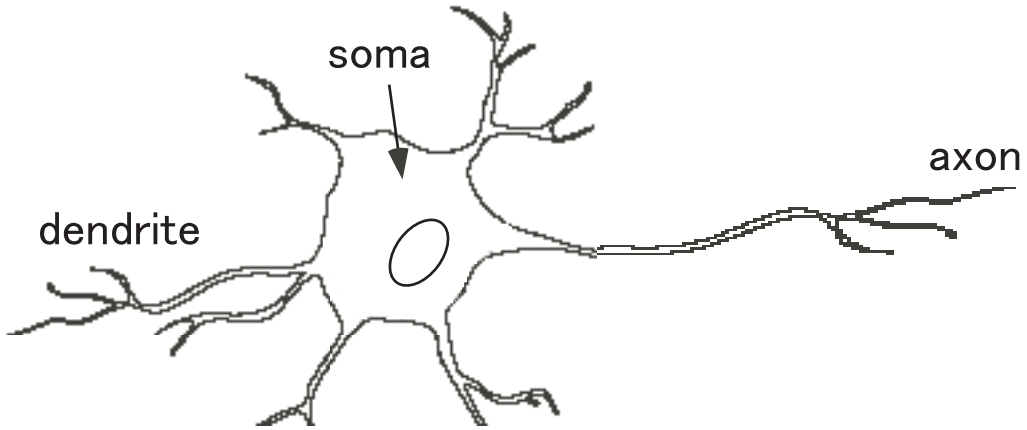


Figure 2

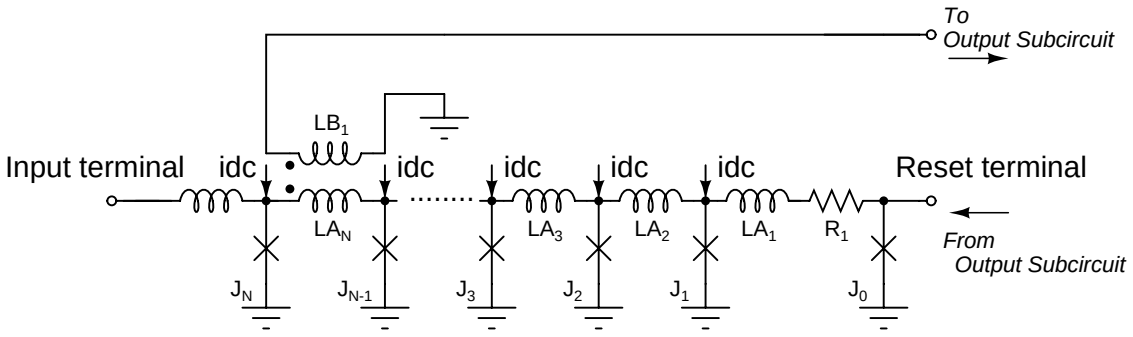

To
Output Subcircuit
LB1
Input terminal
idc
idc
idc
idc
idc
Reset terminal
LAN
LA3
LA2
LA1
R1
From
Output Subcircuit
JN
JN-1
J3
J2
J1
J0

Figure 3

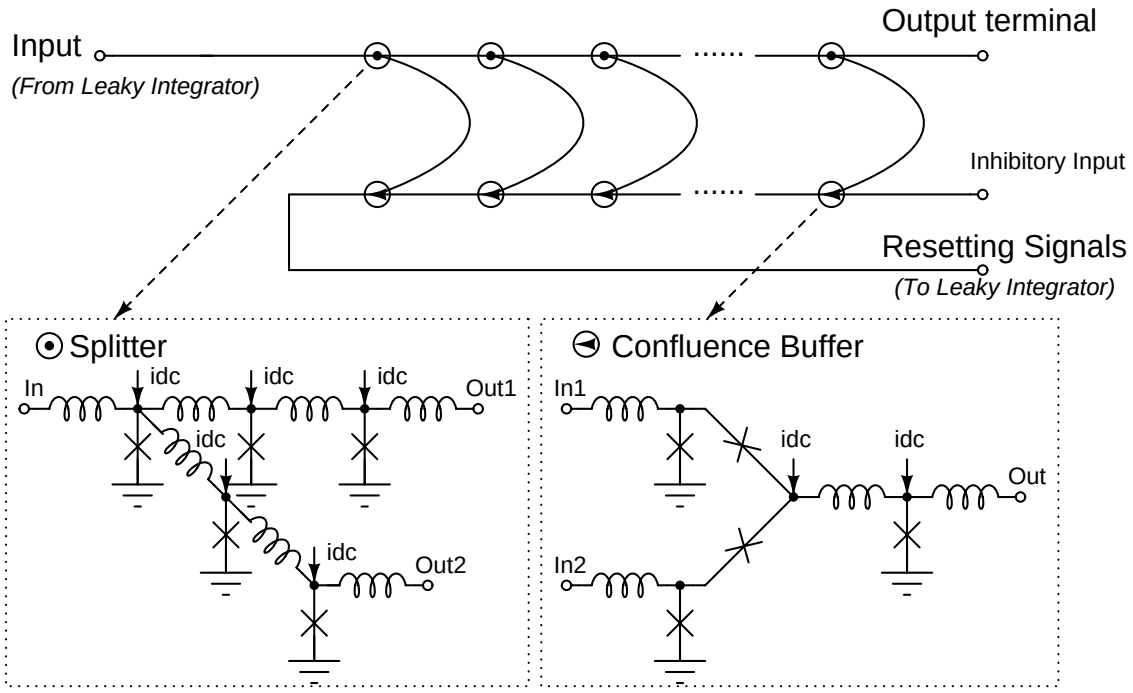

Input
(From Leaky Integrator)
Output terminal
Inhibitory Input
Resetting Signals
(To Leaky Integrator)
Splitter
In
idc
idc
idc
Out1
idc
idc
Out2
Confluence Buffer
In1
In2
idc
idc
Out

Figure 4

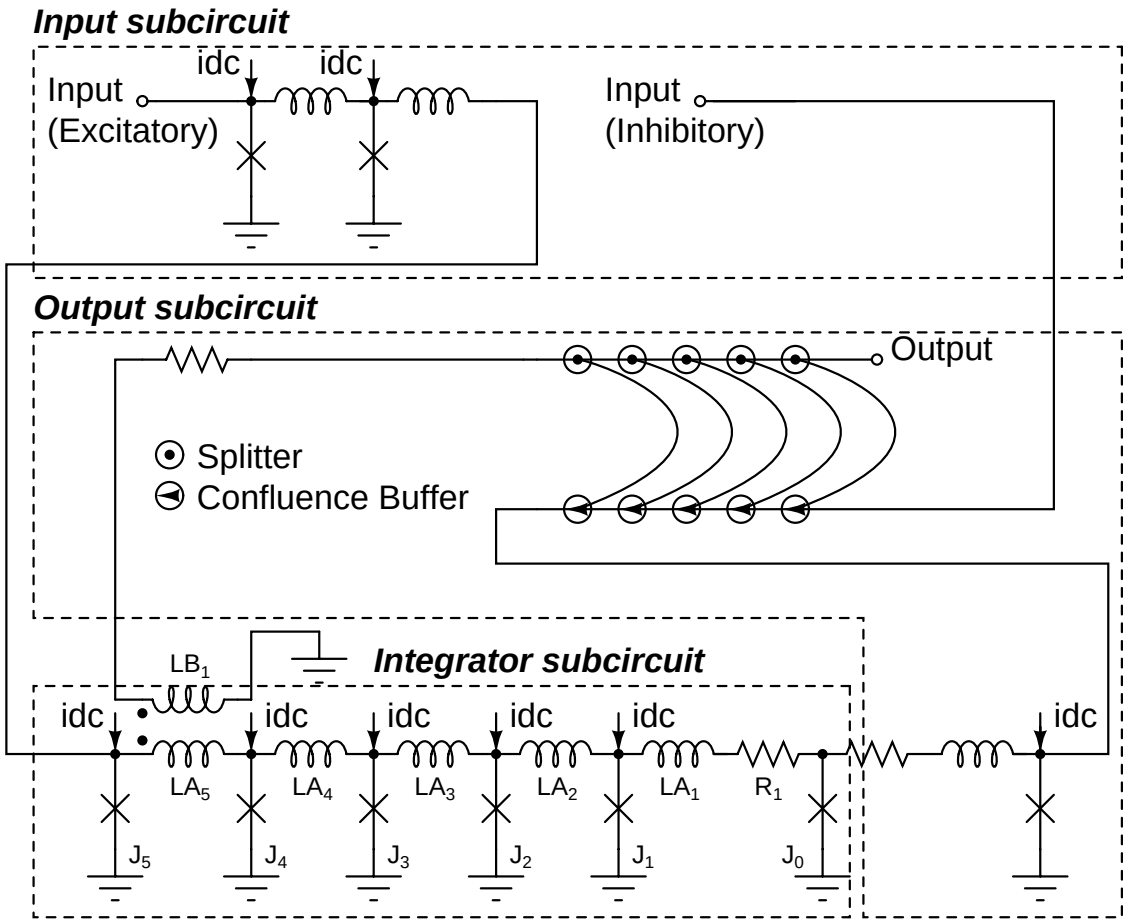
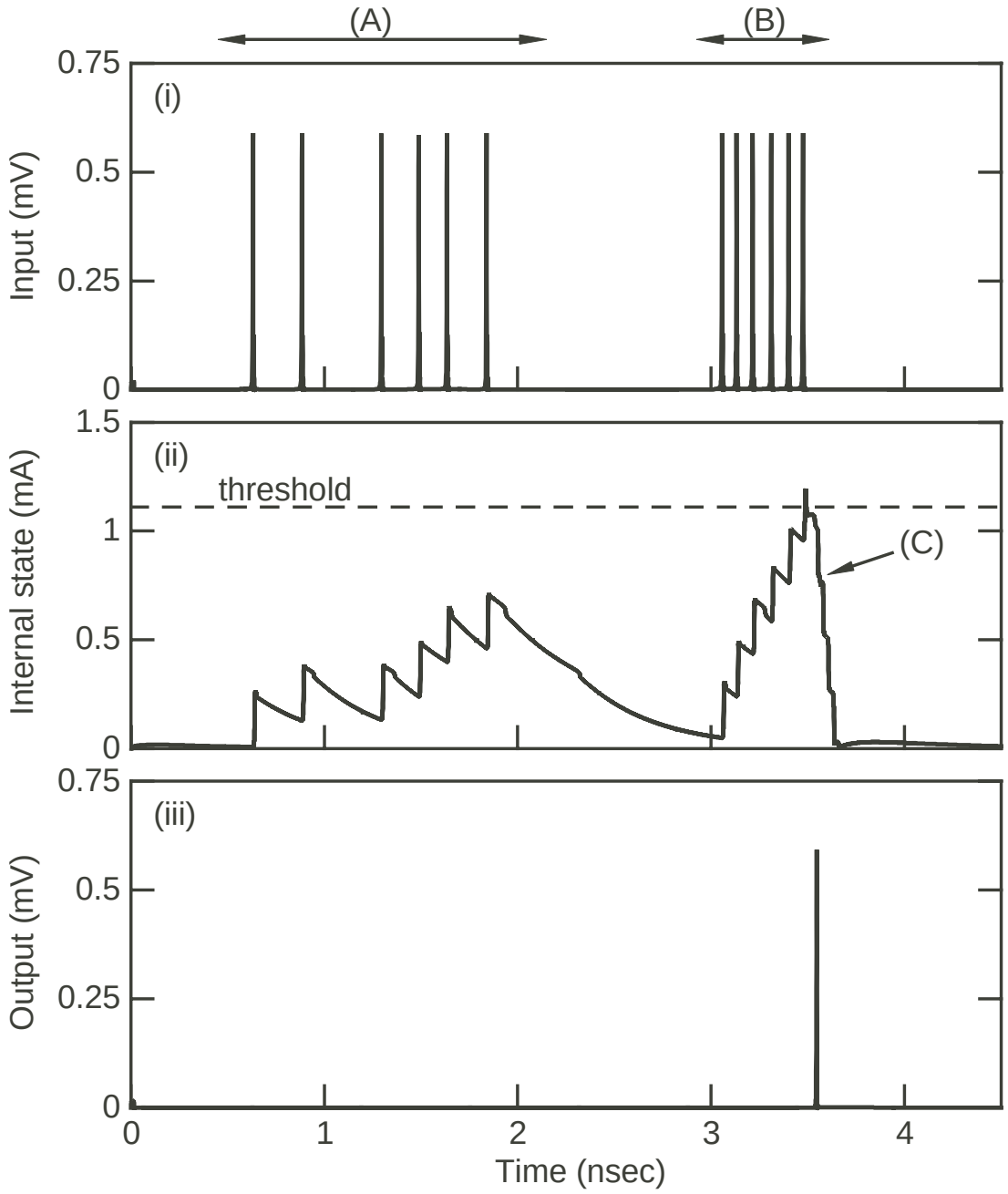

Input subcircuit
idc
idc
Input
(Excitatory)
Input
(Inhibitory)
Output subcircuit
Output
Splitter
Confluence Buffer
LB1
Integrator subcircuit
idc
idc
idc
idc
idc
idc
LA5
LA4
LA3
LA2
LA1
R1
J5
J4
J3
J2
J1
J0

Figure 5


(A)
(B)
(i)
Input (mV)
0.75
0.5
0.25
0
(ii)
threshold
(C)
Internal state (mA)
1.5
1
0.5
0
(iii)
Output (mV)
0.75
0.5
0.25
0
0
1
2
3
4
Time (nsec)